BITS PILANI, DUBAI CAMPUS

II SEMESTER 2011-12

COURSE	:	**CS C444 / EEE C444 REAL-TIME SYSTEMS**
YEAR	:	**IV YEAR ELECTIVE**
COMPONENT	:	**TEST 2 (OPEN BOOK)**
DATE & DURATION	:	**16/05/2012 & 50 MINS**
WEIGHTAGE	:	**20 % (20 MARKS)**

Note: 1. Answer all the Questions and use required assumptions and mention them clearly in answer sheet.
2. Number of pages: 2.
3. Draw the design clearly and do not overwrite the design. ***Make your own assumption wherever needed.***

1. Check whether the given set of tasks can be schedulable using RMA 1 method with overload. The table given below shows the tasks and its parameters. The loss is 19% per KHz, find the rate, and overhead. (4 Marks)

Task	Computation Time	Period	Frequency	Utilization	Priority
T1	6	15	66	?	?
T2	4	20	75	?	?
T3	5	30	34	?	?

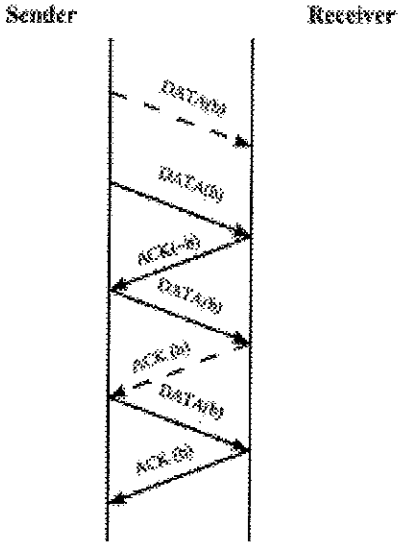
2. Give the Data Flow Diagram for the following problem of statement describing for a manufacturing cell. As components to be assembled by a robot are placed on fixtures, a status bit is set within a **parts status buffer** (a control store) that indicates the presence or absence of each component. Event information contained within the **parts status buffer** is passed as a bit string to a process, *monitor fixture and operator interface.* The process will read **operator commands** only when the control information, bit string, indicates that all fixtures contain components. An event flag **start / stop flag,** is sent to *robot initiation control,* a control process that enables further command processing. Other data flows occur as a consequence of the **process activate** event that is sent to *process robot commands.* (4 Marks)
3. Design a State Chart which specifies the behavior of the coolant monitor in a nuclear reactor that monitors the coolant flow in an experimental nuclear reactor. In this application there are three levels of processing: as *foreground process, dispatcher, and background process.* In foreground process (FG) there are three processes: *a timer process (T) has responsibility for maintaining elapsed time for use by a background alarm clock task and for time stamping events. A second task in FG- F is the second process which detects, isolates, and handles faults by reconfiguring the hardware. The third process in FG is the S process performs the principal application functions of reading and processing coolant flow and related data from sensors. The Background tasks (B) contain less critical processes for testing and display.* The Dispatcher is triggered by a timer interrupt on a 100

ms cycle. One each cycle, it successively activates T, F, and S; each runs to completion and then returns to the Dispatcher. The processes of B are then dispatched in the remaining cycle time. (4 Marks)

4. Construct a efficient DFD for a Billing Application, similar to one at a supermarket check-out stand, for each customer transaction, a running itemized bill is computed and the parameters for the billing applications are as follows: the input ***Transaction_Control*** provides the control data for the start and end of each transaction, denoted by ***start_trans*** and ***end_trans***, respectively. At the end, the itemized bill, named bill, is read from Bill and then ouput by the print_Bill function. The ***Compute_Cost*** function computes the total cost of an item and sends the result to ***Update_Bill*** which then updates the ***Bill*** data.

(4 Marks)

5. Give the Petri Net Model for the following: The temporal sequence of possible internal events in the data transfer phase of the Alternating Bit Protocol (A B Protocol). The operation of the AB protocol is described as follows. The sender sends a `DATA' message to the receiver and simultaneously enables its internal retransmission timer. Each DATA message sent by the sender to the receiver is accompanied by an additional bit `b'. The value of this control bit alters with each new DATA message. The receiver, on receiving the DATA, acknowledges it by sending an ACK message accompanied by the same control bit b that accompanied the DATA. If no acknowledgment reaches the sender before the timer expires, a copy of the message is sent after each timeout repeatedly, until its reception is acknowledged. The DATA LOST during the transfer operation is to be considered in the design of the petri net modeling.



(4 Marks)

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II SEMESTER 2011-12

COURSE : EEE C444 / CS C444 REAL-TIME SYSTEMS
COMPONENT : QUIZ-2
DATE : 25-04-20112 MARKS : 7 MARKS
DURATION : 20 MINS

NAME: _____ ID NO.: _____

1. In stack architecture, instructions are centered on an internal memory store called _____ and on an _____. (1 Mark)
2. Disabling interrupts does not remove the interrupt; rather, the CPU "hold off" the interrupt until an Enable Priority Interrupt instruction is executed. (True / False) (½ Mark)
3. The technique of overlapping of the fetch-execute cycle is _____. (½ Mark)
4. Some processors seek to reduce the programmer's coding responsibility, increase execution speeds, and minimize memory usage. Processors of this type are termed as (½ Mark)

   a) RISC b) CISC c)RSIC d)SISC
5. Fusible-link ROMs are non-volatile and they are called PROM or PLA, consist of an array of paths to ground called fusible links. (True / False) (½ Mark)
6. The new memory technology for programmable ROMs has emerged, they are Flash Memory; it uses _____ per bit. (½ Mark)

   a) Two register b) single transistor c) one register d) none of the above
7. The Programmed I/O has the special instructions in the CPU instruction set, used to transfer the data to and from the CPU; they are _____ and _____. (1 Mark)
8. What is the system signal prevent CPU from performing a data transfer during DMA ? _____ (½ Mark)
9. The Interrupt Controller (external) have the built-in ability to prioritizes and handle multiple interrupts. This device can be used to enable a CPU with a single interrupt input to handle interrupts from several sources. (True / False) (½ Mark)
10. _____ are used to ensure that certain devices are serviced at regular intervals and that the CPU continues to function. (½ Mark)
11. Why is DMA controller access to main memory in most systems given higher priority than CPU access to main memory? (1 Mark)

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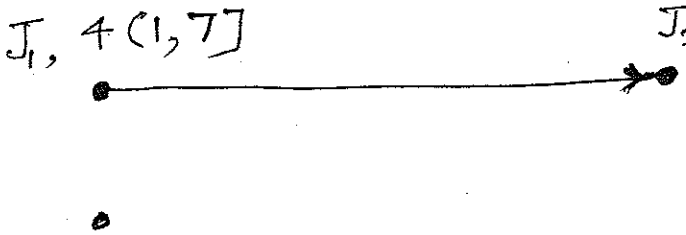
II SEMESTER 2011-12

COURSE	:	CS C444 REAL-TIME SYSTEMS
YEAR	:	IV YEAR ELECTIVE
COMPONENT	:	QUIZ – 1 (CLOSED BOOK)
WEIGHTAGE	:	8 % (8 Marks)
DATE & DURATION	:	14-03-2012 & 20 MINS.

NAME: _____ ID. NO.: _____

1. Real-Time Systems _____ (½ Mark)
   a) Must be embedded
   b) respond to external events in a timely fashion
   c) can never tolerate missed deadlines
   d) require a kernel
2. Response time is the total time: _____ (½ Mark)
   a) It takes to convert analog to digital display thermometer
   b) It takes to resolve a number flight simulation game
   c) Between seeing a stimulus and finally acting according to that stimulus
   d) A processor is utilized
3. An automatic Teller machine from the perspective of the Banking systems would be classified as what type of real-time system: _____ (½ Mark)
   a) Soft
   b) Hard
   c) Medium
   d) firm
4. Failure to meet a soft real-time requirement would most probably result in a death _____
   a) True (½ Mark)
   b) False
5. An embedded navigational system for an autonomous weed killer would be considered : _____
   a) Soft RTS (½ Mark)
   b) Catastrophic RTS
   c) Ridiculous RTS
   d) Firm RTS
6. Process of scheduling and switching CPU between several tasks: _____
   a) Preemptive (½ Mark)
   b) Asynchronous
   c) Non-preemptive
   d) multitasking
7. In non-preemptive scheduling, release of the CPU is determined by the kernel: _____
   a) True (½ Mark)
   b) False
8. The _____ algorithm has been used for scheduling real-time traffic in high-speed switched networks. (1 Mark)

9. Using Minimum-Laxity-First Algorithm schedule the given task graph and check whether they all meet their deadlines. (2 Marks)



10. The _____ and _____ algorithms are not optional when the system is overloaded so some jobs must be discarded in order to allow other jobs to complete in time. (1 mark)

11. In real-time systems, what does precedence graph represent? (½ Mark)