BITS Pilani, Dubai Campus

II SEMESTER 2011-2012

COMPREHENSIVE EXAM

EEE C443 ANALOG AND DIGITAL VLSI DESIGN

7 JUNE 2012 **MAX MARKS: 35**

DURATION: 3 HOURS **WEIGHTAGE: 35%**

Question 1 (1.5 + 2 + 1.5 + 2 + 1.5 + 2 = 10.5 Marks)

1) Draw a CMOS differential amplifier circuit.
    a. Redraw this diagram to obtain a voltage-voltage feedback configuration.
2) Draw a CMOS common gate amplifier circuit.
    a. Redraw this diagram to obtain a voltage-voltage feedback configuration.
    b. Redraw this diagram to obtain a voltage-current feedback.
3) Draw a CMOS common source amplifier circuit.
    a. Redraw this diagram to obtain a current-voltage feedback configuration.
    b. Redraw this diagram to obtain a voltage-current feedback configuration.
    c. Redraw this diagram to obtain a current-current feedback configuration.

Question 2 (1 + 1 + 1 = 3 Marks)

Analyze the impact of feedback on Gain, R_{out} and R_{in} given the following expressions (see under Formulae Section). State all assumptions.

Question 3 (1 x 5 + 1 + 0.5 + 1 = 7.5 Marks)

Given the following values:

$g_m \sim 10^{-4}$ A/V

$g_{mb} \sim 0.1\ g_m$

$g_o \sim 0.01\ g_m$

Temperature = 27 degrees Celsius

A. Make suitable design assumptions and obtain the input referred thermal noise for the following configurations:
    1) Common Source
    2) Common Gate
    3) Source Follower
    4) Cascode
    5) Differential Amplifier

Analyze the impact of R_D and g_{m2} on the above noise values by calculating the input referred noise for 3 carefully chosen values for these parameters.

B. Why is input referred noise preferred over output noise?
C. Explain the corner frequency with mathematical expressions.
D. Analyze the tradeoff between output SNR and bandwidth.

Question 4 (1 + 1 + 2 + 2 = 6 Marks)

1) Draw a CMOS transistor based four-input NAND gate.
2) Draw the corresponding RC model.
3) Determine the resistance and capacitance values (not numerically) that impact the propagation delay of the following transitions:
    a. 0000 to 1111
    b. 0001 to 1111
    c. 1111 to 1100
    d. 1111 to 1110
4) Explain the concept of Dynamic CMOS Design for **Out = (AB + CD)'**.

Question 5 (0.5 x 4 = 2 Marks)

Explain the following metrics for a CMOS inverter.

1) Noise Margin.
2) Fan-in
3) Transistor Sizing
4) Power Dissipation

Question 6 (3 + 2 = 5 Marks)

1) Draw a block diagram of a finite state machine, using positive edge triggered registers. Explain, with diagrams and relevant expressions, the factors that affect clock speed.
2) Draw the transistor-level implementation of a positive latch built using transmission gates.

Question 7 (1 Mark)

Draw a 8x8 NAND ROM that stores the following values at addresses 0 to 7: 00000000, 00000010, 00000000, 00001000, 00100000, 00000000, 10000000, 00000000.

☺ WISH YOU ALL THE BEST IN THE EXAM AND IN THE FUTURE ☺

BITS PILANI, DUBAI CAMPUS

Dubai International Academic City

Second Semester 2011 – 2012

Analog & Digital VLSI Design EEE C443 (IV year)

Test 2 (Open Book)

Duration : 50 minutes **Weightage : 20%**

30 April 2012 **MAX : 20 Marks**

Note: Show all working to get full credit.

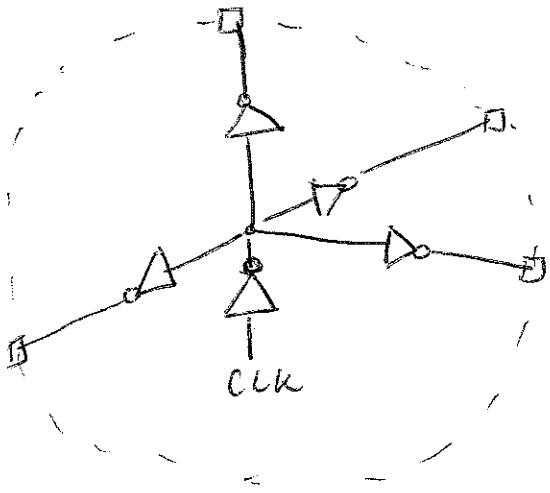
Question 1 (**4 Marks**)

Design and draw the connections for a memory with the following values in addresses 0, 1, 2, and 3: 1100, 0110, 1001, and 1101 using

1) MOS NOR ROM
2) MOS NAND ROM

Question 2 (**2 Marks**)

Clock can be distributed using H-Tree network and Bailey's Grid Structure. Analyze the following clock distribution network for its advantages and disadvantages.



Question 3 (**4 Marks**)

Design and draw a ***static*** master-slave ***negative*** edge-triggered register using multiplexers based on CMOS transistors.

Question 4 (**3 + 2 = 5 Marks**)

You are given the following values for 0.35 μm technology:

$R_D = R_S = 100\ K\Omega$.

$1/g_m = 10\ K\Omega$.

$1/g_{mb} = 100\ K\Omega$.

$1/g_o = 1000\ K\Omega$.

A. Using the above values ***appropriately***, calculate the voltage gain of the following amplifier configurations:
   1) Common Source Stage with Resistive Load that includes the transistor output resistance.
   2) Common Source Stage with Diode Connected Load
   3) Common Source with Current-Source Load
   4) Common Source with Source Degeneration.
   5) Source Follower.
   6) Common Gate.

   Make and state all reasonable assumptions including diagrams of configurations.

B. If voltage gain was the only design criterion, which configuration would you choose? If you included other criteria, which configuration would you choose? Justify your answer.

Question 5 (**3 + 1 + 1 = 5 Marks**)

Draw two-stage and a three-stage basic current mirror to obtain a current amplification of 8. Draw the transistor diagram for each of these configurations and state the aspect ratio for each transistor.

1) If you could use a Cascode current mirror, would you use it? Justify your answer.
2) If you could use a Active Current Mirror, would you use it? Justify your answer.

Test - 1

Question 1 (Total Marks: 12)

Question 1.1 (**3 Marks**)

The parameters for a manual model of a generic 0.25 micron CMOS process (minimum length device) is given below.

	V_{T0} (V)	$\gamma(V^{0.5})$	V_{DSAT} (V)	K' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30×10^{-6}	-0.1

1) Calculate the ratio $(W/L)_p/(W/L)_n$, for an inverter, given by

$$(W/L)_p/\ (W/L)_n \ = \ [k_n'V_{DSATn}(V_M-V_{Tn}-V_{DSATn}/2)]/[\ k_p'V_{DSATp}(V_{DD}-V_M+V_{Tp}+V_{DSATp}/2)$$

for V_{DD} = 2 V.

2) Given that the above ratio is 3.5 for V_{DD} = 2 V, discuss briefly the impact of V_{DD} on the ratio.

Question 1.2 (**3 Marks**)

In 0.25 micron technology, the equivalent resistance R_{eq} (W/L = 1) of NMOS and PMOS transistors is given below. For larger devices, divide R_{eq} by W/L.

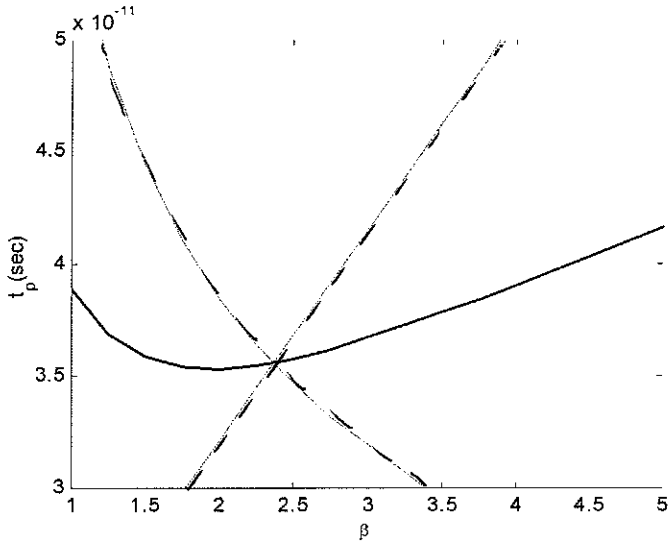
V_{DD}	1	1.5	2	2.5
NMOS (KΩ)	35	19	15	13
PMOS (KΩ)	115	55	38	31

Given that C_L is 6.1 fF for high to low transition and 6.0 fF for low to high transition, calculate, for an inverter,

1) t_{pHL}
2) t_{pLH}
3) average value of t_p
4) given that t_p is 32.5 ps for V_{DD} = 2.5 V, compare the propagation delays for the two supply voltage values.

Question 1.3 (**3 Marks**)

Based on the diagram given below and based on the propagation delays given/calculated for the two supply voltages, are these delays the best or would you choose some other value? Justify your answer.



$$\beta = W_p / W_n$$

Question 1.4 (**3 Marks**)

1. Calculate the dynamic power dissipation for an inverter for V_{DD} = 1.5 V.
2. Given that the dynamic power dissipation for an inverter with V_{DD} = 2.5 V is 580 µW, compare the variation of dissipated power with supply voltage and propagation delay.

Question 2 (Total Marks: 13)

Question 2.1 (**4 Marks**)

Synthesize and draw the static design of the following logic using PDN and PUN.

Output = [(A+B).(C+D)]'

Question 2.2 (**3 Marks**)

Write down all possible expressions for (based on various combinations of inputs) t_{pHL} and t_{pLH} in terms of R_n, R_p, C_L.

Question 2.3 (**3 Marks**)

Write down the expression for the minimum and maximum dynamic power dissipation for this CMOS design.

Question 2.4 (**3 Marks**)

Design and draw the circuit using dynamic CMOS design. What is one advantage of dynamic CMOS design for the given logic?

BITS Pilani, Dubai Campus

Dubai International Academic City, Dubai

Second Semester, 2011-2012

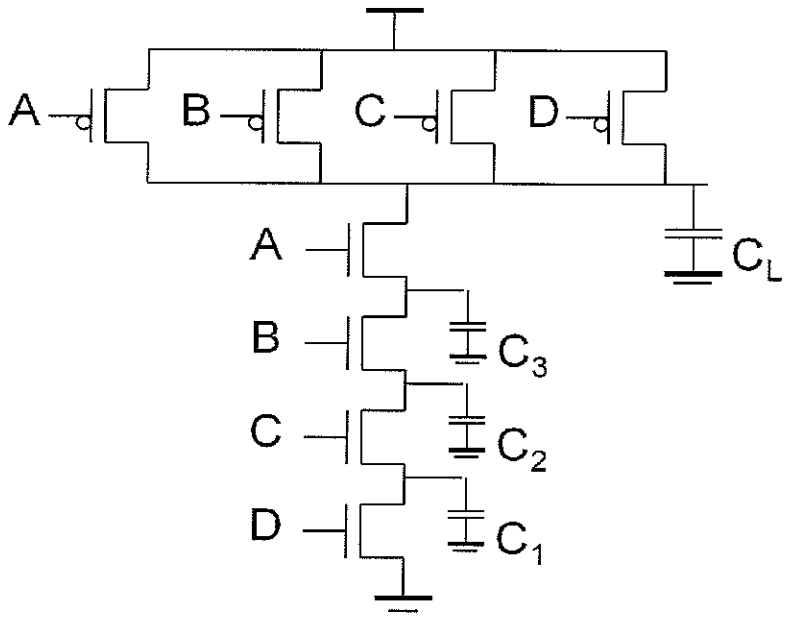
Analog and Digital VLSI Design, EEE C443 (IV Year)

Quiz I (Closed Book)

Duration: 25 Minutes **Weightage: 8%**

25 March 2012 **Mark: 8 Marks**

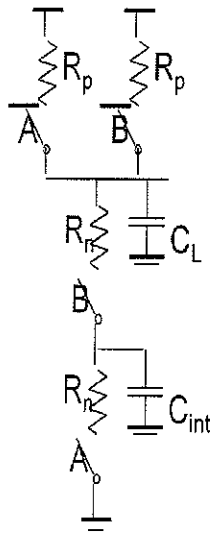
Question 1 (1.5 Marks)



For the above circuit, which of the following expressions is likely to be the correct one for propagation delay?

a) $t_{pHL} = 0.69\ R_{eqn}C_L$
b) $t_{pHL} = 0.69\ R_{eqn}(C_1+2C_2+3C_3+4C_L)$
c) $t_{pHL} = 0.69\ R_{eqn}(C_1+C_2+C_3+C_L)$

Question 2 (2 Marks)



In the above circuit, which of the following would be the best choice of transistor choices, given that we want t_{pHL} (worst case) to be approximately equal to t_{pLH} (worst case)? Assume that R_{eqn} = 15 K and R_{eqp} = 38 K for 0.25 micron technology for W/L = 1.

a) $(W/L)_{A,p} = (W/L)_{B,p} = (W/L)_{A,n} = (W/L)_{B,n} = 2$
b) $(W/L)_{A,p} = 2 = (W/L)_{B,p}$, $(W/L)_{A,n} = 1 = (W/L)_{B,n}$
c) $(W/L)_{A,p} = 1 = (W/L)_{B,p}$, $(W/L)_{A,n} = 1 = (W/L)_{B,n}$

Question 3 (1 Mark)

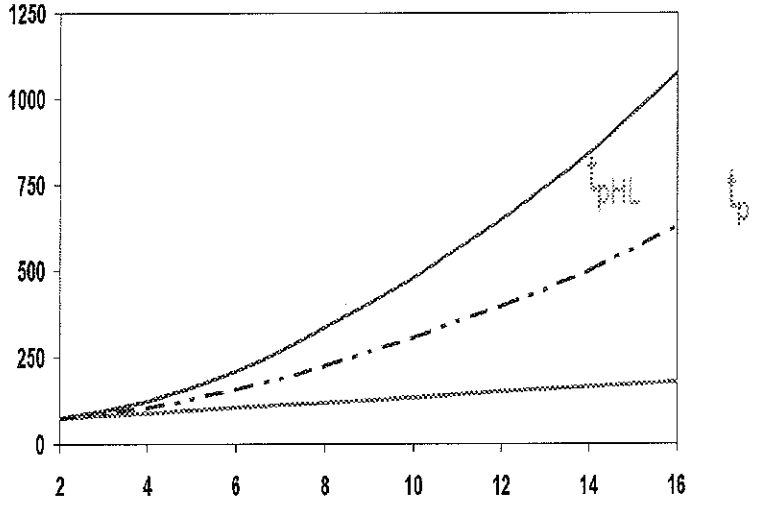
Would the dynamic CMOS implementation of the gate in Question 2, have better or worse t_{pHL} than the static CMOS design?

Question 4 (1 Mark)

In the diagram below propagation delay (y-axis) is plotted against fan-in (x-axis)

The fan-in should be

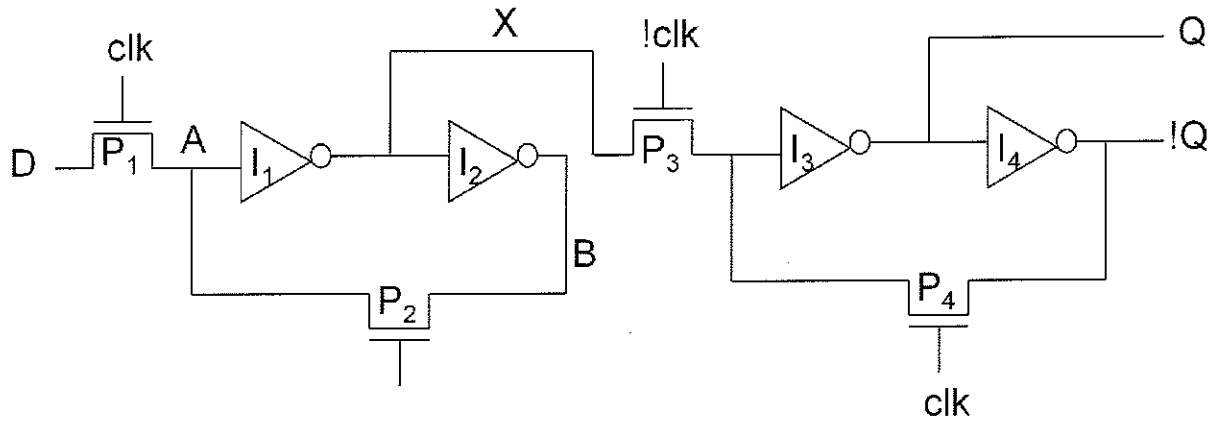
a) Between 12 and 16
b) Between 2 and 6
c) Between 2 and 4
d) Between 6 and 12



Question 5 (1.5 Marks)

A race condition occurs in circuit below when

1) Clk is high
2) Clk is high and D = 0
3) Clk is high and D = 1



Question 6 (1 Mark)

Draw the dynamic CMOS design circuit for the dynamic edge triggered register.