BITS PILANI – DUBAI

International Academic City, Dubai

Second Semester 2010 – 2011

Analog and Digital VLSI Design EEE C443 (IV year)

Comprehensive Exam (Closed Book)

Duration: 3 Hours **Weightage: 35%**

Date: 5 June 2011 **MAX: 35 Marks**

Note: Show all working to get full credit.

Question 1 (Total: 15 Marks)

Use the datasheet provided for the inverter IC ELM7504B.

Part 1 (Noise Margins) (1 + 1 + 2 + 2 + 2 + 2 = 10 Marks)

i. Draw the ideal VTC for any inverter.
ii. Draw a piecewise linear approximation of the VTC for the inverter specified in IC ELM7504B.
iii. Calculate the switching threshold, V_M, using the datasheet for VDD = 2V, 4.5V and 6V.
iv. Calculate noise margins, NM_H and NM_L, using the datasheet for VDD = 2V, 4.5V and 6V.
v. Calculate the ideal switching threshold for VDD = 2V, 4.5V and 6V.
vi. Compare the switching threshold obtained in part (v) with the ideal switching threshold calculated in part (v). How can we design the inverter to get closer to the ideal switching threshold?

Part 2 (Device Sizing to obtain desired switching voltage V_M) (3 + 2 = 5 Marks)

i. Calculate the PMOS to NMOS ratio for ELM7504B for 0.25 micron technology for VDD = 2V, 4.5V and 6V and for the V_M calculated in Part 1.
ii. Calculate the value for W each of the cases in part (i).

Question 2 (5 + 2 + 5 + 5 + 5 = 22 Marks)

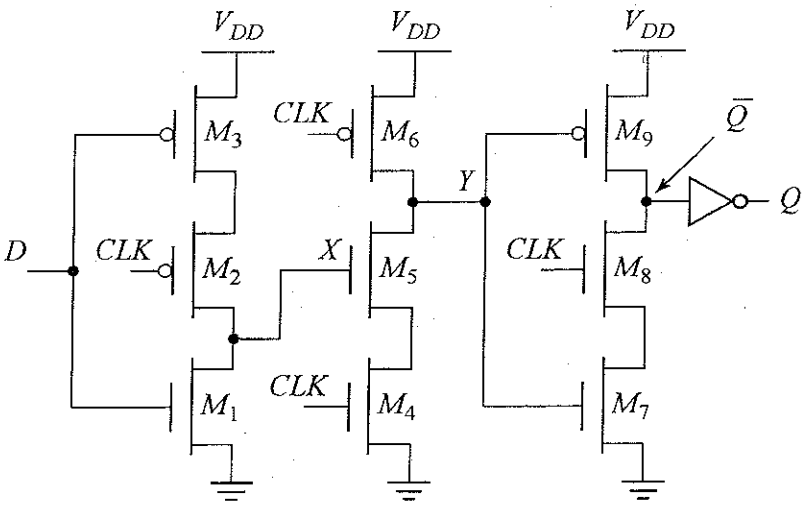
1. Given the following logic, design and draw the transistor circuits using concepts of pull up and pull down: $OUT = \overline{D + A(B + C)}$.
2. Draw the RC Model for this circuit (example for an RC Model is given in the *Useful Formula and Information* section). You can ignore C_{int} in your circuit.
3. Calculate the delay when the input changes from (assume that all NMOS transistors are identical and that R_N = 13 KΩ; assume that all PMOS transistors are identical and R_P = 31 KΩ; assume C_L = 3 fF)
   a. A = B = C = D = 1 to A = B = C = 1, D = 0

b. A = B = 0; C = D = 1 to A = 1; B = C = D = 0

4. For the above logic and transistor circuit, calculate the propagation delay t_{pHL}? (Hint: how many ways are there in which OUT = 1 can become OUT = 0 ?). Assume resistor and capacitance values as in part (3).
5. Assuming that each transistor is purely a switch combined with a resistor, calculate the power consumed by the circuit for each of the 16 combinations of A, B, C, and D. Assume that all NMOS transistors are identical and that R_N = 13 KΩ; assume that all PMOS transistors are identical and R_P = 31 KΩ. Assume also that V_{DD} = 5V.

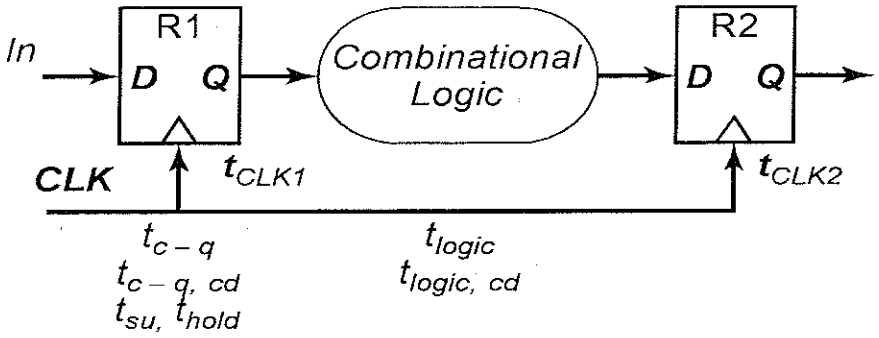
Question 3 (6 Marks)

For the given circuit below draw the timing diagram showing CLK, D (your choice of at least 2 values e.g., 0101), X, Y, Q and Q^c. Explain what function the circuit accomplishes.



Question 4 (4 + 6 = 10 Marks)

1. For the diagram below, draw labeled timing diagrams to illustrate the various parameters that affect clock speed.



2. The following inequalities are to be satisfied for good functioning of a circuit.

a. $$T_{c\text{-}q} + T_{LM} + T_{SU} < T - T_{JI,1} - T_{JI,2} - \delta$$

b. $$T_{c\text{-}q} + T_{LM} - T_{JI,1} < T_H + T_{JI,2} + \delta$$

Calculate the minimum clock speed for the following scenarios.

a) Skew time = 0.075 ns, setup time = 1 ns, hold time = 1 ns, jitter time (assume all jitter times are equal) = 140 ps, logic delay (T_{LM}) = 10 ns, register propagation delay = 1 ns. Does the hold time meet the inequality given above? If it does not, calculate hold time value that minimally satisfies the inequality.

b) Skew time = 0.03125 ns, setup time = 1 ns, hold time = 1 ns, jitter time (assume all jitter times are equal) = 140 ps, logic delay (T_{LM}) = 10 ns, register propagation delay = 1 ns. Does the hold time meet the inequality given above? If it does not, calculate hold time value that minimally satisfies the inequality.

c) Skew time = 0.075 ns, setup time = 0.2 ns, hold time = 0.2 ns, jitter time (assume all jitter times are equal) = 140 ps, logic delay (T_{LM}) = 10 ns, register propagation delay = 1 ns. Does the hold time meet the inequality given above? If it does not, calculate hold time value that minimally satisfies the inequality.

d) Skew time = 0.03125 ns, setup time = 0.2 ns, hold time = 0.2 ns, jitter time (assume all jitter times are equal) = 140 ps, logic delay (T_{LM}) = 10 ns, register propagation delay = 1 ns. Does the hold time meet the inequality given above? If it does not, calculate hold time value that minimally satisfies the inequality.

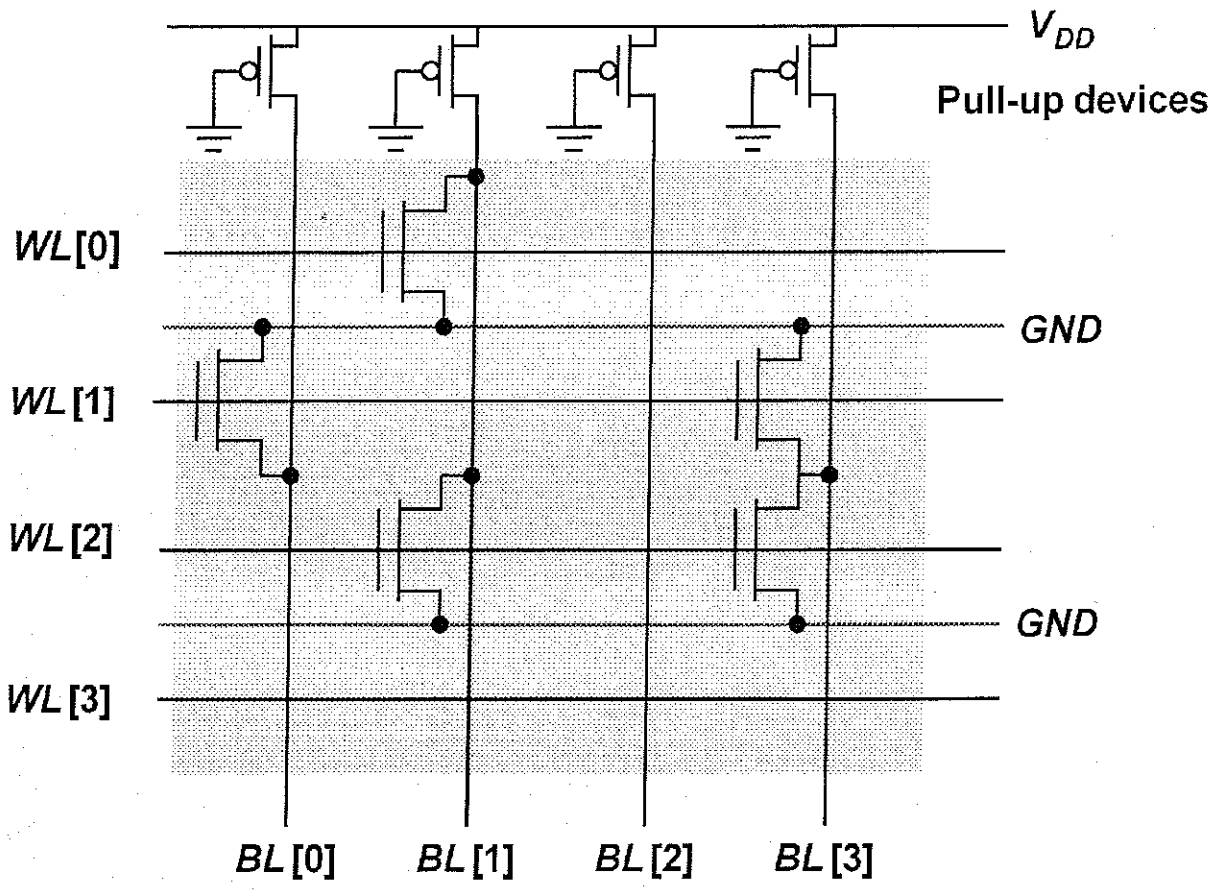
e) Skew time = 0.075 ns, setup time = 0.2 ns, hold time = 0.2 ns, jitter time (assume all jitter times are equal) = 140 ps, logic delay (T_{LM}) = 1 ns, register propagation delay = 0.1 ns. Does the hold time meet the inequality given above? If it does not, calculate hold time value that minimally satisfies the inequality.

f) Skew time = 0.03125 ns, setup time = 0.2 ns, hold time = 0.2 ns, jitter time (assume all jitter times are equal) = 140 ps, logic delay (T_{LM}) = 1 ns, register propagation delay = 0.1 ns. Does the hold time meet the inequality given above? If it does not, calculate hold time value that minimally satisfies the inequality.

g) In each of the above scenarios, identify the parameter that most affects the clock speed.

Question 5 (4 + 3 = 7 Marks)

The NOR ROM circuit is given below.



a) Determine the values in the data stored in locations 0, 1, 2, and 3 in the ROM.

b) Determine maximum and non-zero minimum static power dissipation in this ROM for standby current of 0.21 mA and an output voltage of 2.5V.

Question 6 (2 + 1 + 1 + 2 + 3 + 1 = 10 Marks)

a) Draw a labeled diagram of a cascode current mirror.

b) What is the main advantage of a differential mode amplifier?

c) Name three capacitances that affect high frequency performance of an amplifier.

d) Name five major performance characteristics of an amplifier.

e) Briefly describe the two major noise types. Identify environment parameters, transistor parameters, and circuit parameters that affect these noise types. Also indicate whether the noise value increases or decreases as these parameters increase.

f) List four impacts of having feedback in circuits.

Useful Formula and Information

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

$$\frac{(W/L)_p}{(W/L)_n} = \frac{k_n' V_{DSatn}\left(V_M - V_{Tn} - V_{DSatn}/2\right)}{k_p' V_{DSatp}\left(V_{DD} - V_M - V_{Tp} V_{DSatp}/2\right)}$$

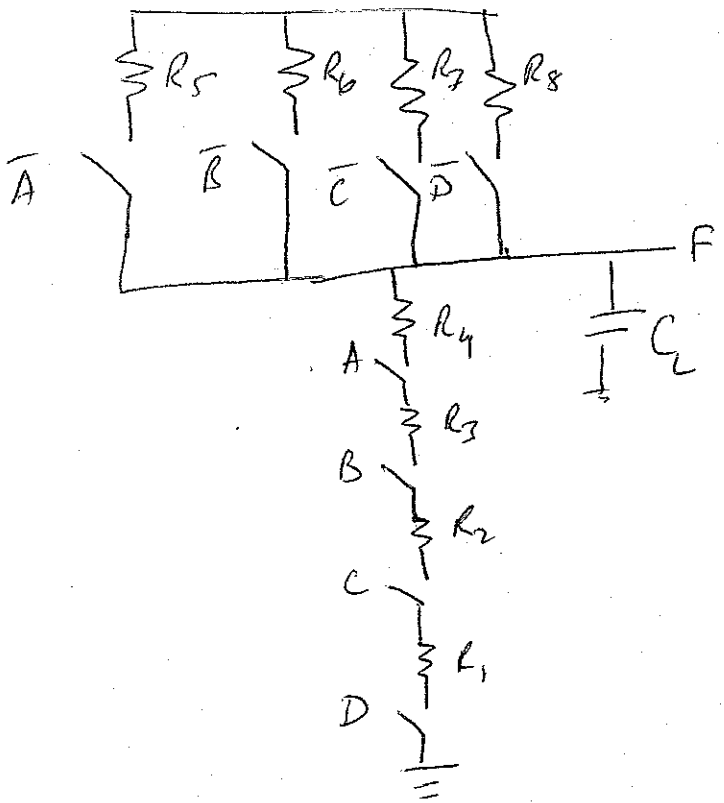
$K_n' = 115 \times 10^{-6}$ $V_{DSatn} = 0.63$

$K_p' = 30 \times 10^{-6}$ $V_{DSatp} = 1$

$V_{Tn} = 0.43$ $V_{Tp} = -0.4$

Delay = $0.69 R_{eq} C_L$

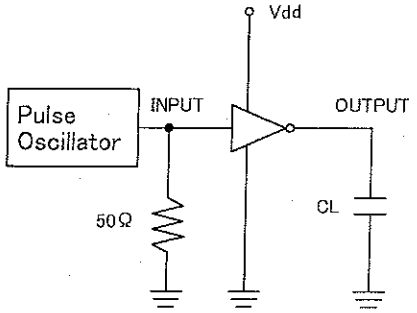
RC Model for 4-input NAND gate



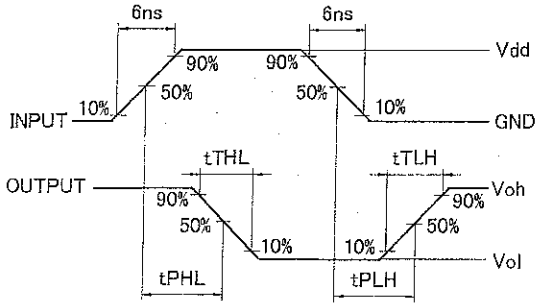
■DC electrical characteristics

Parameter	Sym.	Vdd	Top=25°C			Top=-40 to +85°C		Unit	Condition	
			Min.	Typ.	Max.	Min.	Max.			
Input voltage	Vih	2.0	1.50			1.50		V		
		4.5	3.15			3.15				
		6.0	4.20			4.20				
	Vil	2.0			0.50		0.50	V		
		4.5			1.35		1.35			
		6.0			1.80		1.80			
Output voltage	Voh	2.0	1.90	2.00		1.90		V	Vin=Vil	Ioh=-20μA
		4.5	4.40	4.50		4.40				
		6.0	5.90	6.00		5.90				
		4.5	4.18	4.35		4.13				Ioh=-2mA
		6.0	5.68	5.83		5.63				Ioh=-2.6mA
	Vol	2.0		0.00	0.10		0.10	V	Vin=Vih	Iol=20μA
		4.5		0.00	0.10		0.10			
		6.0		0.00	0.10		0.10			
		4.5		0.12	0.26		0.33			Iol=2mA
		6.0		0.13	0.26		0.33			Iol=2.6mA
Input current	Iin	6.0	-0.1		0.1	-1.0	1.0	μA	Vin=Vdd or GND	
Static current	Idd	6.0			1.0		10.0	μA	Vin=Vdd or GND	

■Test circuit



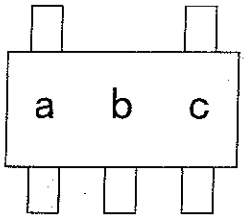
■Measured wave pattern



* Output should be opened when measuring current consumption.

■Marking

SOT-25



No.	Mark	Content
a	E	ELM7S series
b	5	ELM7S04B
c	A to Z (except I, O, X)	Lot No.

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International Academic City, Dubai

Second Semester 2010 – 2011

Analog and Digital VLSI Design EEE C443 (IV year)

Test 2 (Open Book)

No. of Questions : 4

No. of Pages : 2

Duration: 50 minutes **Weightage: 20%**

17 April 2010 **MAX: 20 Marks**

Note: Show all working to get full credit.

Question 1 (5 Marks)

A cascode current mirror is to operate with $I_{REF,\,max}$ = 100 µA. Based on the expression below for the maximum reference current, design this current mirror for 0.5 micron technology.

$$I_{REF,max} = \frac{\mu_n C_{OX}}{2} \frac{(V_{DD} - 0.5V - V_{TH0} - V_{TH1})^2}{\left(\sqrt{\left(\frac{L}{W}\right)_0} + \sqrt{\left(\frac{L}{W}\right)_1}\right)^2}$$

State all values in design and justifying design assumptions and decisions where necessary.

Question 2 (3 + 2 + 1 = 6 Marks)

1) Determine the output resistance, voltage gain, and CMRR for a differential pair with active current mirror. Assume the following parameters

   $g_{m1} = g_{m2} = g_{m3}$ = 0.5mA/V

   $r_{o1} = r_{o2}$ = 400KΩ

   $r_{03} = r_{04}$ = 240 KΩ

   I_{SS} = 100 µA

   V_{SS} = 0.5 V

2) What is the impact on the design of changing I_{SS}?
3) What is the impact on CMRR if
   a. g_{m1} = 0.5 mA/V and g_{m2} = 0.25 mA/V with all other parameters remaining unchanged?
   b. Compare this result with the result in part (1) of question.

Question 3 (1 + 2 + 1 = 4 Marks)

For 0.35 micron technology, the following values are given for a Common Source Amplifier:

$g_m = 10^{-4}$ A/V C_{GS} = 1.1fF C_{GD} = 0.2fF C_{DB} = 0.7fF R_D = 10 KΩ f = 1 MHz

1) ***Without*** obtaining the expression for $|A_V|$, would you expect the gain to be higher for R_S = 600 Ω or R_S = 0 K Ω?
2) Determine the condition under which the gain varies inversely with frequency i.e., as 1/f.
3) For the question in part (2), what is the frequency categorized – HF, VHF, …?

Question 4 (3 + 2 = 5 Marks)

Assume that $V_{in} = 5\cos(\omega_0 t)$ with f_0 = 1 KHz is the input to a Common Source transistor. The following parameter values are given:

K (Boltzmann's constant) = 1.38 x 10^{-23} J/K T = 300°K g_m = 0.1 mA/V R_D = 10 KΩ W = 0.7 μm

L = 0.35 μm C_{OX} = 0.54275 x 10^{-2} F/m^2 K = 1.06 x 10^{-25} V^2/F

1) Compute the output noise (consider thermal and flicker noise) voltage per unit bandwidth (V^2/Hz).
2) Compute the total output noise between 900 Hz and 1100 Hz.

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Analog and Digital VLSI Design EEE C443 (IV year)

Test 1 (Closed Book)

No. of Questions : 2
No. of Pages : 2

Duration: 50 minutes **Weightage: 25%**

27 February 2010 **MAX: 25 Marks**

Note: Show all working to get full credit.

Question 1 (Total Marks: 14)

Part 1-1: Design I (Gate-based Design of **A XOR B**) **(0.5 + 1 + 1.5 + 1 Marks)**

1. Write down the algebraic expression for the Exclusive OR function (**A XOR B**).
2. Design and draw **A XOR B** in terms of inverters, AND, and OR gates.
3. Design and draw the PMOS and NMOS transistor-based inverter, AND and OR Gates.
4. What is the total number of PMOS and NMOS transistors needed to implement this gate-based design for **A XOR B**?

Part 1-2: Design II (Direct translation of **A XOR B** functionality into transistor schematic) (4 Marks) **(3 + 1 Marks)**

1. Design and draw the **A XOR B** logic directly in transistor schematic using PMOS and NMOS transistors.
2. How many transistors are required in this design? Justify your answer.

Part 1-3: Comparison of Designs **(1 + 1 + 1 + 1 Marks)**

1. Which design would result in lower power dissipation? Justify your answer.
2. Which design would result in smaller surface area? Justify your answer.
3. Which design would result in lower propagation delays? Justify your answer.
4. Which design approach would you take to implement **A XOR B** in the lab if **X OR B** ICs were *not* available?

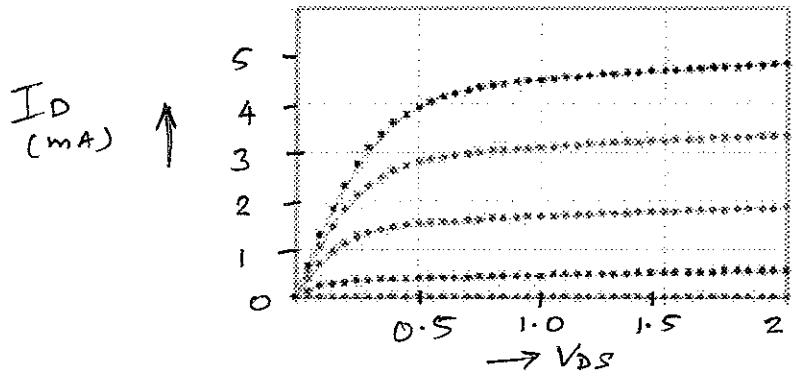
Part 1-4: Extension of Design to **A XOR B XOR C XOR D (2 Marks)**

Which quality metric in digital design would be most relevant in deciding whether to use 2-input, 3-input or 4-input OR or AND gates in the implementation? Justify your answer.

Question 2 (Total Marks: 11)

Part 2-1 (2 Marks)

Consider the following plot with the five curves corresponding to V_{GS} = 0.6 V (lowermost curve), 0.9 V, 1.2 V, 1.5 V, 1.8 V (topmost curve):



What would be your specification in terms of V_{DS} and V_{GS} for the following cases of drain current (I_D):

i. I_D is between 1 mA and 2 mA
ii. I_D is between 4 mA and 5 mA

Part 2-2 (6 + 3 Marks): The following data is given to you for NMOS transistors:

V_{DD}	Type of MOS	V_{TH}	t_{ox}	W/L	V_{GS}	V_{DS}
1.8 V	Low Power	0.6	$125x10^{-10}$ m	10/0.18	1.5 V	1.5 V
1.8 V	Standard	0.43	$125x10^{-10}$ m	10/0.18	1.5 V	1.5 V
1.8 V	Low Power	0.6	$125x10^{-10}$ m	10/0.5	1.5 V	1.5 V
3.3 V	Low Power	0.7	$60x10^{-10}$ m	10/0.18	3 V	2.7 V
3.3 V	Low Power	0.7	$60x10^{-10}$ m	10/0.35	3 V	2.7 V

Common information:

1) $I_{REF} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2(1+\lambda V_{DS})$

where $C_{OX} = \frac{k_{OX}\,\varepsilon_0}{t_{OX}}$ where $k_{OX} = 3.9, \varepsilon_0 = 8.85x10^{-12} F/m$

2) Assume λ = 0.1 and μ_n = 350. $cm^2\ N\text{-}S$.

Answer the following questions

i. Compute I_D for each of the five combinations of values in the above table.
ii. Compare and analyze the value of various drain currents obtained in (i).

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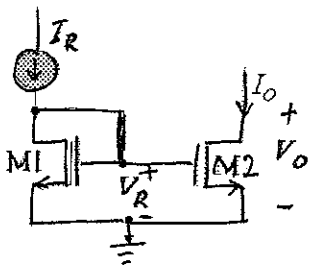
International Academic City, Dubai
Second Semester 2010 – 2011
Analog and Digital VLSI Design - EEE C443 (IV year)
Quiz 1 (Closed Book)

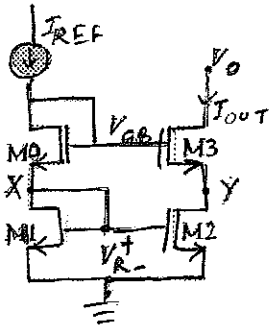
Duration: 20 minutes **Weightage: 8%**
21 March 2011 **MAX: 16 Marks**

Note: Show all working to get full credit.

Question 1 (1 + 1 = 2 Marks)

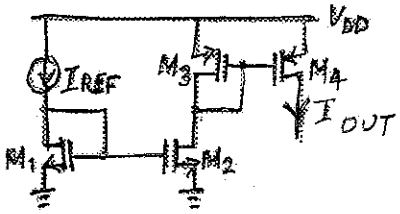
Identify and name the two current mirrors below.





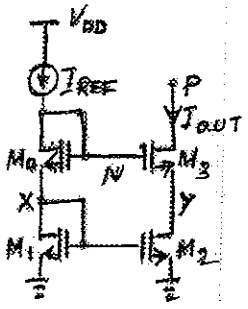
Question 2 (2 Marks)

Circle and name the major components of the circuit below.

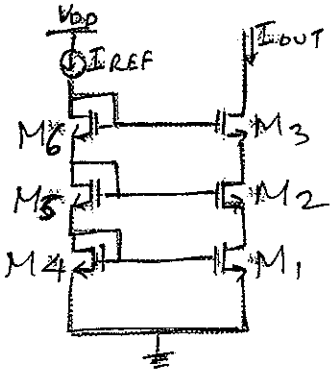


Question 3 (1 + 1 + 1 + 1 = 4 Marks)

Assume in circuits that all transistors are identical and $r_o = 5\ M\Omega$, $g_m r_o = 50$.

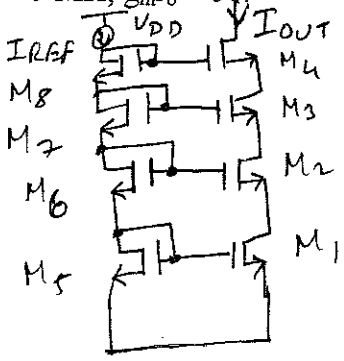


$R_o = r_o [1 + g_m r_o] + r_o$



$R_{o2} = r_o [1 + g_m r_o] + r_o$

$R_o = r_o [1 + g_m R_{o2}] + R_{o2}$

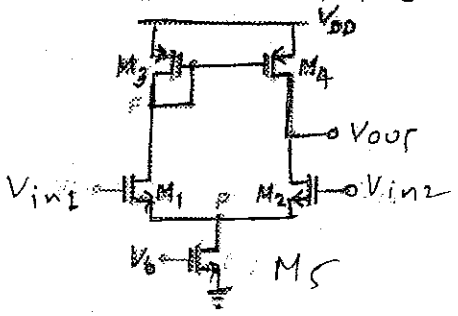


$R_o = ?$

1) Calculate R_o for the left-most circuit.
2) Calculate R_o for the middle circuit.
3) Extrapolate the expression for R_o for the right-most circuit.
4) Calculate R_o for the right-most circuit.

Question 4 (3 + 3 + 2 = 8 Marks)

For the circuit below, assume all transistors are identical. You are given
$R_{out} = r_o || r_o = r_o/2$; $|A_v| = g_m R_{out}$; CMRR = $(1 + 2\ g_m\ r_o)\ g_m\ r_o/2$.



1. Calculate R_{out}, $|A_v|$, and CMRR assuming $r_o = 5\ M\Omega$, $g_m = 10^{-5}$.
2. Calculate R_{out}, $|A_v|$, and CMRR assuming $r_o = 128\ K\Omega$, $g_m = 10^{-3}$.
3. On what basis would you make a design choice between the above two possibilities.