BITS PILANI – DUBAI CAMPUS

Knowledge Village, Dubai 2005-2006 Year IV – Semester II Comprehensive Examination (Closed Book)

Course No.: EEE UC 415

Course Title: DSP

Date: 31st May, 2006

Time: 3 Hours

Max. Marks = 40

(State clearly the assumptions made if any)

1. Design a digital butterworth filter satisfying the constraints

$$0.707 \le |H(e^{j\omega})| \le 1 \text{ for } 0 \le \omega \le \pi/2$$

 $|H(e^{j\omega})| \le 0.2 \text{ for } \sqrt[3]{4} \pi \le \omega \le \pi$

with T = 1 sec using bilinear transformation. Realise the filter using most (7)convenient realization form.

- 2.a.Derive the expression for finding the error variance due to quatisation and hence the variance of the output energy of a digital system
 - b. The A/D converter used in a digital system is 12 bit and the quantized signal is processed by a first order IIR digital filter whose transfer function is Find the steady state noise power due to given by H(z) = z / (z - 0.75). quantization that occur at the output of H(z).
- An FIR digital filter has impulse response h(n) defined over the interval $0 \le n \le N-1$. Show that if N=8 and h (n) satisfies the symmetry condition h(n) = h(N-n-1), the filter has a linear phase characteristics.
- 4. Consider an audio band signal sampled at a rate of 80 KHz. It is required to down rate the sampling frequency to 10 KHz. The highest frequency of interest after decimation is 2 KHz. Design a suitable optimum two stage decimator which will satisfy the following overall specifications.

Pass band ripple = 0.1;

Stop band ripple = 0.01

Filter length N = $\frac{-10 \log (\delta_s \delta_p) - 13}{1} + 1$;

 $14.6 \Delta f$

where Δf is the normalized frequency.

Draw also the frequency response of the designed decimator stages. (7)

Starting with the equation for the mean square error, derive the Wiener -Hopf equation to estimate the optimum weights of the adaptive filter. (4)

6.	With a neat block diagram, explain the internal architecture of							
	TMS	320 C 5X	Processors.				(4)	
7.	i)	The syn	nbol used to	indicate th	e immed	iate address	mode for the	
		a) \$	b) *	c)#	d) &	e) %		
	ii)	The	data memory pages	used wis each of _	th C5X	processors vords long.	is split into	
		a) 512, 1	28 b) 2	56,256	c) 12	8,512	d) 1024,64	
iii) The register in which the result of multiplication and its bit wide.						on is stored is		
	a) PREG, 32 b) PREG, 16 c) TREG0,16 d) TRE							
	iv)	The status register bit that determines whether multiplier's 32-bit product is left shifted by 0,1,4 or right shifted by 6 with sign extension before it is transferred / added to the ACC is						
		a) CNF	b) PM	c) HM	d) XF	e) IN	TM	
	v) Assume that the contents of ACC, ARP, AR3, and locations 0045 40C5H are 1000H, 3, 40C5H, 2400 H and 2300H respective initially. When the instruction LAMM * is executed, the content ACC is							
		a) 2400H	b) 2300H	c)	40C5H	d) 0003H		
							(1x5)	

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BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai Year IV – Semester II 2005–2006 Test II (Open Book)

Course No.: EEE UC 415

Date:

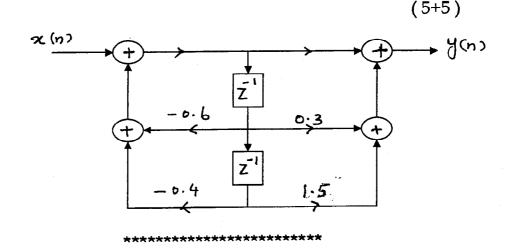
Course Title: DSP

Time: 50 Minutes

Max. Marks = 30

(Only Text Book & class Notes are Allowed)

- A 4-point linear phase FIR filter is characterized by the following frequency samples. | H (k) | = 1, k = 0 = ½, k = 1, 3 = 0, k = 2
 - a) Determine the transfer function of the Recursive FIR frequency sampling filter and show that it contains four zeroes and three poles.
 - b) Sketch the pole -zero diagram
 - c) Determine the four coefficients of the filter which could be implemented. (4 x 3)
- 2. Determine the frequency response of the FIR filter defined by y(n) = 0.25 x(n) + x(n-1) + 0.25 x(n-2). Calculate the phase delay and Group delay. (4 + 4))
- 3. Scale the second order digital filter structure shown in figure below using the L_2 norm- scaling rule. Also find the total steady state output noise power caused by round off errors.



BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai Year IV – Semester II 2005–2006 Quiz I (Closed Book)

Course No.: EEE UC 415 Course Title: DSP

Date: March 14, 2006 Time: 50 Minutes Max. Marks = 24

(Question nos. 1-10 carries one mark each and Question Nos 11-17 carries 2 marks each)

- 1. A digital Filter is said to be IIR if
 - a.) All its pole lie outside the unit circle
 - b.) One or more denominator coefficients is non zero
 - c.) Current output depends on previous output
 - d.) It oscillates
- 2. For the same filter specifications the order of FIR filter can be as high as 5 to 10 times that of IIR filter. (True / False)
- 3. To do the spectrum analysis of an analog signal of frequency 500 Hz, it is sampled to produce 1024 data values. What is its frequency spacing between spectral samples
- 4. Draw the impulse response of an ideal low pass filter
- 5. What is the principle of designing optimum FIR filter?
- 6. For what type of filters frequency sampling method is suitable?
- 7. An Analog band pass signal is to be sampled in accordance with the band pass sampling theorem. Assuming the signal has the frequency band of 28 kHz 64 kHz, what should be the minimum theoretical sampling rate to avoid aliasing?
- 8. What are the properties that are maintained same in the transfer of analog filter into a digital filter?
- 9. Distinguish between Butterworth and Chebyshev (Type-I) filters.
- 10. Write a Bilinear transform equation between s-plane and z-plane, which is used for digital filter design.
- 11. A Discrete filter has poles at z = +j0.6 and -j0.6 and zeroes at z = -0.8 and at z = +0.8What is the amplitude response of the filter at $1/4^{th}$ of its sampling frequency?
- 12. A discrete time filter transfer function is given by

 $H(z) = (1 - 1.6 z^{-1} + z^{-2}) / (1 - 1.5 z^{-1} + 0.8 z^{-2})$ What is its DC amplitude response?

- 13. For the system transfer function given in question no.12, What are the radii of the poles and zeroes?
- 14. Obtain the digital filter transfer function of the analog filter with H(s) = 1/(s + 1), by Impulse Invariant method.
- 15. Under what conditions a finite duration sequence h(n) will yield constant group delay in its frequency response characteristics and not the phase delay?
- 16. State the condition for a digital filter to be causal and stable.
- 17. Draw the canonic form realization of the transfer function given in question No. 12

BITS, PILANI - DUBALCAMPUS

Knowledge Village, Dubal Year IV – Semester II 2005–2006 Test I (Closed Book)

Course No.: EEE UC 415

Course Title: DSP

Date: February 22, 2006

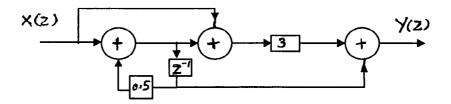
Time: 50 Minutes

Max. Marks = 40

(Answer all the questions)

- 1. Design an analog low pass Butterworth filter that has a pass band attenuation of 2dB at a frequency of 20 rad/sec and at least 10 dB stop band attenuation at a frequency of 30 rad/sec. (10 M)
- 2. For the digital system shown in figure below,
 - a) Determine the transfer function
 - b) Determine the poles and zeroes of the system
 - c) Realize the transfer function using Direct form II
 - d) Realize the transfer function in the parallel form

(5Mx4)



- 3. A causal discrete time system has a pole at z = 0.707 and a zero at z = -1.
 - a) Determine the transfer function of the system.
 - b) Draw the pole zero diagram
 - c) Determine the frequency response (Amplitude & Phase) of the system and plot for a complete cycle of sampling frequency. (10)

Table 7.1 Butterworth Polynomials

n	Polynomial					
1	(s+1)					
2	$(s^2 + 1.414s + 1)$					
3	$(s+1)(s^2+s+1)$					
4	$(s^2 + 0.7654s + 1) (s^2 + 1.8478s + 1)$					
5	$(s+1)(s^2+0.6180s+1)(s^2+1.6180s+1)$					
6	$(s^2 + 0.5176s + 1) (s^2 + 1.4142s + 1) (s^2 + 1.939s + 1)$					