BITS, PILANI – DUBAI CAMPUS

Accademic City, Dubai
Year IV – Semester I 2007 – 2008
Test I (Closed Book)

Course No.: **EEE UC 415** Course Title: **DSP**

Date: October 28, 2007 Time: 50min. Max. Marks = 30

(Any assumptions made should be indicated clearly)
[Windows table given at the back]

1. Determine the frequency response of FIR filter defined by
   $y(n) = 0.25\,x(n) + x(n-1) + 0.5\,x(n-2)$.
   Calculate the phase delay and group delay. (7)

2. a) What is the most general form of IIR filter representation? (2)

   b) Design a digital butterworth filter satisfying the following specifications

   $0.707 \le |H(e^{j\omega})| \le 1$ for $0 \le \omega \le \pi/2$

   $|H(e^{j\omega})| \le 0.25$ for $\frac{3}{4}\pi \le \omega \le \pi$

   with T = 1 sec using bilinear transformation. Realise the filter using direct form I. (7)

3. Design a linear phase digital FIR filter with the following frequency response specifications and a stop band attenuation >= 38 dB, using window method, with N=7 .

   $H_d(\omega) = e^{-j3\omega}$ for $-\pi/4 \le \omega \le \pi/4$

   $H_d(\omega) = 0$ for $\pi/4 \le \omega \le \pi$ (7)

4. By pole-zero placement method, obtain the transfer function and the difference equation of a simple digital notch filter that meets the following specifications.

   Notch frequency : 40 Hz ; 3 dB width of notch : +/- 5 Hz

   Sampling frequency : 320 Hz (7)

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BITS, PILANI – DUBAI

Dubai Academic City, Dubai

Year IV – Semester I 2007 – 2008

TEST II (OPEN Book)

Course No.: **EEE UC 415** Course Title: **DSP**

Date: December 09, 2007 Time: 50 minutes. Max. Marks = 30

(Any assumptions made should be indicated clearly.
Text book / Reference book with hand written notes are allowed)

1. Obtain the FIR linear phase and cascade realizations of the system function

   $H(z) = (1+ z^{-1} / 2 + z^{-2})(1+ z^{-1} / 4 + z^{-2})$ (10)

2. Two first order digital filters whose functions are given below are cascaded together to derive the output.

   $H_1 = 1 / (1- 0.9 z^{-1})$ $H_2 = 1/ (1- 0.8 z^{-1})$

   Determine the overall noise power contained in the output if the filter uses 8-bit ADC (10 M)

3. Design an optimum two-stage decimator for the following specifications

   Sampling rate of the input signal = 20,000 Hz
   the required sampling frequency is 500Hz.
   Pass band = 0 to 40 Hz
   ~~Transition band = 40 to 50 Hz~~
   Pass band ripple = 0.01
   Stop band ripple = 0.002
   Also draw the frequency response. (10 M)

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BITS PILANI – DUBAI

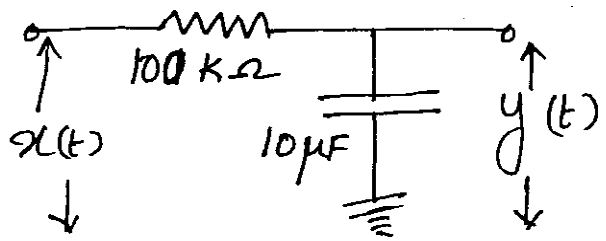
Dubai International Academic City
Year IV – Semester I 2007– 2008
Comprehensive Examination (Closed Book)

Course No.: **EEE UC 415** Course Title: **DSP**

Date: 07th January, 2008 Time: 3 Hours Max. Marks = 40

(State clearly the assumptions made if any)

1. Using Bilinear – Z transform method of designing digital filters, determine the transfer function and hence the difference equation for the digital equivalent of the Resistance - Capacitance filter shown in figure below. Assume a sampling frequency of 150 Hz and a cut off frequency of 30 Hz. (7)



2. A digital filter is characterized by the following transfer function.

$H(z) = (1 + 1.5947\, z^{-1} + z^{-2}) / (1 - 0.6152\, z^{-1} + 0.2581\, z^{-2})$

The filter is to be implemented using an 8bit system. Assuming that a second order canonic section is used to realize the filter, and each product has to be quantized to 8 bit,

a) Sketch the realization diagram showing the round of errors with in the filter

b) Determine the $\mathcal{L}_2$- norm scaling factor for the system. (4+4)

3. An FIR digital filter has impulse response h(n) defined over the interval $\mathbf{0 \le n \le N-1}$. Show that, if **N=6** and h (n) satisfies the symmetry condition $\mathbf{h(n) = h(N - n - 1)}$, the filter has a linear phase characteristics. (5)

4. Consider an audio band signal sampled at a rate of 80 KHz. It is required to down rate the sampling frequency to 10 KHz. The highest frequency of interest after decimation is 2 KHz. Design a suitable optimum two stage decimator which will satisfy the following overall specifications.
Pass band ripple = 0.1; Stop band ripple = 0.01

(Contd...

Filter length $N = \frac{-10 \log(\delta_s \delta_p) - 13}{14.6 \Delta f} + 1$;

where Δf is the normalized frequency.

Draw also the frequency response of the designed decimator stages. (7)

5. Starting with the equation for the **mean square error**, derive the Wiener – Hopf equation to estimate the optimum weights of the adaptive filter. (4)

6. With a neat block diagram, explain the internal architecture of **TMS 320 C 5X** Processors. (4)

7. i) The symbol used to indicate the immediate address mode for the operand is _____

a) $ b) * c) # d) & e) %

ii) VLIW architecture differs from conventional P-DSP in which of the following aspect?
a) Instruction Cache b) Number of functional Units
c) Use pipelining
d) A single word fetch from memory using many instructions.

iii) The status register bit that determines whether multiplier's 32-bit product is left shifted by 0,1,4 or right shifted by 6 with sign extension before it is transferred / added to the ACC is _____

a) CNF b) PM c) HM d) XF e) INTM

iv) The addressing mode that is convenient for FFT computation is
a) indirect addressing b) circular mode
c) Bit reversed addressing d) Memory mapped

v) Assume that the contents of ACC, ARP, AR3, and locations 0045H, 40C5H are 1000H, 3, 40C5H , 2400 H and 2300H respectively initially. When the instruction LAMM * is executed, the content of ACC is _____

a) 2400H b) 2300H c) 40C5H d) 0003H

(1x5)

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