BITS Pilani - Dubai Campus
Knowledge Village, Dubai
I – Semester 2005-2006

Number of Pages: 2

Number of Questions: 14

Course Number	:	CS UC 444
Course Name	:	Real-Time Systems
Nature of Component	:	**Comprehensive Examination**
Weightage	:	40%
Max. Marks	:	40 Marks
Duration	:	180 minutes
Date of Examination	:	02.01.2006

Note: 1) Please follow all the instructions to candidates given on the cover page of the answer book.
2) All parts of the question should be answered consecutively. Each answer should start from a fresh page.

1. Show the Moore Finite State Automata for a system that scans for the bit sequence 01111110 in a string of bits (the sequence is allowed to appear anywhere in a bit string). This bit sequence is standardly used to denote packets boundaries in serial communications. (3 marks)
2. Why is it important for a real-time system to have a watchdog timer? Is a timer interrupting routine an appropriate point in the software to reset the watchdog timer, why or why not? (3 marks)
3. Give Petri Net's design for a Model communication protocol between TWO processes. The design should consider the parameters like send message, send acknowledge, wait acknowledge, wait acknowledge, receive acknowledge, buffer between the two process in order to avoid loss of information during communication, process 1 and process 2 and justify your design in order to implement it in the real world of application. (4 marks)
4. Consider the following four fixed priority tasks:T1 = (3,1), T2 = (5,1.5), T3 = (7, 1.25), T4 = (9,0.5). Give the time –demand function $w_4(t)$ of T4 and also give the time-demand analysis for the above sets of tasks. (4 marks)
5. Consider there are three tasks T1, T2, T3, their Runtime are 3,6,8; and their periods are 9,18,36; check whether the given tasks are Harmonic or not, and also calculate the total utilization and assign priority for the tasks, clearly mention on what basis the priorities are assigned to the tasks. (3 marks)
6. Give the formula to calculate the number of jobs in each hyper period. (1 mark)
7. Give the difference between the priority-inheritance and priority-ceiling protocol. (3 mark)
8. Mention the difference between Dynamic systems and static systems. (2 marks)

9. Find the Hyper period and frame size using the three frame size constraints for the given set of task as shown below: (3 marks)

Task τi	Period pi	Deadline Di	Run-Time Ci
$\tau 1$	4	4	1
$\tau 2$	5	5	1.8
$\tau 3$	20	20	1
$\tau 4$	20	20	2

10. Check whether the task T3 is schedulable are not? Calculate the total utilization, also assign priorities to the tasks and mention on what basis the priorities are assigned. (4 marks)

Task	pi (ms)	ei (ms)	priority	Blocking	Deadline
T1	100	40	?	0	100
T2	150	50	?	0	150
T3	400	70	?	0	270

11. Write short note on Deferred Server? (3 marks)

12. Give the 0-address machine, 1-address machine, 2-address machine and 3-address machine coding for the expression given below: $a = (b + c) * d - e$ (3 marks)

13. For a given set of tasks to a processor, and their deadlines & release times are same, under this condition what will be the algorithm used for the assigning the priorities to the tasks in order to schedule tasks for execution? (1 marks)

14. Consider a payroll processing systems for a small manufacturing firm. Describe three different scenarios in which the system can be justified as hard, firm, or soft real-time. (3 marks)

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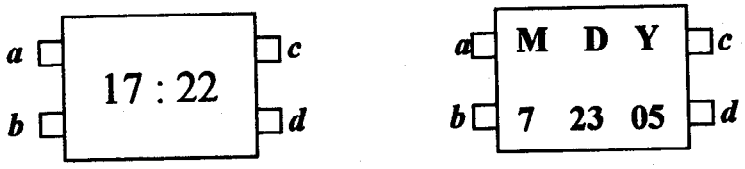
BITS Pilani - Dubai Campus
Knowledge Village, Dubai
I – Semester 2005-2006

Course Number	:	CS UC 444
Course Name	:	Real-Time Systems
Nature of Component	:	**Open Book**
Weightage	:	20%
Duration	:	50 minutes
Date of Examination	:	13.11.2005

Note: 1) Please follow all the instructions to candidates given on the cover page of the answer book.
2) All parts of the question should be answered consecutively. Each answer should start from a fresh page.

1. Design a Finite State Machine for the following problem definition: Consider the behavior and associated events of a gate at a train crossing. Suppose that there is a road crossing railway track, and a gate that opens and closes over the road. When a train approaches the crossing, the gate should close. More than one train can be crossing area at once, for example, a convoy of trains, each with a single engine and no cars. When the last train has left and the area is empty of trains, the gate should open. The gate could be in one of four states: **open, closed, opening,** and **closing**. The relevant events are: **cg** and **og** which are commands to close and open the gate, respectively; and **o-o** and **c-c** indicating from sensor input that the gate has completed opening (and thus changed from the opening to the opened state), and that the gate has completed closing, respectively. The initial state is closed and there are no stop states. The Finite state machine accepts the **cg** and **og** commands in all its states; thus, for example, the gate may be commanded to close while it is opening. (5 marks)
2. Give the real-time design for the digital watch given below using *state chart design* methodology: the problem definition for the digital watch design is as follow: the design must contain the three modes and their interactions. The three different modes are ***Normal_Display mode, Update mode, and Chime_Alarm_set mode.*** There are four buttons in the digital watch as ***a, b, c, d,*** input events caused by pressing one of four buttons, and are represented on the transitions by the button identifiers. There are four buttons ***a, b, c, d,*** in the digital watch, while pressing the button ***a*** in ***Normal_Display*** there is change of state due to transition from ***time state*** to ***date state*** and back from ***date state*** to ***time state,*** and if you press the button ***c*** in ***Normal_Display*** there occurs a state transition to ***Update state.*** The ***Update state*** is also called as a super state, since it has its own set of states like ***minutes, hour, day, month, year*** with its transition variables as b/m_{60}, b/h_{24}, b/D_{31}, b/M_{12}, b/Y_{100}. If you are pressing the button ***a*** while in any state inside ***Update*** superstate, there occurs the state transition within the states ***minute, hour, day, year.*** Once the transition reaches the ***year state*** of the ***Update super state,*** if the user presses the button ***a*** then the transition takes back to the

Normal_Display. Upon pressing the button ***d*** while in any state inside ***Update***, a transition back to the entry state of ***Noraml_Display*** occurs. There occurs a state transition from ***Normal_Display*** to ***Chime_Alarm_Set*** by pressing the button ***b*** and ***Chime_Alarm_Set*** state has **two** internal states as ***Alarm*** and ***Chime*** while pressing the button ***a*** inside the ***Chime_Alarm_Set state*** there occurs state transition between ***Alarm state*** and ***Chime state.*** Upon pressing button ***d*** while in any state inside ***Chime_Alarm_set*** state, a transition back to the entry state of ***Normal_Display*** occurs. (8 marks)



3. Calculate the hyper period and frame size for the given set of task? (3 marks)

Ti	pi	ei	Di
T1	15	1	14
T2	20	2	26
T3	22	3	22

4. Consider a system that contains four independent periodic tasks and their hyper period is 20, they are T_1=(4,1), T_2=(5,1.8), T_3=(20,1), and T_4=(20,2). The cyclic schedules of these periodic tasks are as follows: T_1 starts execution at time 0, 4, 9.8, 13.8, 16, and so on; T_2 starts execution at 2, 8, 12, 18, and so on; T_3 starts execution at 1 and so on; T_4 starts execution 6, and so on. Draw the timing diagram for the above problem definition using one processor. Three aperiodic jobs A_1, A_2, and A_3; their release times are immediately before 4, 10, and 14, and their execution times are 1.5, 0.5 and 2 respectively. Use slack stealing scheme improve the response times of aperiodic jobs by executing them ahead of the periodic jobs. Show the above problem definition using the timing diagram illustrating slack stealing process. (4 marks)

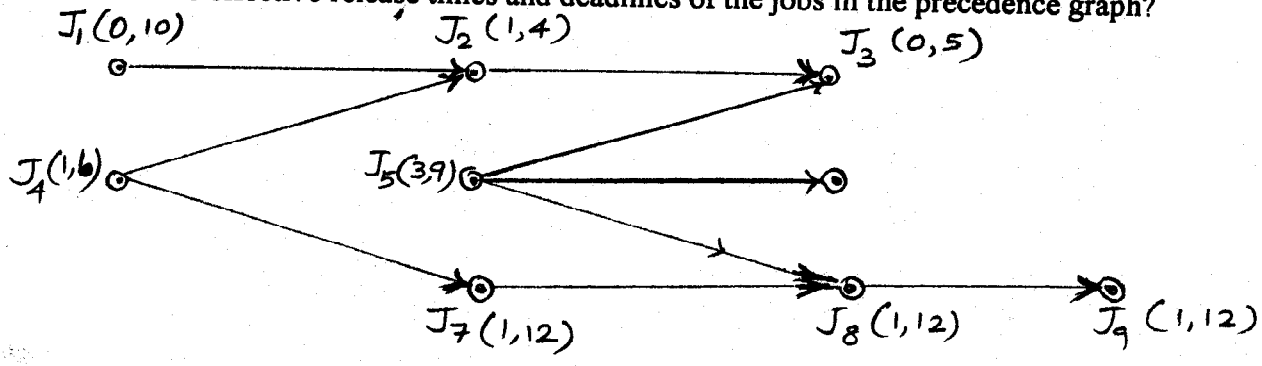
BITS, Pilani – Dubai Campus
Knowledge Village, Dubai
First Semester 2004 – 2005
Test - I

Real-Time Systems CS UC 444
Weightage: 20%
Max. Marks: 20

Date: **25.09.2005**
Time: 50mins
Closed Book

Note: All questions are compulsory. Write any assumption made with its requirement. Symbols have usual meaning.

1. What is major constraint that distinguishes Real-Time System from Non-Real-Time System? (1)
2. Under what condition, we will choose the Latest Release Time Algorithm to produce a feasible schedule. (2)
3. Give the definition of relative deadline and absolute deadline. (1)
4. Consider a real time weapon control system aboard an aircraft. Discuss (provide a brief explanation) which of the following events would be considered synchronous and which would be considered asynchronous to the software: (2)
   a. A signal indicating the pilot has pressed the "fire rocket" button.
   b. A divide-by-zero error.
   c. A 10-millisecond clock interrupt.
   d. A built-in software failure.
5. Why is DMA controller access to main memory in most systems given higher priority than CPU access to main memory? (1)
6. A job is said to be at level i if the length of the longest path from the job to jobs that have no successors is i. So, jobs j3, j6, and j9 are at level 0, jobs j2, j5, and j8 are at level 1, and so on. Suppose that the priorities of the jobs are assigned based on their levels: the higher the level, the higher the priority. The execution times of all jobs are equal to 1. (6)
   a. Find a priority-driven schedule of the jobs in figure given below, according to this priority assignment and check whether the jobs misses their deadline or not?
   b. Find the effective release times and deadlines of the jobs in the precedence graph?



7. What was the algorithm used for scheduling real-time traffic in high-speed switched networks. Justify your answer related to the problem. (3)
8. Describe the relationship between the main processor and co-processor in a system with which you are familiar. (2)
9. Assign an algorithm for a set of jobs that fix priorities to jobs based on their deadlines and this algorithm is optimal when it used to schedule jobs on a processor as long as preemption is allowed and jobs do not contend for resources. (2)

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Knowledge Village, Dubai
First Semester 2004 – 2005
Test - I

Real-Time Systems CS UC 444
Weightage: 20%
Max. Marks: 20

Date: **Makeup**
Time: 50mins
Closed Book

Note: All questions are compulsory. Write any assumption made with its requirement. Symbols have usual meaning.

1. Classify the given system/task as Hard or Soft Real-time systems/task.
   a. In multimedia application, frames of video should send at a rate of 80 frames/sec.
   b. Interactive Database system for Air traffic control.
   c. Power supply frequency controller that maintains frequency at (500) Hz, at power generating station.
   d. Car engine management system.
   e. Autopilot system for aircraft navigation
   f. Virtual Reality environment computer game.
   g. Automatic cash dispensing machine.
   h. Interactive BITS database of student information. (4)
2. Compare advantages of RISC and CISC processor types for embedded Real-time system applications. (4)
3. Draw the precedence graph for the following description of jobs assigned to two processors, here jobs J_1, J_2, J_3, J_4, J_6, J_7, J_8 are released at time 0, and only job J_5 is released at time 5, their execution time are given next to the job number. J_1, 3 is independent job and it does not have any successor. Job J_2, 1 has successors has job named J_3, 2 and its successor is J_4, 2. Similarly job J_5, 2 its successor has J_6, 4 and job J_7 4 its successor has J_8 1. Show the scheduling of jobs using Gantt chart or timing diagram under preemption and non-preemption conditions. (4)
4. Explain the usage of MUX Transceivers with a block diagram and also show the bus structure represented by Mil-Std-1553B as a transmission and receipt protocol. (3)
5. Explain the anomalous behavior of priority-driven systems and prove the anomalous behavior based the job table given below. The table shows FOUR different independent jobs and they are scheduled to TWO identical processor in a priority manner. Draw the timing diagram shows the scheduling sequences of the given jobs. (4)

	r_i	d_i	$[e_i^-$ $e_i^+]$
Job 1	1	12	7
Job 2	0	15	8
Job 3	0	12	[3, 5]
Job 4	2	18	12

6. Define and explain Dynamic and Static systems? (1)

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BITS Pilani - Dubai Campus
Knowledge Village, Dubai.
Quiz – I
I – Semester 2005-2006

A

CS UC 444 – Real –Time Systems Max. Marks: 10 Date: 25.10.2005

Name:_____ ID. No.:_____

1. An Expression _____ denotes the difference between the desired state and the measured state at time t, of an analog single-input / single output PID controller.
2. In a Radar signal processing & tracking system, the amount of frequency shift is proportional to the velocity of the object. The frequency shift is other wise called _____.
3. The gating process tentatively assigned to one or more established trajectory if it is within a _____ distance away from the predicted current position and velocity of the object moving along the trajectory.
4. Give one of the algorithms used as data association process _____.
5. A real-time database contains data objects, called _____ that represent real-world objects.
6. The _____ of a job is the instant of time by which its execution is required to be completed.
7. On-Line Transaction Systems have _____ deadline and is a _____ real-time systems.
8. The release times of jobs are not known until the event triggering them occurs. These jobs are called _____ or _____ because they are released at random instant of time.
9. The execution time of a job Ji is the range _____, where _____ and _____ are the minimum and maximum execution time of Ji .
10. A task is _____ if the jobs in it have either soft deadlines or no deadlines.

11. The _____ algorithm has been used for scheduling real-time traffic in high speed switched networks.

a) EDF b) LRT c) LST d) Weighted Round Robin

12. One way to implement a scheduler that makes scheduling decision periodically in time-driven approach of scheduling is to use a _____.

a) Fixed slice driven, b)hardware timer, c) soft system, d) none of the above.

13. What is the other name for the priority approach is _____.

a) First-In-First-Out, b) Time slice approach, c)event-driven, d)all of the above.

14. What is the algorithm which assigns priorities to jobs according to their release time's _____.

a) EDF, b) LST, c) LIFO, d) LRT

15. _____ memory uses a single transistor per bit.

a) EEPROM, b) PROM, c) UVROM, d) Flash.

16. In programmed I/O method, an _____ instruction will transfer data from a specified I/O device into a specified CPU register.

a) PUSH, b) POP, c) LOAD, d)IN.

17. Programmable Logic Arrays are sometimes called _____.

18. The enable priority interrupt is used to enable interrupts for processing by the _____.

a) CPU, b) memory-mapped, c) programmed IO, d) none of the above.

19. The DMA controller is responsible for assuring that only one device can place data on the bus at any time, this process is called _____.

20. A/D circuitry converts continuous signals into _____ ones.

a) linear, b) non-linear, c)discrete, d)none of the above.

BITS Pilani - Dubai Campus
Knowledge Village, Dubai.
Quiz – I
I – Semester 2005-2006

B

CS UC 444 – Real –Time Systems Max. Marks: 10 Date: 25.10.2005

Name:_____ ID. No.:_____

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