O/C Director's office

BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai

Year IV – Semester I 2004– 2005

Test I (Closed Book)

Course No.: INSTR UC 421 Course: Digital Systems

03 - 10 - 04 Time: 50 Minutes M.M. = 40 Weightage = 20 %

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1. An 8-bit DAC has a full scale output of 2mA and Full scale error of +/- 0. 5% F.S. What is the range of possible outputs for an input of 1000 0000 ? 10

2. With a neat schematic explain the principle of operation of a successive approximation type ADC. 10

3. Design a complete digital system which will display the decimal equivalent of ten bit binary input. (Hint : First convert the Binary input into equivalent BCD) 10

4. (a) Show the schematic of two dimensional ROM addressing of 1K x 8 memory 5
   (b) How will you achieve the above memory bank using 256 x 4 ROM ICs. Design the addressing scheme . 5

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Test II (Open Book)

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01 - 12 - 04 Time: 50 Minutes M.M. = 40 Weightage = 20 %

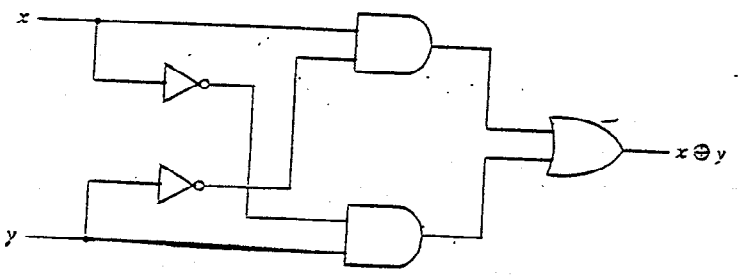
(Answer all questions. Part A have 5 questions each carrying 2marks and Part B have three questions each carrying ten marks)

Part A

1. Explain why a digital oscilloscope need to use fast ADCs?
2. Differentiate between dual beam and dual trace oscilloscopes. What are the merits of a dual beam oscilloscope?
3. Pulses of frequency of 10 MHz are applied to the time base selector of a digital circuit, which consists of 7 frequency dividers each diving the incoming frequency by a factor of 10. What is the time base setting at the 3rd and 6th frequency divisors?
4. What is a operation of the level detector used in the integrating type digital voltmeter? Draw a circuit which can be used as a level detector in an integrating type digital voltmeter.
5. What does GPIB or HPIB stands for? What are the handshake signals available in an IEEE – 488 Bus? Explain their functions.

Part B

1. Design a divide by twenty decade counter circuit which can be used along with a time base circuitry of a frequency counter and explain its operation.
2. The Ex-OR circuit of the figure shown below has gates with delay of 10ns for an inverter, 20 ns delay for an AND gate and 30ns delay for an OR gate. The input of the circuit goes from xy = 0 0 to xy = 0 1.



(a) With AND-OR-NOT gates

a) Determine the signals at the output of each gate from t = 0 to t = 50 ns.

b) Write the HDL description of the circuit including the delays.

c) Write a stimulus module for the part (a)

3. A digital counter timer frequency meter having a 4 digit display has gating periodic signal with periods of 1ms, 10ms, 100ms, 1s, and 10s. When a gating period of 100msec is used, a reading of 0143 is obtained.

   a) Find the likely frequency of the input signal

   b) What step should be taken to get most accurate result?

   c) Suppose the frequency of input signal is 5.307 kHz. Find the display for various gating signals.

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Year IV – Semester I 2004– 2005

Comprehensive Examination

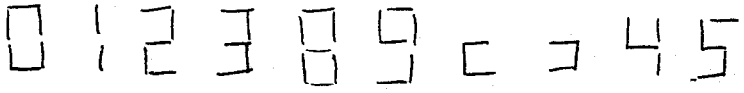
Course No.: INSTR UC 421 Course: Digital Systems

04 - 01 - 05 Time: 3hrs M.M. = 60 Weightage = 30 %

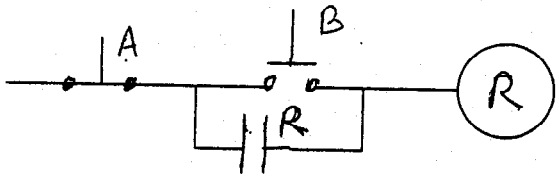
(Answer all questions. Part A have 10 questions each carrying 2marks and Part B have five questions each carrying eight marks)

Part A

1. A BCD to 7-segment decoder output is connected to a seven segment LED display. For the BCD inputs starting from 0000 to 1001 sequentially, the seven segment LED display obtained is as shown below. Analyse the output and trouble shoot the same.



2. Write the VHDL codes to generate a clock signal of frequency 1MHz
3. For the following ladder diagram, write the Boolean function



4. Draw the state diagram of a motor control circuit which has two start buttons and two stop buttons. (Assume that a single start or stop switch can also do the function)
5. Calculate the duration for which the data is to be available per digit of a set of 6 display devices connected at the output port of a computer so that the display will appear to be stable.
6. Write the control status word of an 8255 PPI to set the Port A as mode 0 input, the port B as mode1 output, Port C LSB as input and Port C upper as output
7. How many address lines will be there in a 2K x 8 ROM? Draw the two dimensional ROM array addressing.

Write short notes on any three of the following

8. FPGA's
9. Bus Interface Standards
10. Computer controlled systems
11. Flash Converters

Part B

1. Design a triangular waveform generator (with variable amplitude and frequency) using a binary counter and a DAC. Additional flip-flops or logic gates may be used if required. Explain the operation of the circuit. (8)

2. a) Design a J-K flip flop using D flip flop . (2)

   b) Write the HDL structural description of the J-K flip flop circuit in part a) (3)

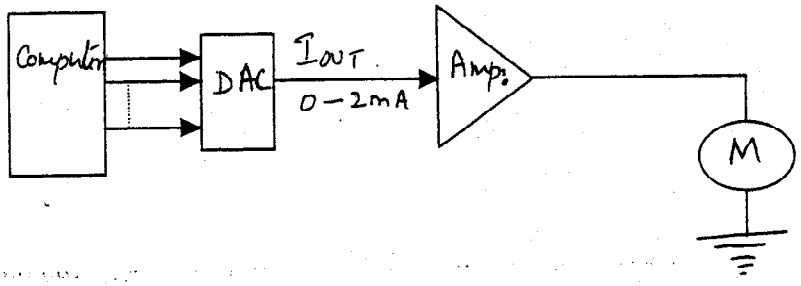
   c) Write a stimulus for testing the above HDL codes. (3)

3. a) With a neat block diagram, explain the principle of operation of a digital storage oscilloscope. (5)

   b) Compare between the Analog and Digital storage oscilloscopes (3)

4. Show how a high power device can be interfaced to a microcomputer port with the example of a stepper motor driver circuit. Also derive the control status word and the data to be out from the microcomputer if the motor works in the full step mode (8)

5 a) The figure below shows a computer controlling the speed of a motor. The 0-2mA analog current from the DAC is amplified to produce the motor speeds from 0 to 1000 rpm. How many bits should be used if the computer is to be able to produce a motor speed that is within 2 rpm of the desired speed? (5)



b) Using 8 bits how close to 326 rpm can the motor speed be adjusted? (3)

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