BITS, Pilani – Dubai Campus
Knowledge Village, Dubai.
Second Semester 2003-2004
Comprehensive Examination

Advanced Computer Organization (CS UC 342)

Weightage: 40%

Date: 07.06.2

Max. Marks: 80.

Time: 3 Hrs

Partly Open Book

Note: All questions are compulsory. Write any assumption made with its requirement. Symbols ha usual meaning.

(CLOSED BOOK PART)

1. Given the MIPS Instruction format of type:

Opcode	Rs	Rt	Displacement

Give **Three** possible addressing modes this format can represent with example. (2+2+2)= 6

2. A C Program segment contains the FIVE variables f,g,h,i,and j : **f =(g+h)-(i+j);** What would be the MIPS Instructions generated by the C compiler?
3. What are the **two** key principles helped to built the today's digital computer systems? (2)
4. What is the MIPS code to test if variables **x** is less than variable **y** and then branch to label **LES** if the condition holds? (2)
5. What is the MIPS Code for the following C version of a ***switch*** statement ? (2)

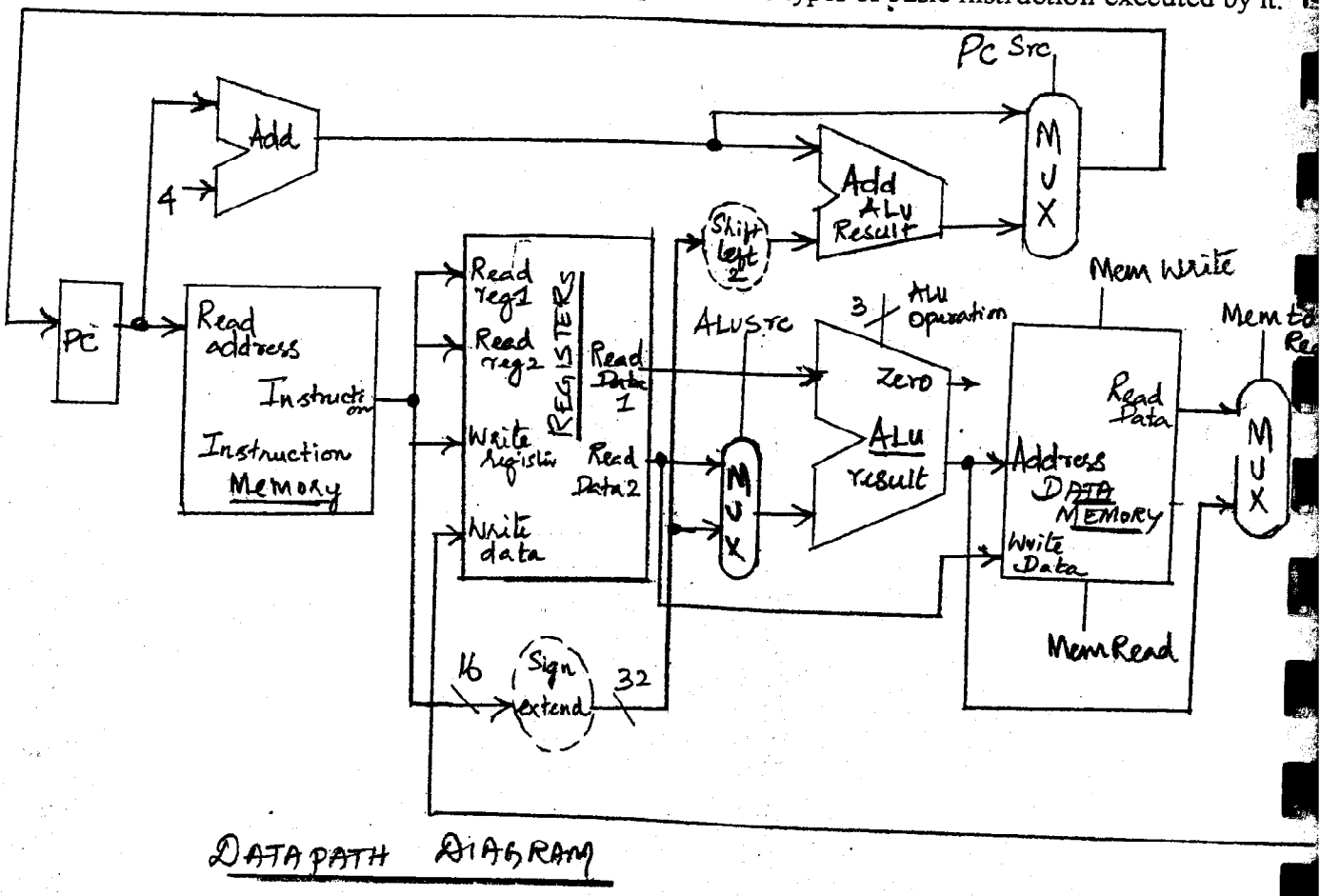
```
Switch ( k )
 {
  case 0: f=i+j;
   break;
 case 1: f=g+h;
   break;
 case 2: g-h;
  break;
case 3: i-j;
break;
}
```

6. Give the Translation Hierarchy diagram, that describes the **Four** steps involved in Transforming a C Program in a file on Disk into a Program running on a computer. (4)
7. Here is short loop which produces a result in register **$s0**. What the program does as a whole? What exactly gets stored in **$s0?** (3)

```
      beq  $s3, $s4, Loop1
      add $s0, $s1, $s2
Loop1: sub $s0, $s0, $s3
```

8. Give the first version of the Multiplication Hardware diagram. (2)
9. Define Clocking Methodology. Give any one of the clocking methodology implemented in the design of the Digital Computer Architecture. (2)
10. Draw and explain the datapath flow organization for fetching instructions and incrementing the program counter. (3)
11. What is the CPI for the following code segment, that has a mixture of 22% of load instructions, 11%of stroes instructions, 49% of R-format operations, 16% of Branch instructions, 2% of jumps instructions. And the number of cycles for each instructions class is has following:
    Load instructions = 5 cycles, Store instruction = 4 cycles, R-format operations = 4 cycles,
    Branch operations = 3 cycles, Jump operations = 3 cycles.
    Determine what is the maximum number of clock cycle required for all types of instructions and compare the same from the CPI value, whether the assigned number of clock cycles are correct or not? (4)

12. What are the **eight** specialized peripherals available for DSP? What is the use of On-chip peripherals design of DSP? (5)
13. Give the different types of processors applications based on increasing cost and increasing volume? (5)
14. For the diagram given below, check for the following: (10)
Whether the given diagram is a datapath for executing the instructions in a single clock cycle or not?What types of basic instructions are executed with the help of below given datapath diagram Explain the given datapath diagram, with respect to the types of basic instruction executed by it.



DATAPATH DIAGRAM

(Open Book Part)

15. What do you mean by **FIVE – STAGES Pipeline?** How many instructions will be executed during any single clock cycle? Explain them in detail with a block diagram. (10)
16. Since many instructions are simultaneously executed in pipeline datapath, what are the ***Two*** basi style of graphical representation of pipelining? (2)
17. What are the ***Three*** different types of Hazards in Pipeline Execution. (3)
18. What are the ***Three portions of*** an address in a direct-mapped cache or in a set associative cache? (3)
19. What do you mean by Write Through and Write Back in Cache? Give its advantages. (4)
20. What are the ***Three*** different I/O types are considered in the design of computer organization. (3)

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TEST – II (CLOSED BOOK)

Subject: CS UC 342 – ADVANCED COMPUTER ORGANIZATION

Duration: 50 mins

Max Marks: 40

Date: 02-05-2004

Weightage : 20

Answer all the Questions:

1. Explain Booth's Algorithm with its Hardware block diagram and give performance. (8

2. Compare and contrast the hardware requirements and performance of t three different versions of multiplication algorithms. (6

3. Explain and give a neat diagram illustrating the abstract overview Implementation of the MIPS datapath as subsets showing the major functional units and the major connection between them. (6

4. With a neat diagram, Explain the datapath for a load and store operations, followed by a memory address calculation to read or writ from memory and then to write the same into the register file if the instruction is load. (6)

5. Explain with a neat diagram revealing the Hardware / Software / IC Partitioning of a cellular Telephone Systems of DSP. (6)

6. Differentiate between DSP and General Purpose Microprocessor. (4)

7. Classify the Three Levels of DSP Applications and give examples. (4)

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SECOND SEMESTER –2004 – TEST -I

COURSE: CS UC342, III YEAR CS **DATE: *MAKE -I***
COURSE NAME: ADVANCED COMPUTER ORGANIZATION **MAX. MARKS:**
DURATION: 50 MINUTES **WEIGHTAGE:**
ANSWER ALL THE QUESTIONS:

1. Draw the major blocks of a Pentium Pro die and label the blocks. The die area is 306 m memory is a smaller fraction of the die area, because Pentium Pro is packaged with an exter In the block diagram locate the place and position Micro code control, Instruction decode, R stations, recorder buffer, cache and memory buffer area.
2. Assume that the manufacturing cost of a wafer $4500 and the defect density is 2.5 p centimeter, and the wafer radius is 20 cm, die area is 2 cm^2, Calculate the die per wafer, yield, per die for the die area of 1 cm^2 and 2 cm^2 .
3. Give the definition and the expression for the following terms: CPU clock cycles, CPU ti Clock cycle time, Performance.
4. An Application program runs in 10 seconds on computer X, which has a 600MHz clock. We a to help a computer designer build a machine, M, that will run this program in 6 seconds. The has determined that a substantial increase in the clock rate is possible, but this increase will a rest of the CPU design, causing machine M to require 1.2 times as many clock cycles as machi this program. What clock rate should we tell the designer to target?
5. Suppose Machine J has a clock cycle time of 1ns and a CPI of 2.0 for some program, and Ma has a clock cycle time of 2ns and a CPI of 1.2 for the same program. Which machine is faste program execution and by how much time?
6. Consider the machine with three instruction classes and they are compiled and executed different compilers and the table given below shows the instruction count for each instructio Assume that the machine's clock rate is 500 MHz. Which code sequence will execute faster ac to MIPS and according to Execution Time?

Code from	Instruction counts (in billions) for each instruction class		
	A	**B**	**C**
Compiler 1	5	1	1
Compiler 2	10	1	1

7. Answer the following:
   a) What are the MIPS Machine Instruction Fields represents, give a brief description of them

op	rs	rt	rd	shamt	func

   b) Categories the MIPS Assembly Language Instructions into **FOUR groups** and give Assembly code explaining each of the instructions.
   c) Illustrate **FIVE different** MIPS Addressing modes with a neat diagram.