BITS, PILANI – DUBAI 2013 – 2014
ANALOG ELECTRONICS (Make-up)

Course Code: ECE F341/EEE F341/INSTR F341/ECE C364
Course Title: Analog Electronics — Date: 13.4.2014
Duration: 50 Minutes — Weightage: 15%
Component: TEST 2 (Open Book) — Max Marks: 30

Note: This question paper has 5 questions and 2 pages. Answer all Questions. Semi log graph sheet is provided along with question Paper. Assume suitable data if required

Q1 The cut off frequency of a certain second order Butterworth low pass filter is **2KHZ**.Assume all the capacitor values to be **0.01μF** and feedback resistance R_f connected between pin2 and pin6 of op amp as **15.83kΩ.** Draw a schematic of the circuit and determine suitable values of all resistors used in the filter design. Also draw the frequency response of the filter by expressing gain in decibels for frequencies of 100Hz, 200Hz, 1000Hz, 2000Hz and 10,000Hz and find cut off frequency from the frequency response plot.

(6 Marks)

Q2 Two analog inputs represent two positive real quantities. Design an analog circuit that will determine both arithmetic mean and geometric mean of the two quantities. (4 Marks)

Q3 Design a suitable Signal conditioning circuit for the following specifications:

(i) Connect RTD (Resistance Temperature Detector of platinum type (Pt-100)) in one arm of the wheatstone DC bridge circuit which has temperature variations of 50°C - 90°C. Design a suitable signal conditioning circuit using Wheatstone bridge and op amp which can give 0 to 4 V output for a temperature range of 50°C - 90°C. The temperature co-efficient of resistance for RTD, $(\alpha) = 0.0034/°C$. Dissipation Constant of RTD (P_D)=30mW/°C. The error due to self-heating of RTD should not exceed 1°C. Assume supply for DC bridge circuit as 5V. Resistance at 0°C(R_0) for platinum type RTD is equal to 100Ω.

(ii) What additional modifications you can do in the above circuit design to get 4 – 20 mA current output for the same temperature range. .Also draw the necessary circuit diagram for the above specifications.

(10 marks)

Q4 Identify the circuit in Fig 1 and analyze its output voltage when $V_i > 0V$ and when $V_i < 0V$. Assume $R_F = R_1 = 1K\Omega$. Sketch the input and output waveforms

(5 marks)

P.T.O

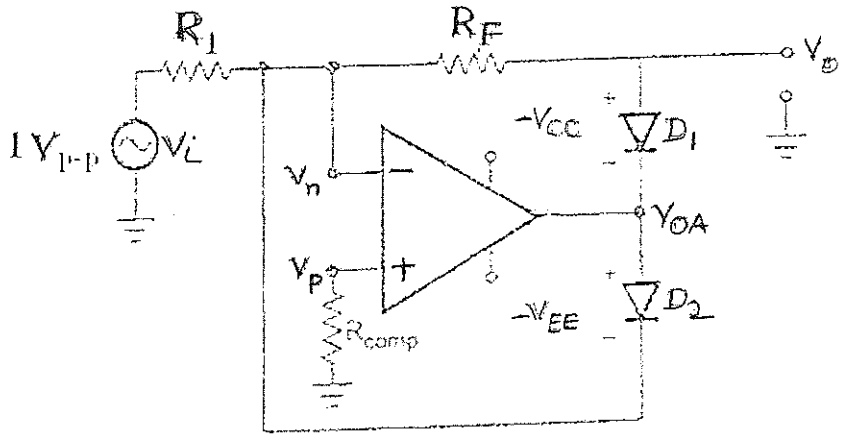

Figure 1

Q5 For the Schmitt trigger circuit shown in Fig 2, calculate the upper and lower threshold voltage levels. Assume Vsat = 0.9Vcc., Vcc =12V and Vin=10 Vp-p sinusoidal waveform. Sketch the input and output waveforms. What is the purpose of the 0.8kΩ resistor. Why the value is chosen as 0.8kΩ . Also sketch the output waveform if the input is triangular with a peak-peak voltage of 4 V.

(5 marks)

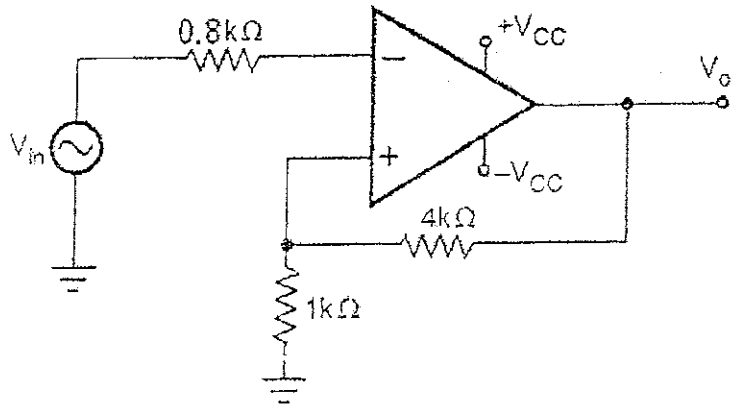

Figure 2

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BITS, PILANI – DUBAI CAMPUS

SECOND SEMESTER 2013-2014 THIRD YEAR ECE/EEE/EIE TEST1 (CLOSED BOOK)

Course Code: ECE C364/ ECE F341/EEE F341/ /INSTR C364/INSTR F341

Date: **23.02.2014**

Course Title: ANALOG ELECTRONICS Weightage:15%

Duration:50 Minutes Max Marks: 30

Note: This question paper has **2 Pages** & **5 questions**. Answer all questions.

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1. A common emitter amplifier has an npn transistor with β =80.The collector terminal is connected to a 10V power supply through a resistor Rc = 5KΩ. A dc bias of 1V is applied to the base terminal through a resistor R_B = 2KΩ & the emitter terminal is connected to ground through a resistor R_E = 1KΩ. The transistor is in the active mode of operation. Assume V_{BE} = 0.7V. Draw the necessary circuit diagram and determine I_C, I_B, I_E & V_{CE}.

[5M]

2. For the diode circuit of Fig.1(a) assume that the voltage drop across the diode when conducting is 0.7 V. For a sinusoidal voltage V_S as shown in Fig.1(b), draw the waveforms for the input (V_{in}) and output (V_o). What is the maximum voltage across the diode when it is not conducting?

[5M]

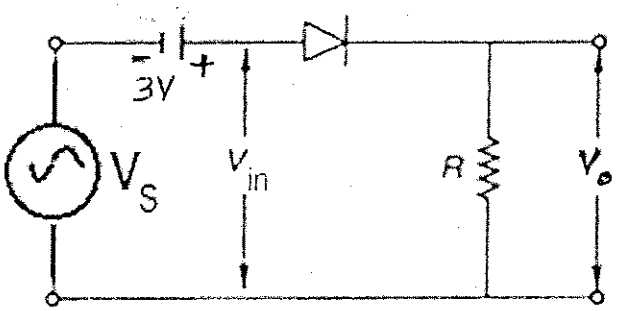

Fig. 1(a)

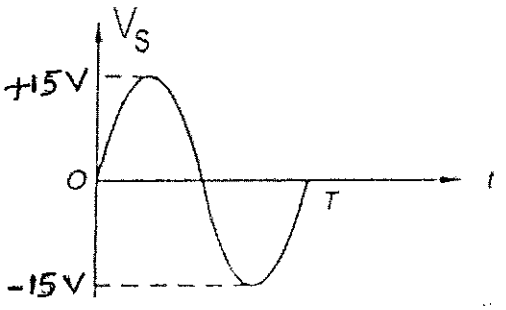

Fig.1(b)

3. In the circuit shown in figure 1(a), the signal source V_s (in volts) is changed to 0.01sin ωt and R = 100 Ω. The diode is replaced with a practical diode whose i_D and v_D are related by $i_D = I_S\left[e^{(v_D/V_T)} - 1\right]$, where I_S = 10^{-13} A and V_T = 26 mV
   (a) Do a DC analysis for the circuit and calculate I_D and V_D.
   (b) Determine the small signal ac resistance r_d for the diode
   (c) Draw the ac equivalent circuit and hence calculate the signal output voltage across R

[8M]

P.T.O

4. It is desired to implement the following expression:

$$V_o = (2v_1 + v_2 - 4v_3) \quad \text{.....(1)}$$

Where $v_1 = V_1 sin\omega t$, $v_2 = V_2 sin\omega t$ and $v_3 = V_3 sin\omega t$ are three ac inputs and V_o is the output voltage.

(a) Design two opamp circuits such that the inputs V_1 and V_2 are individually converted to $-V_1$ and $-V_2$ respectively.

(b) Using $-V_1$ and $-V_2$ available from (a) above, along with the third input V_3, design an inverting adder circuit such that equation (1) is implemented.

[7M]

5. Use only **<u>one</u>** non inverting op amp circuit to implement the following expression: $V_0 = V_1 - (V_2 + V_3 + V_4)$ where $V_1, V_2, V_3 and\ V_4$ represent dc battery sources and V_0 represents the output voltage. In your design, consider the feedback resistor R_f to be 6kΩ. All other resistors used in the circuit have identical values. Draw the complete circuit diagram. What is the input resistance provided by the opamp circuit for each of its inputs?
Note that for any battery source V_x, if its positive terminal is grounded, the negative terminal has a potential ($-V_x$).

[5M]

.....END OF PAPER.....