BITS, PILANI – DUBAI CAMPUS

Dubai International Academic City

II SEMESTER 2012 – 2013 III Yr ECE / EEE / EIE

Comprehensive Examination

Course No. : EEE / ECE / INSTR C391 Course Name : DECO

Duration : 3 hours Date : 10 – 03 – 2013 Max. Marks : 70

Clearly indicate the assumptions made if any. All logic used are positive logic

Answer Part A and Part B separately

Calculators are not allowed

PART A

1. a) Find the 16's complement of $(B2FA)_H$
   b) Convert $(B2FA)_H$ to binary
   c) Find 2's complement of the hexadecimal number $(B2FA)_H$
   d) Find the base of number system which satisfies following expression: $54/4 = 13$ (1.5 x 4M)

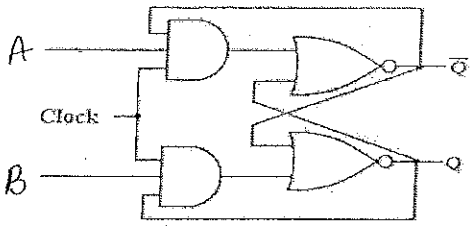
2.a. Construct NOT, OR, AND, NAND and EXOR gates using only positive logic NOR gate (0.5 + 0.5 + 1 + 1 + 2M)

b. i) Simplify the following boolean expression using boolean algebra
   $G = xyz + xyz' + x'yz + y'$
   ii) Represent the following Boolean expression in the two canonic forms SOP and POS
   $F = (C+D)' + A'C + A'B'CD$ (2 + 4)

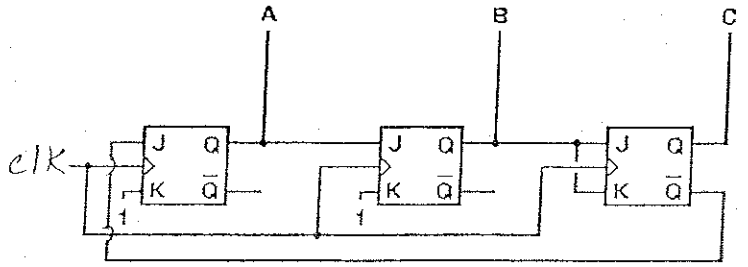
3.a) List the PLA programming table for the four bit binary to gray code converter. Optimize the no.of product terms for the PLA. (5M)

b) Draw a neat circuit and explain the function of each component of a three input TTL NAND gate circuit with totem-pole output. (4M)

4. a) Explain the operation of following flip flop circuit and develop its truth table (4M)



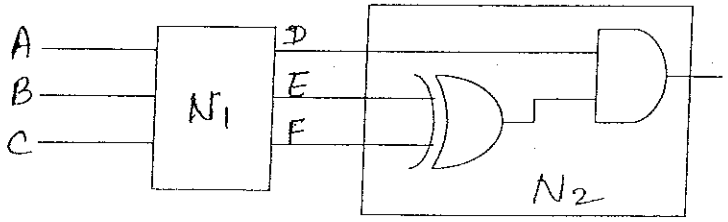
b) Construct the state stable and state diagram for the synchronous circuit given below. (5M)



PART B

(9) 5.a. Use a 4 x 1 multiplexer to implement the following function, assuming that all inputs and outputs are active high. It is required that minimum external logic gates to the MUX be used and that the data select inputs be A and B. Assume A is the MSB; F (A,B,C,D) = π (0,4,5,6,7,8,9,13,15) (4M)

b. A combinational circuit is divided into two sub networks N1 and N2 as shown in below. Network N1 is described by the truth table given in table 1. Redesign each of these sub networks N1 and N2 using minimum number of two input NAND gates (5M)



A	B	C	D	E	F
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	1	0	1

(5) 6. Given Boolean function F (w, x, y, z) = Σ (0,2,3,4,7,10,15) and don't care terms d (w, x, y, z) = (6,9,11,13) Using K-Map,

i)) Identify the Prime Implicants
ii) Identify the Essential Prime Implicants
iii) Find the reduced expression in the SOP form
iv) Implement the function using NOR gates alone
(Assume only true inputs are available) (5M)

(12) 7. Answer any three questions from the following (4 x 3)

a. Perform the operation -12 x 8 using Booth's algorithm. Verify your answer.

b. Explain the block diagram of non-restoration method for division of unsigned integer numbers. Show the step by step working of the division operation with an example 11 ÷ 4.

c. Draw the block diagram of a full adder circuit using half adders and NAND gates. Also write its Verilog HDL description .

Briefly explain the following

d. Carry Look Ahead adder.
e. ROM

(9) 8. a. Design a feedback shift register using D flip-flop to generate six timing signals. Draw its waveform with reference to the clock signal (4M)

b. Design a synchronous counter which counts states 0,1,3,4,6,7 using T flip flops. Assign don't care values for the unused states. (5M)

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II Sem Compre DEC.

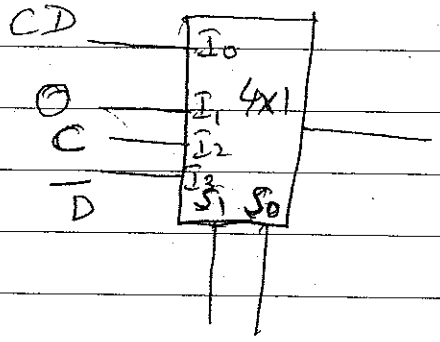
PART B MS.

10/03/13. Max Mark: 70.

PART B: 35 M

5. Q) $\Pi(0,4,5,6,7,8,9,13,15) = \Sigma(1,2,3,10,11,12,14)$

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	1	C+D
0	0	1	1	1	
0	1	0	0	0	
0	1	0	1	0	
0	1	1	0	0	0
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	
1	0	1	0	1	C
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	0	$\bar{D}$
1	1	1	0	1	
1	1	1	1	0	



(b) $D = C$.

$E = A \oplus B \oplus C$.

$F = A$

$G = (A \oplus B \oplus C \oplus F)' C$

$G = (A \oplus B \oplus C)' C$.

$= \bar{A}BC + A\bar{B}C$

$(\bar{A}B + A\bar{B})C$.

$= (A \oplus B) \cdot C$.

$= BC$

7. a). -12×8. Booths

M 01000
$-M$ 11000

A	Q	Q_{-1}		
00000	10100	0		
00000	01010	0	shift	I
00000	00101	0	shift	II
11000	00101	0	A−M	III
11100	00010	1		
00100	00010	1	A+M	IV
00010	00001	0		
11010	00001	0	A−M	V
11101	00000	1		

$2^1C. - 00011\ 00000. = 64 + 32 = 96.$

$12 \times 8 = 96.$

(b). Non Restoration method 11×4.

$M = 0100$
$-M = 1100$.

A	Q		
0000	1011		
0001	011−		
1101	0110	Sub M	I
1010	110−	shift left	II
1110	1100	Add M.	
1101	100−		III
0001	1001		
0011	001−		
1111	0010		IV
0011	0010	A+M.	

Reminder. Quotient.

BITS PILANI, DUBAI CAMPUS

II SEMESTER 2012 – 2013

Course Code: **EEE / ECE / INSTR C391** **TEST-2 (Open Book)** Date: 16.**05.2013**

Course Title: **DECO** Max.Marks:30

Duration: **50 minutes** Weightage: **15%**

Instructions: 1.ANSWER all questions in sequence of their order.
2. Clearly state the assumptions made if any.
3. All questions carry 5 marks each

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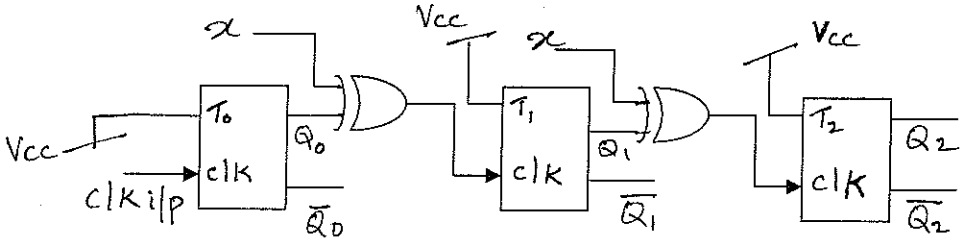
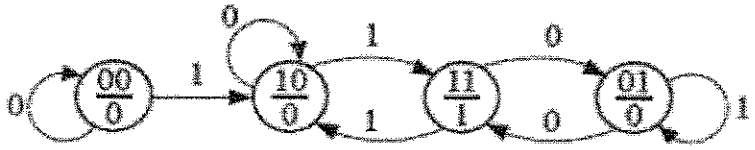
1. Design a JK flip-flop using T – flip-flop

2. Analyse the following Asynchronous sequential circuit and explain the function. Also draw its state diagram

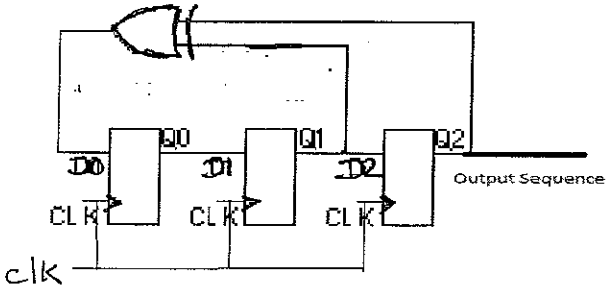


3. Design a sequential circuit for the following state diagram using D flip-flop (Synchronous)



4. Develop the PLA programming table of a Full adder circuit and draw the PLD diagram

5. Indentify the output binary sequence from the circuit if the initial state of Q_2,Q_1,Q_0 is 101



6. Design an universal Shift Register for the given function table.

Control signals (C_1 C_0)	Function
0 0	Clear the register
0 1	Load new data
1 0	Shift right
1 1	No change

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DEC 2. / II Sem 2012-2013

MS for T2. (16-05-13)

(4)

$S = \Sigma\, 1,2,4,7 = A'B'C + A'BC' + AB'C' + ABC$

$C = \Sigma\, 3,5,6,7 = (\Sigma\, 0,1,2,4) = (A'B'C' + A'B'C + A'BC + AB'C')'$

programming table:

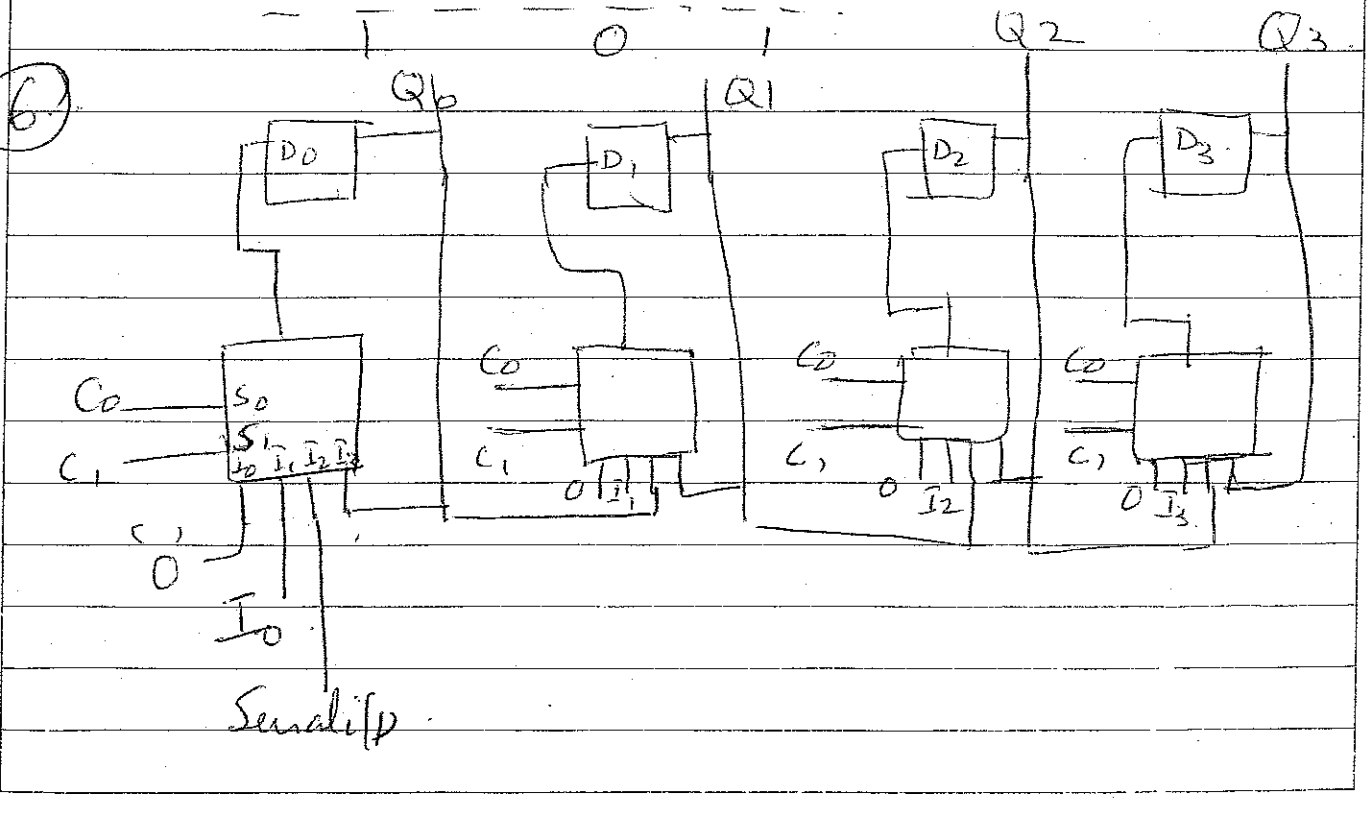
Product terms	i/ps A	B	C	o/ps Sum(T)	Carry (C)
1	0	0	0	—	1
2	0	0	1	1	1
3	0	1	0	1	1
4	1	0	0	1	1
5	1	1	1	1	—

(5)

	Q_0	Q_1	Q_2
initial state	1	0	1
	1	1	0
	1	1	1
	0	1	1
	0	0	1
	1	0	0
	0	1	0
	1	0	1

o/p sequence is 1 0 1 1 1 0 0 1

(6)



BITS PILANI, DUBAI CAMPUS

II SEMESTER 2012 – 2013

Course Code: EEE / ECE / INSTR C391 TEST-1 Date: 21.03.2013

Course Title: DECO Max.Marks:30

Duration: 50 minutes Weightage: 15%

Instructions: 1.ANSWER all questions in sequence of their order.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Calculators are not allowed

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1. Convert the following $(101101.0110)_2 = (\text{----------})_{10} = (\text{----------})_8$ 3

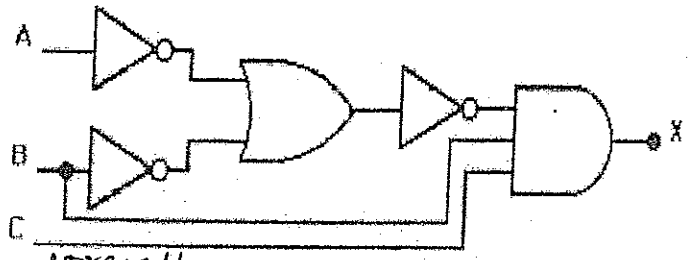
2. Simplify the following function using K-map and implement the same using two level NOR gates alone 5
$F(A,B,C,D) = \sum(1,3,5,6,7,8,9,) + d(10,11,12,13,14,15)$

3. Implement the following function using only two 2 to 4 line active high decoders with enable pin and basic logic gates 5
F(A,B,C) = ∑ (0,1,4,7)

4. Design a half adder using dual 2x1 multiplexer 4

5. Design a full subtractor circuit 4

6. Write the input - output truth table of the following logic circuit 4



7. Design logical circuit to implement following function using k-Map. 5
&Draw the

Input				Output
A3	A2	A1	A0	F
1	1	1	1	1
1	1	1	0	1
1	1`	0	1	1
1	1`	0	0	1
1	0`	1	1	1
1	0`	1	0	1
All other input values				0

NAME: ID NO:

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Version B

Course Code: **EEE C391/ECE 391/ INSTR C391** **Quiz-2** Date: 23.**04.2013**

Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

Duration: **20 minutes** Weightage: **5%**

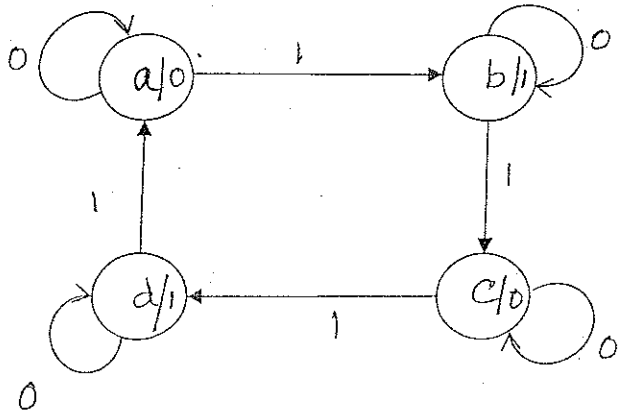
Instructions: 1.ANSWER all questions at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Questions 1-4 carry one Marks each questions 5-7 carry two marks each.
4.. Write on back side if the space is insufficient.

1. Draw the **state diagram** of the **D** flip-flop

2. Convert **D Flip–Flop into T** flip flop

3. Draw the logic diagram of a **JK flip flop with preset and clear using NAND gates**

4. **Write the output sequence** of the sequential circuit described by the state diagram shown in figure below for the give **input sequence 101101001**. Assume the initial state is '**c**'



NAME: ID NO:

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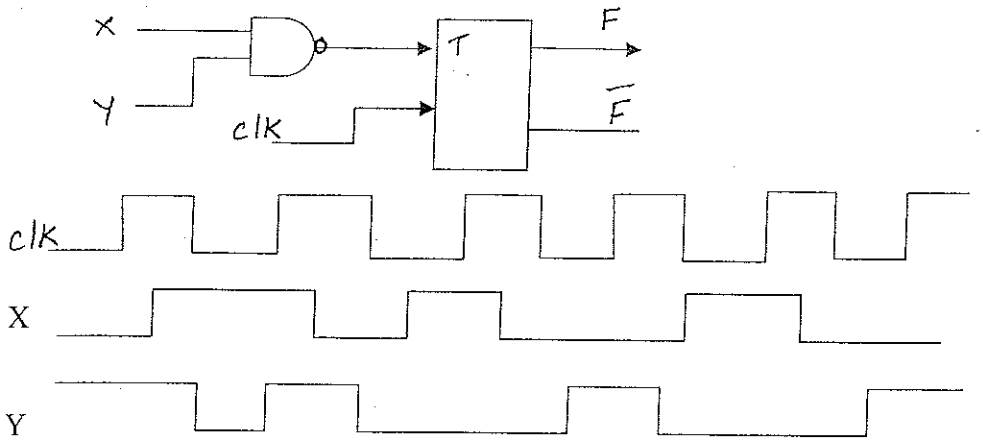
II SEMESTER 2012 – 2013

III Yr ECE/EEE/EIE

5. For the following input signals shown in the figure, draw the flip flop output waveforms



F

6. Write the Boolean expression for two 2-bit word (C_1C_0 and D_1D_0)comparator to give outputs LT, GT and EQ

7. Draw the logic diagram to implement a 2x2 bit multiplier circuit

MS.

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BITS, PILANI – DUBAI CAMPUS

II SEMESTER 2012 – 2013

III Yr ECE/EEE/EIE

Version B

Course Code: EEE C391/ECE 391/ INSTR C391 Quiz-2 Date: 23.04.2013

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Duration: 20 minutes Weightage: 5%

Instructions: 1.ANSWER all questions at the space provided.
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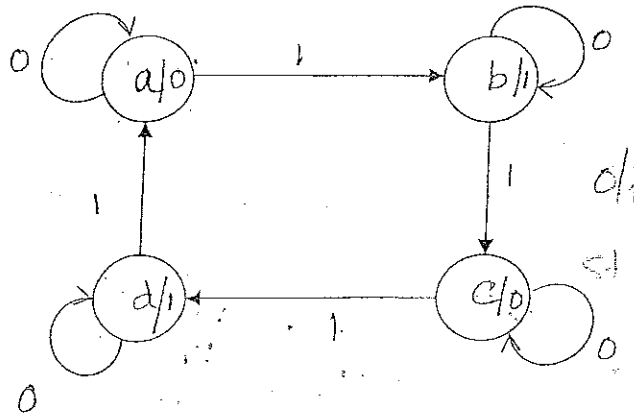
3. Questions 1-4 carry one Marks each questions 5-7 carry two marks each.
4.. Write on back side if the space is insufficient.

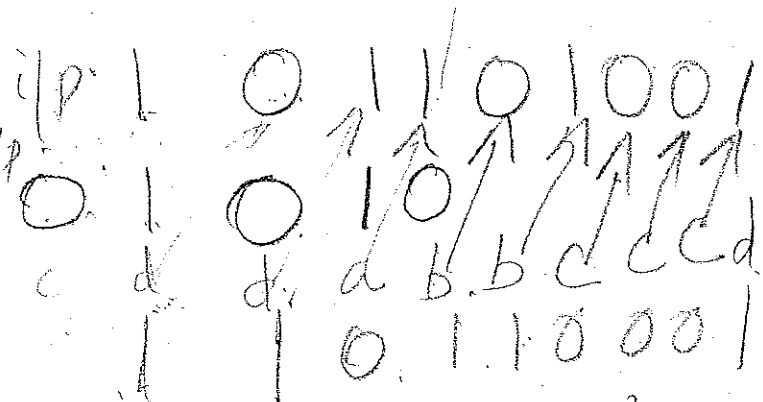
1. Draw the **state diagram** of the D flip-flop

2. Convert D Flip–Flop into T flip flop

3. Draw the logic diagram of a JK flip flop **with preset and clear using NAND gates**

4. **Write the output sequence** of the sequential circuit described by the state diagram shown in figure below for the give **input sequence 101101001**. Assume the initial state is 'c'





NAME: B MS. ID NO:

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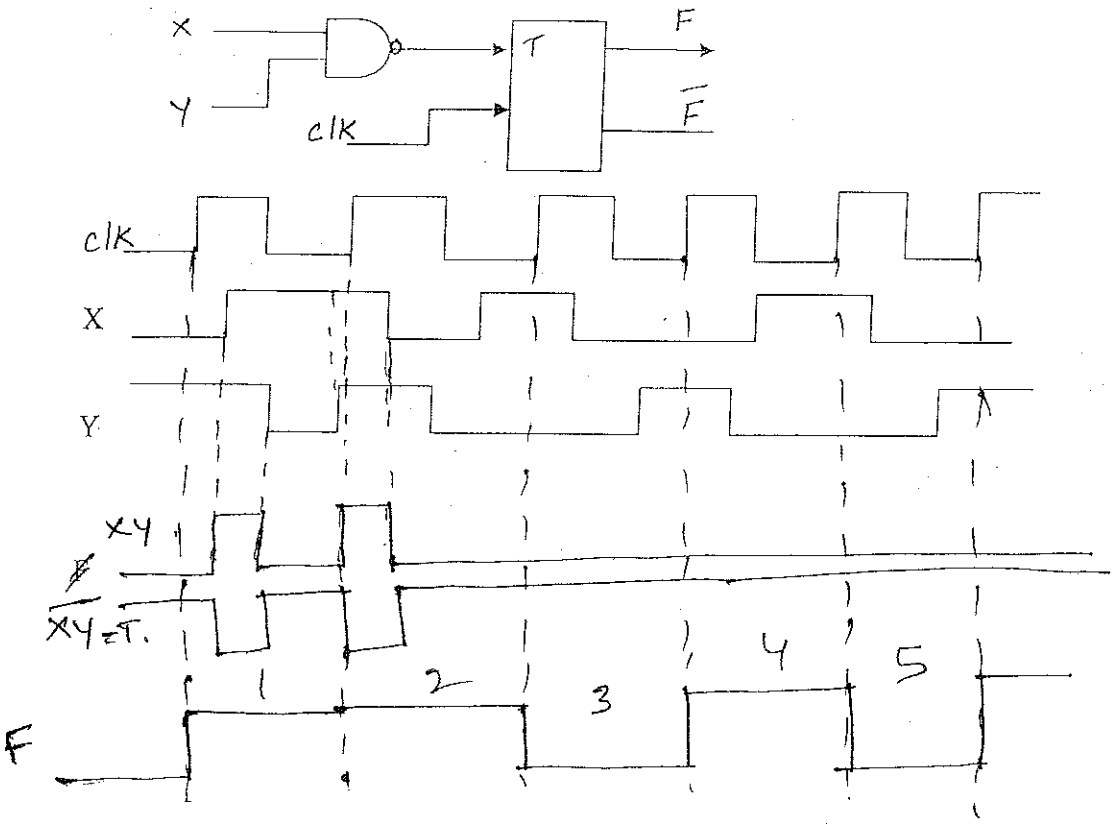
III Yr ECE/EEE/EIE

5. For the following input signals shown in the figure, draw the flip flop output waveforms



6. Write the Boolean expression for two 2-bit word (C_1C_0 and D_1D_0) comparator to give outputs LT, GT and EQ

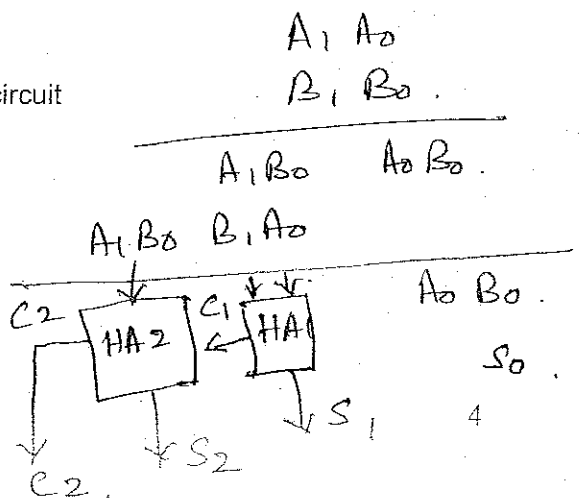
$LT = \bar{C_1} D_1 + x_1(\bar{C_0} D_0)$; $x_1 = \overline{(C_1 \oplus D_1)}$

$GT = C_1 \bar{D_1} + x_1 (C_0 \bar{D_0})$;

$EQ = x_1 \cdot x_0$; $x_0 = \overline{(C_0 \oplus D_0)}$

7. Draw the logic diagram to implement a 2x2 bit multiplier circuit

$P = C_2 S_1 S_2 S_0$. (4 bit).



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II SEMESTER 2012 – 2013

III Yr ECE/EEE/EIE

Version A

Course Code: **EEE C391/ECE 391/ INSTR C391** **Quiz-2** Date: 23.**04.2013**

Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

Duration: **20 minutes** Weightage: 5%

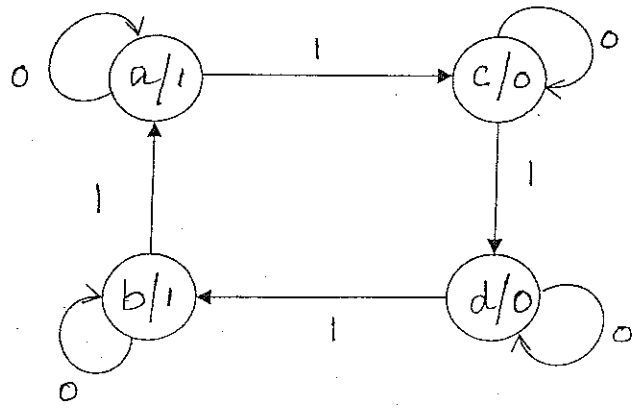
Instructions: 1.ANSWER all questions at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Questions 1-4 carry one Marks each questions 5-7 carry two marks each.
4.. Write on back side if the space is insufficient.

1. Draw the **state diagram** of the **T** flip-flop

2. Convert **D Flip–Flop into JK** flip flop

3. Draw the logic diagram of a **JK flip flop with preset and clear using NAND gates**

4. **Write the output sequence** of the sequential circuit described by the state diagram shown in figure below for the give **input sequence 101101001**. Assume the initial state is '**c**'



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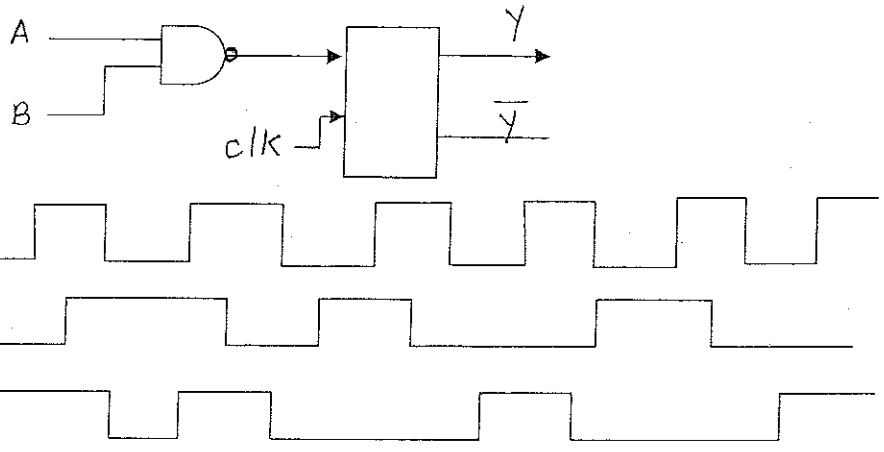
II SEMESTER 2012 – 2013

III Yr ECE/EEE/EIE

5. For the following input signals shown in the figure, draw the flip flop output waveforms



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6. Write the Boolean expression for two 2-bit word (A_1A_0 and B_1B_0)comparator to give outputs LT, GT and EQ

7. Draw the logic diagram to implement a 2x2 bit multiplier circuit

MS.

NAME: ID NO:

BITS, PILANI – DUBAI CAMPUS

II SEMESTER 2012 – 2013

III Yr ECE/EEE/EIE

Version A

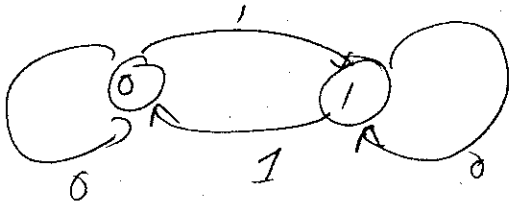
Course Code: **EEE C391/ECE 391/ INSTR C391** **Quiz-2** Date: 23.**04.2013**

Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

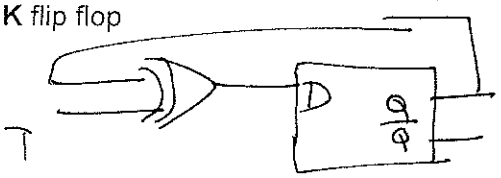
Duration: **20 minutes** Weightage: **5%**

Instructions: 1.ANSWER all questions at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Questions 1-4 carry one Marks each questions 5-7 carry two marks each.
4.. Write on back side if the space is insufficient.

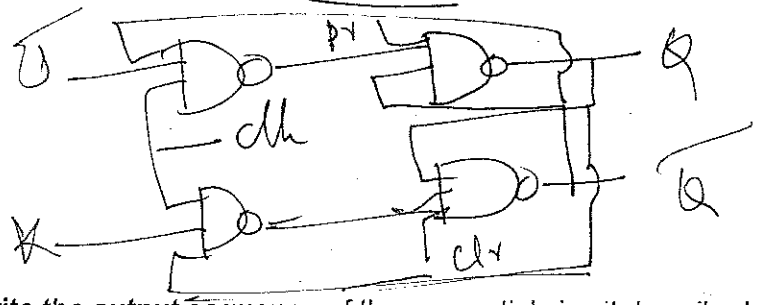
1. Draw the **state diagram** of the **T** flip-flop



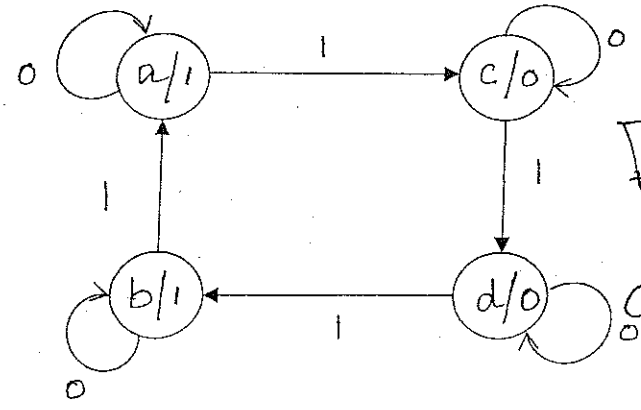
2. Convert **D Flip–Flop into JK** flip flop



3. Draw the logic diagram of a **JK flip flop with preset and clear using NAND gates**



4. **Write the output sequence** of the sequential circuit described by the state diagram shown in figure below for the give **input sequence 101101001**. Assume the initial state is '**c**'



1	0	1	1	0	1	0	0	1
d	d	b	a	a	c	c	c	d
0	0	1	1	1	0	0	0	0

1

NAME: A MS ID NO:

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II SEMESTER 2012 – 2013

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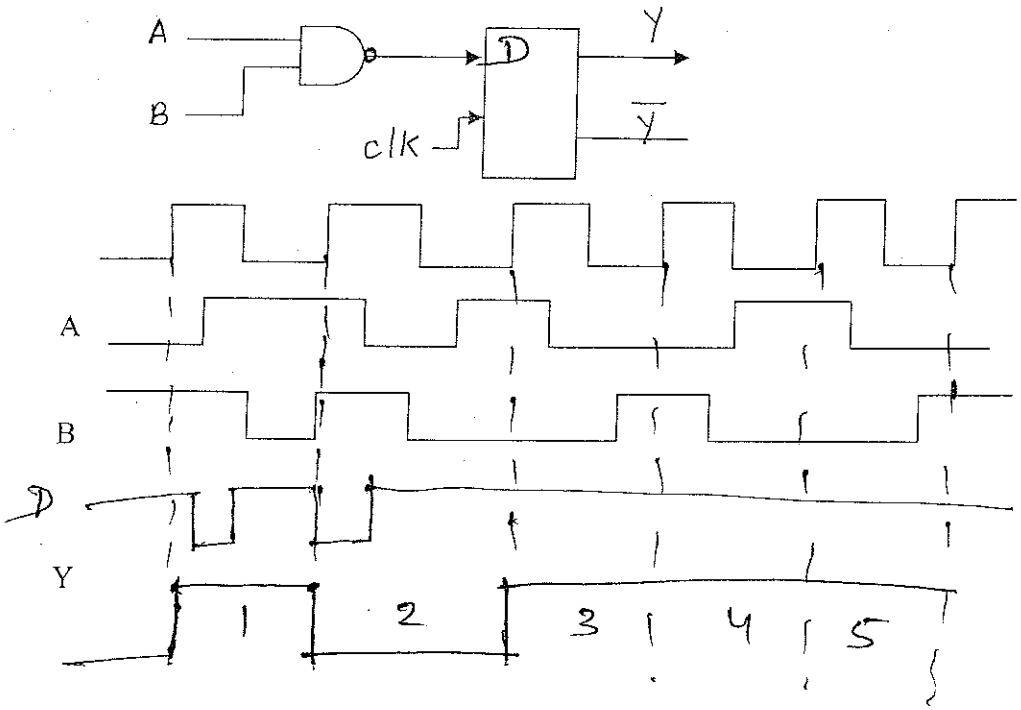
5. For the following input signals shown in the figure, draw the flip flop output waveforms



6. Write the Boolean expression for two 2-bit word (A_1A_0 and B_1B_0)comparator to give outputs LT, GT and EQ

7. Draw the logic diagram to implement a 2x2 bit multiplier circuit

NAME: _____; ID NO: _____;

SET A

BITS PILANI, DUBAI CAMPUS

II SEMESTER 2012 – 2013 III Yr ECE/EEE/EIE

Course Code: **EEE C391/ ECE C391/ INSTR C391** **Quiz-1** Date:05.**03.2013**

Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

Duration: **20 minutes** Weightage: **5%**

Instructions: 1.ANSWER all questions **with most appropriate answer(s)**, at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. **Calculators are not allowed**

1. Find out the **base x** of number system if $(101)_x=(26)_{10}$

2. Convert $(\mathbf{2345.76})_8$ to hexadecimal

3. compute $(964)_{BCD}+(751)_{BCD}$

4. Write the missing Gray code

Binary	Gray code
0000	0000
0001	0001
1111	- - - -

5. Use 2's complement arithmetic to compute 13 – 24.

NAME: _____; ID NO: _____;

SET A

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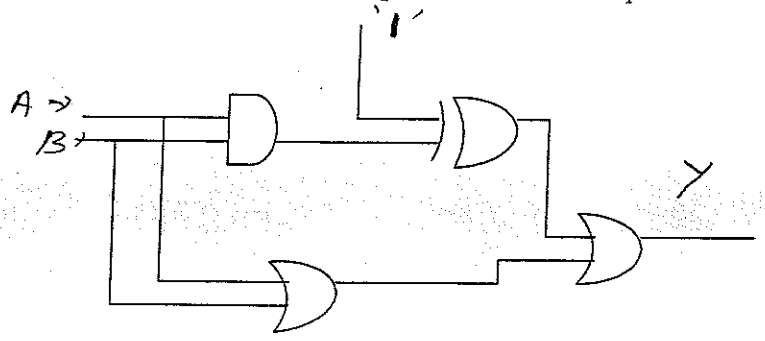
6. Simplify the following logic expression using Boolean Algebra **P(x,y,z) = x'y +xy' +xyz**

7. Express the 3-variable Boolean function F(A,B,C) = Σ (2,3,4,6) in **maxterms**

8. Implement function $Y = AB + \overline{AB}$ by using **only two EX-OR** gates

9. Implement the Boolean function F(p, q, r) = **(p+r')(q'+r)** using **NAND** gates alone

10. Write the **simplified Boolean expression** for the output of the circuit shown in figure below.



NAME: _____; ID NO: _____;

SET A

BITS PILANI, DUBAI CAMPUS

II SEMESTER 2012 – 2013 III Yr ECE/EEE/EIE

Course Code: EEE C391/ ECE C391/ INSTR C391 Quiz-1 Date:05.03.2013

Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

Duration: **20 minutes** Weightage: 5%

Instructions: 1.ANSWER all questions **with most appropriate answer(s)**, at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. **Calculators are not allowed**

1. Find out the **base x** of number system if $(101)_x=(26)_{10}$

$x^2+1=26$; $x=5$.

2. Convert $(2345.76)_8$ to hexadecimal $010011100101 . 111110$

$= 4E5.F8$

3. compute $(964)_{BCD}+(751)_{BCD}$

```
 1001  0110  0100        964 +
 0111  0101  0001        751
-----------------
 1 0001 1011  0101
       0110  0110
-----------------
 1 0111 0001  0101  = 1715
```

4. Write the missing Gray code

Binary	Gray code
0000	0000
0001	0001
1111	----

1000

5. Use 2's complement arithmetic to compute 13 – 24.

```
+13 -> 0 0 1 1 0 1
+24 -> 0 1 1 0 0 0   +
-24 -> 1 0 1 0 0 0
-ve    1 1 0 1 0 1
2's C -> 0 0 1 0 1 1 = -11
```

NAME: _____; ID NO: _____;

SET A

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6. Simplify the following logic expression using Boolean Algebra **P(x,y,z) = x'y +xy' +xyz**

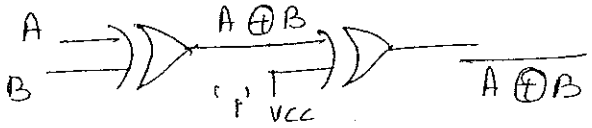
$= x'y + xy' + (xz) = x'y + xy' + (yz)$ (any one).

7. Express the 3-variable Boolean function F(A,B,C) = Σ (2,3,4,6) in **maxterms** $= \Pi(0,1,5,7)$

$= (A+B+C).(A+B+\bar{C}).(\bar{A}+B+\bar{C}).(\bar{A}+\bar{B}+\bar{C})$

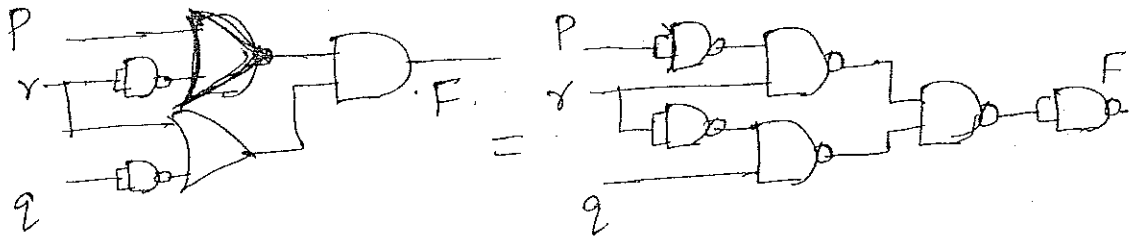
8. Implement function $Y = AB + \overline{A}\,\overline{B}$ by using **only two EX-OR gates**

$A B + \bar{A}\,\bar{B} = \overline{\bar{A}\cdot B + A\bar{B}} = \overline{A \oplus B}$

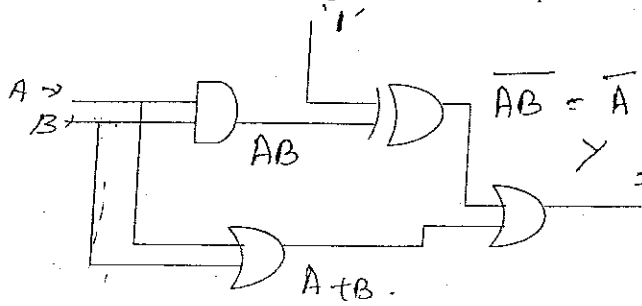
$\therefore$ 

$= AB + \bar{A}\,\bar{B}$

9. Implement the Boolean function F(p, q, r) = **(p+r')(q'+r)** using **NAND** gates alone



10. Write the **simplified Boolean expression** for the output of the circuit shown in figure below.



$\overline{AB} = \bar{A} + \bar{B}$

$Y = \bar{A} + \bar{B} + A + B = 1.$

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SET A

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Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

Duration: **20 minutes** Weightage: **5%**

Instructions: 1.ANSWER all questions **with most appropriate answer(s)**, at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. **Calculators are not allowed**

1. Find out the **base x** of number system if $(101)_x=(37)_{10}$

2. Convert $(\mathbf{5432.67})_8$ to hexadecimal

3. compute $(867)_{BCD}+(751)_{BCD}$

4. Write the missing Gray code

Binary	Gray code
0000	0000
0001	0001
1010	- - - -

5. Use 2's complement arithmetic to compute 31 – 42.

NAME: _____; ID NO: _____;

SET B

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SET B

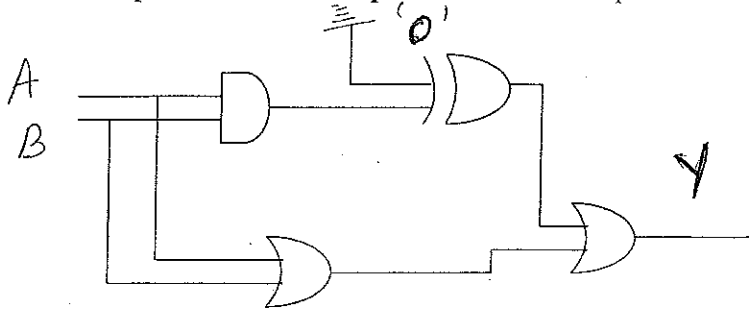
6. Simplify the following logic expression using Boolean Algebra **P(x,y,z) = x'y +xy' +x'y'z**

7. Express the 3-variable Boolean function F(A,B,C) = π (2,3,4,6) in **minterms**

8. Implement function **Y=A'B + AB'** by using **only two EX-NOR** gates

9. Implement the Boolean function **F(p, q, r) = (p+r')(q'+r)** using **NAND** gates alone

10. Write the **simplified Boolean expression** for the output of the circuit shown in figure below.



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SET B

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Instructions: 1.ANSWER all questions with most appropriate answer(s), at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Calculators are not allowed

1. Find out the base x of number system if $(101)_x=(37)_{10}$

$x^2+1=37;$ $x=6.$

2. Convert $(5432.67)_8$ to hexadecimal $101\,100\,011\,010 \cdot 110\,111 = B1A.DC$

3. compute $(867)_{BCD}+(751)_{BCD}$

	1000	0110	0111
	0111	0101	0001
1	0000	1011	1000
		0110	0110
1	0110	0001	1000

	8	67
	7	51
	1	618

4. Write the missing Gray code

Binary	Gray code
0000	0000
0001	0001
1010	----

1111.

5. Use 2's complement arithmetic to compute 31 – 42.

$+31 = 0011111$

$+42 = 0101010$

$2'c\text{-}42 = 1010110$ +

1110101 – ve no:

$2'c = -0001011 = -11.$

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SET B

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SET B

6. Simplify the following logic expression using Boolean Algebra P(x,y,z) = x'y +xy' +x'y'z

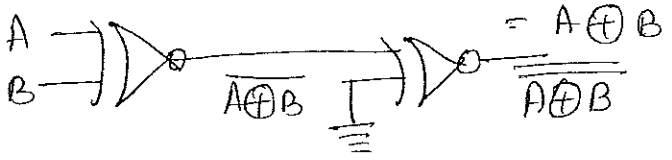
$= x'y + xy' + x'z / y'z$

7. Express the 3-variable Boolean function F(A,B,C) = π (2,3,4,6) in minterms $= \Sigma(0,1,5,7)$

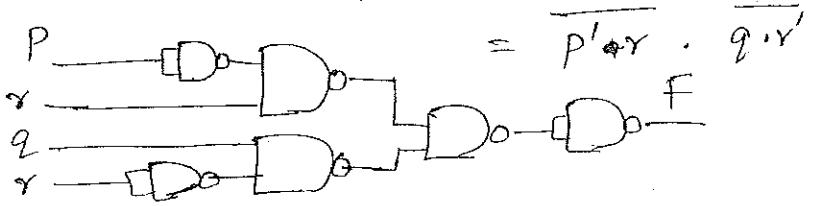
$= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + ABC$

8. Implement function Y=A'B + AB' by using only two EX-NOR gates $A'B + AB' = A \oplus B$

$= \overline{A \oplus B}$ ∴



9. Implement the Boolean function F(p, q, r) = (p+r')(q'+r) using NAND gates alone



10. Write the **simplified Boolean expression** for the output of the circuit shown in figure below.