BITS, PILANI – DUBAI	
SECOND SEMESTER 2012 – 2013	
Course Code: ECE C364	Date: 8.06.2013
Course Title: Analog Electronics	Max Marks: 60
Duration: 3 Hours	Weightage: 30%
Component: COMPREHENSIVE EXAM (CLOSED BOOK)	

Note: This question paper contains 6 questions and 4 pages.. Answer all Questions. Assume suitable data if required.

Q1(a) By applying Superposition Principle determine the output voltage for the circuit shown in Fig.1 if V_1 = 2V, V_2=1V and V_3= 1V..

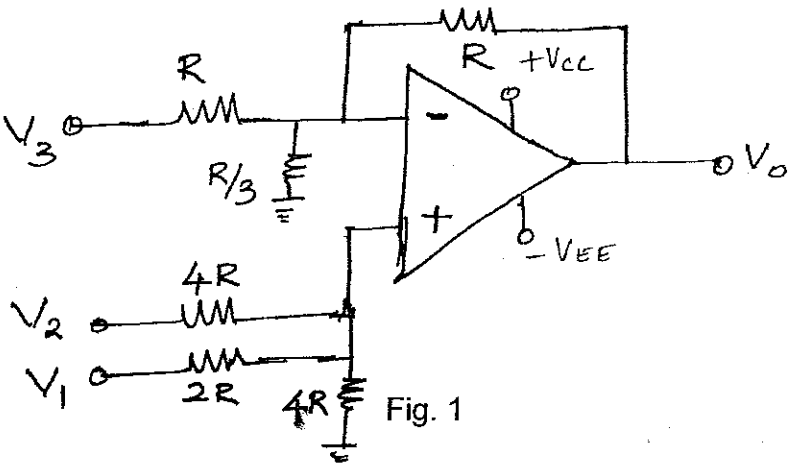


Fig. 1 [5M]

(b) An op-amp using IC741 is connected as a Non-inverting amplifier with R_1(connected between pin 2 and ground) =1kΩ and R_F = 10KΩ.Draw the circuit diagram and assume that the IC 741 OP AMP Connected in the circuit has the following parameters:

A=200,000,R_{in} = 2MΩ, Ro =75Ω,Supply voltage = ±15V

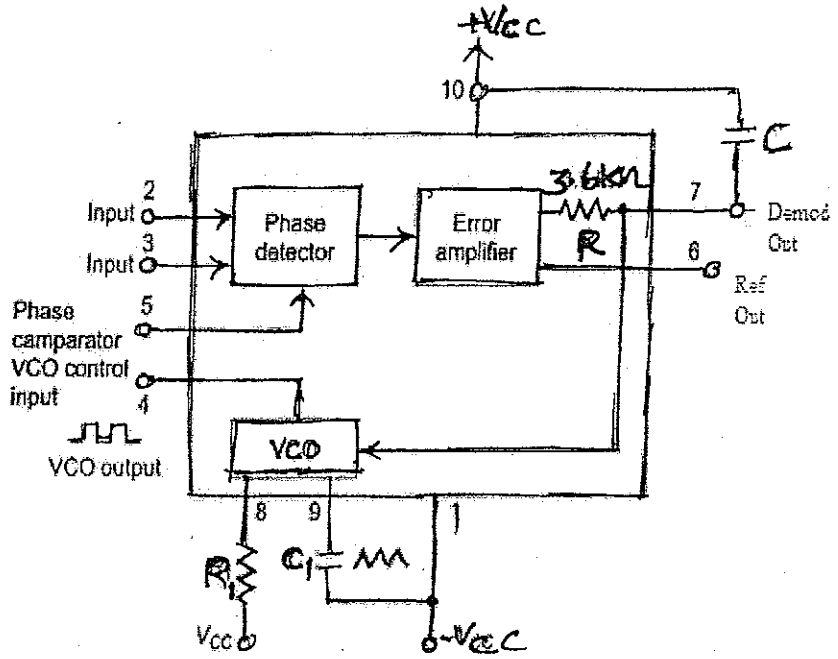
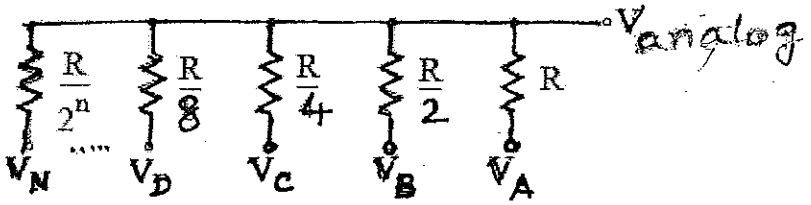
Find the voltage gain with feedback, input resistance with feedback and output resistance with feedback for the above amplifier. [3M]

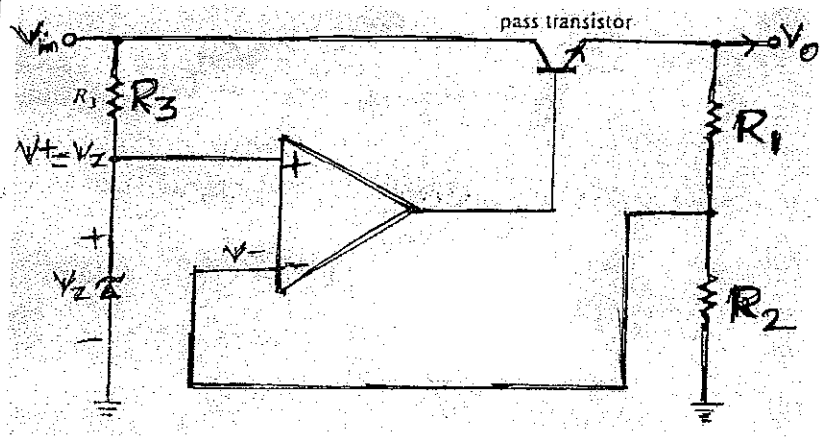
(C) Implement the following expression

$$V_0 = 2\cdot[(V_1+V_2) - (V_3+V_4)]$$

Using only two inverting op-amps. Assume that the inputs V_1,V_2 V_3 and V_4 cannot be modified before they are applied to the op amp inputs. The input resistance for the op amp circuit is required to be 10kΩ. The opamp supply voltages are ±10V.All the applied inputs are in volts. Draw the complete circuit diagram. [4M]

P.T.O

Q2(a)	For the circuit shown in Fig.2, given the free running frequency as 100KHZ, the demodulation capacitor of 2μF and supply voltage is ± 6V, determine the lock and capture frequencies and find the value of C_1. Assume R_1 =12KΩ.  Fig.2	[5M]
(b)	Fig. 3 shows a digital to analog converter with binary weighted resistors. Derive an expression for Vanalog.  Fig. 3	[3M]
(C)	List the different types of Analog to digital Converter.	[2M]

3(a)	With respect to signal conditioning circuit using RTD, answer the following question: Connect RTD (Resistance Temperature Detector of platinum type (Pt-100)) in one arm of the wheatstone DC bridge circuit which has temperature variations of 50°C-90°C. Design a suitable signal conditioning circuit using whetstone bridge and op amp which can give 0-4V output for a temperature range of 50°C-90°C .Use temperature Co-efficient for RTD ($\propto$) $= 0.0034/°C$. Dissipation Constant of RTD (P_D)=30mW/$°C$. The error due to self-heating of RTD should not exceed 1°C.Assume supply for DC bridge circuit as 5V. Resistance at 0°C(R_0) for platinum type RTD is equal to 100Ω.	[8M]
(b)	Draw the output waveform if Vi = 5Sin ωt is applied to the input of the squarer circuit and the output passed through a DC blocking capacitor	[2M]
Q4(a)	An op-amp based voltage regulator is shown in Fig. 4. The zener diode is designed to operate at 10 V, 0.5 A. In the circuit, R_1 = 20 kΩ, R_2 = 10 kΩ. Assuming that the op amp is ideal, determine the following: (i) output voltage, V_o, (ii) minimum input voltage V_{in} (Assume V_{CE}=0.2V) (iii) the value of R_3 based on minimum V_{in} If the op amp is not ideal with an open loop gain of 1000, by how much will the output voltage Vo change?  Fig. 4	[5M]
(b)	Realize log and antilog amplifiers using opamp, transistor and resistors. Show how log and antilog amplifiers can be used as a building block to obtain an output waveform $y=a^b$ where a and b are independent input waveforms.	[3M]

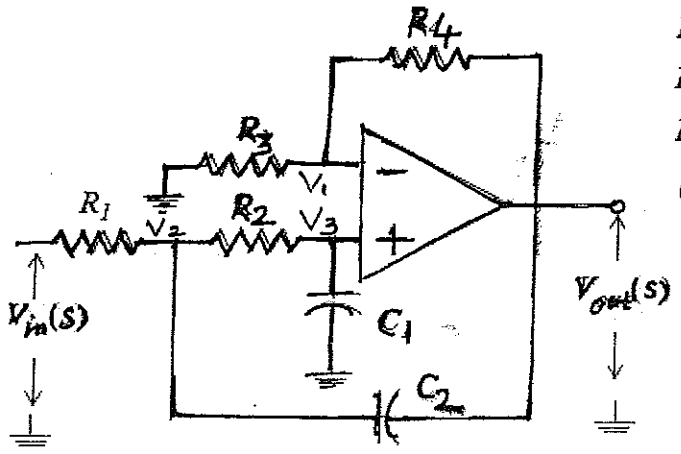
Q5(a) Design the circuit diagram of IC 723 based positive voltage regulator to give +8V output at 200mA. Incorporate short circuit protection current limit circuit to operate at 400mA. Find all resistor values .Calculate their wattage and specify the type of resistors. Assume C=500pF,R_1=1kΩ (connected between pin3 and pin4)and V_{ref} =7V.Draw the complete circuit diagram. [5M]

(b) In Class A power amplifier, the total collector current is given by

$$i_c = (2.3)(2 + V_{in})^3 \text{ mA}$$

where the input V_{in} (in mV) = 10sinωt. Determine the quiescent collector current, average collector current and the total harmonic distortion for the power amplifier. Given $sin3\theta = 3sin\theta - 4sin^3\theta$ [5M]

Q6(a) Compute the transfer function $G(s) = \frac{V_{out}(s)}{V_{in}(s)}$ for the circuit shown in Fig.5



$R_1 = 11.3\ k\Omega$
$R_2 = 22.6\ k\Omega$
$R_3 = R_4 = 68.1\ k\Omega$
$C_1 = C_2 = 0.01\ \mu F$

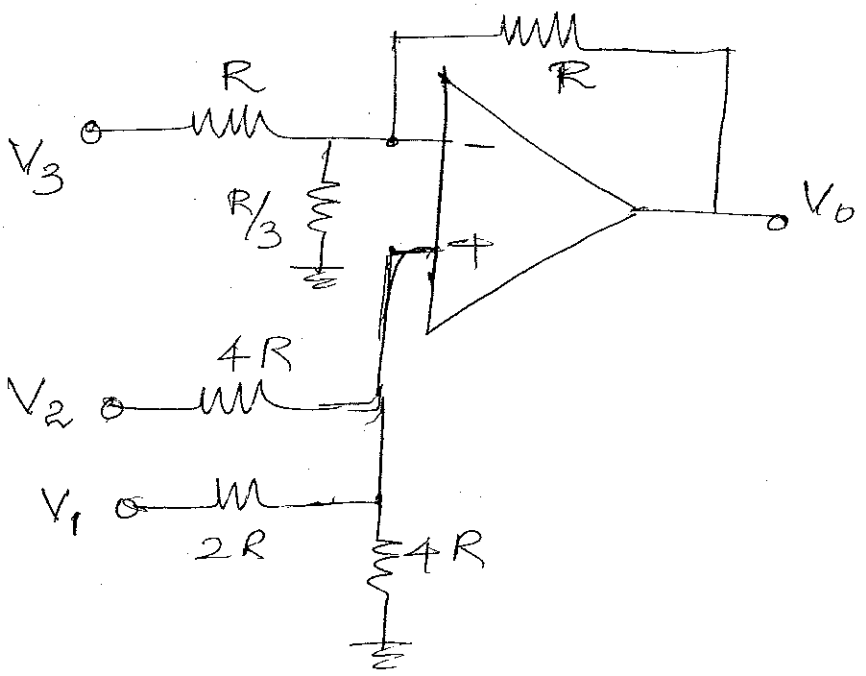
[8M]

Fig. 5

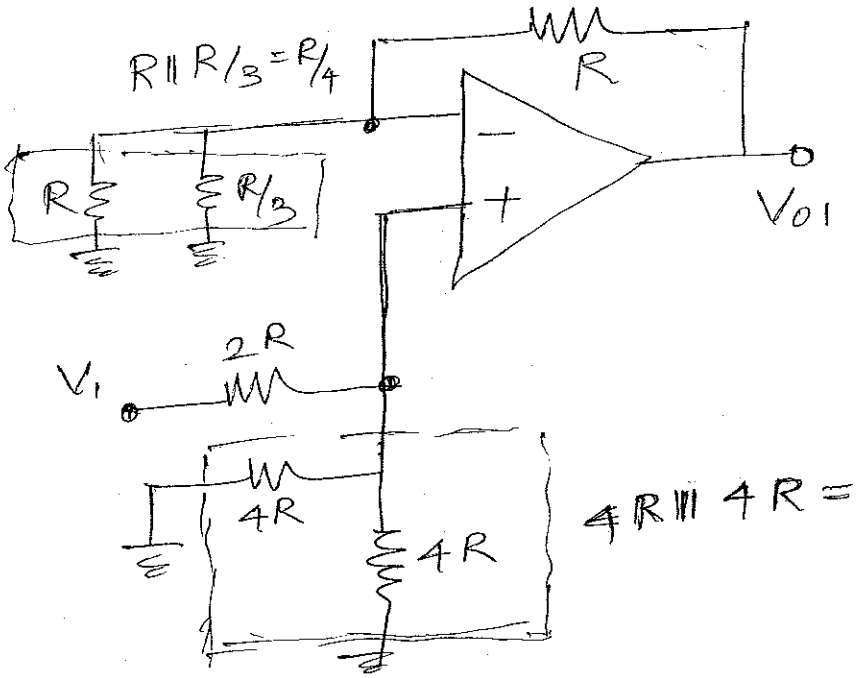
(b) Positive or regenerative feedback is an essential characteristic of all oscillator circuits. Why, then, do comparator circuits utilizing positive feedback not oscillate? Instead of oscillating, the output of a comparator circuit with positive feedback simply saturates to one of its two rail voltage values. Explain this [2M]

ANALOG ELECTRONICS

(1)(a)



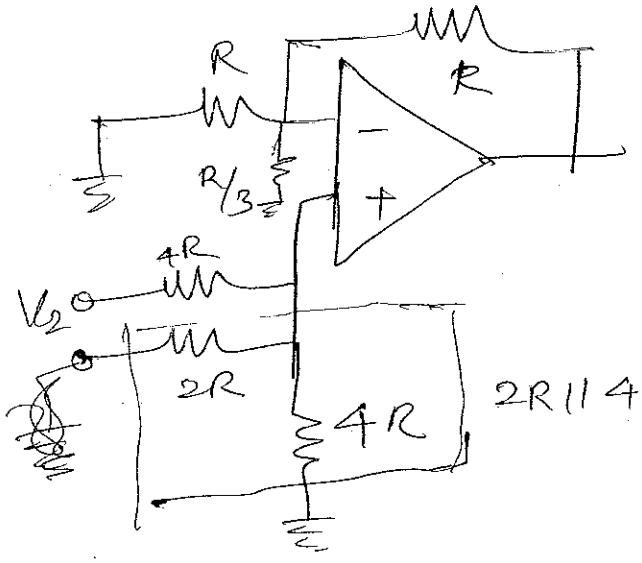
V_1 alone $V_2 = 0$ $V_3 = 0$.



$$V_{o1} = \left[1 + \frac{R}{(R/4)}\right]\left[\frac{2R}{2R+2R}\right]$$

$$= 5 \cdot \frac{1}{2} V_1 = 2.5 V_1$$

$V_1 = 0$ $V_3 = 0$.

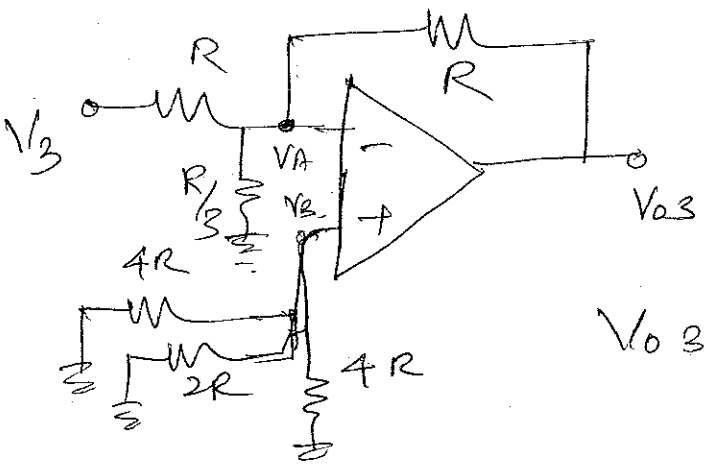


$2R \| 4R = \frac{4}{3R}$.

$$V_{02} = \left[1 + \frac{R}{(R/4)}\right]\left[\frac{4/3R}{4R + 4/3R}\right] V_2.$$

$$= 5 \cdot \frac{4/3}{16/3} = 1.25 V_2.$$

Consider V_3 alone V_1 and V_2 both zero.



$V_A = V_B = 0$.

$$V_{03} = -\frac{R}{R} V_3$$

$$= -V_3.$$

$$V_0 = V_{01} + V_{02} + V_{03}$$

$$\boxed{V_0 = 2.5V_1 + 1.25V_2 - V_3}$$

node B is at ground potential as input current of op-amp is zero. while node A is also at ground potential $V_A = V_B = 0$.

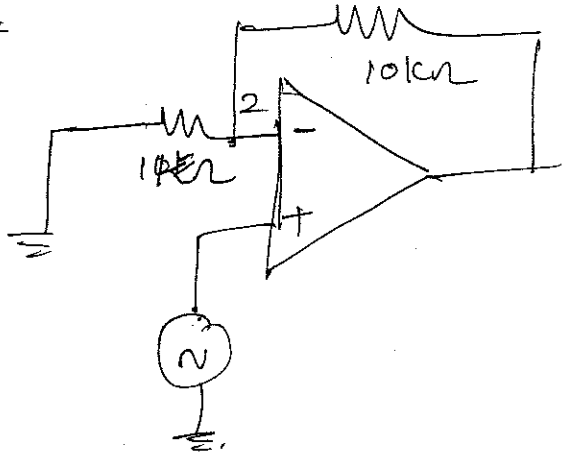
$V_0 = 2.5(2V) + 1.25(1) - 1.$

$V_0 \Rightarrow 5.25V$

——— (5M)

(1)(b)

A_f =



$A = 200,000$. $R_{in} = 2M\Omega$

$R_o = 75\Omega$. Supply voltage $= \pm 15V$.

$$A_f = \frac{A}{1+A\beta} = 10.999.$$

$$\beta \Rightarrow \frac{R_1}{R_1+R_f} = \frac{1k\Omega}{(1+10)\times 10^3} = 0.0909$$

$$A_{CL} \Rightarrow \frac{200,000}{1+200,000\times 0.0909} \Rightarrow 10.99 \approx 11.$$

—(1M)

$$R_{inf} = 2\times 10^6(1+2\times 10^6 \times 0.0909)$$

$$= 3.64\times 10^{11}\Omega \text{ (or) } 36.36G\Omega.$$

—(1M)

$$R_{of} = \frac{R_o}{1+A\beta} = 4.12M\Omega$$

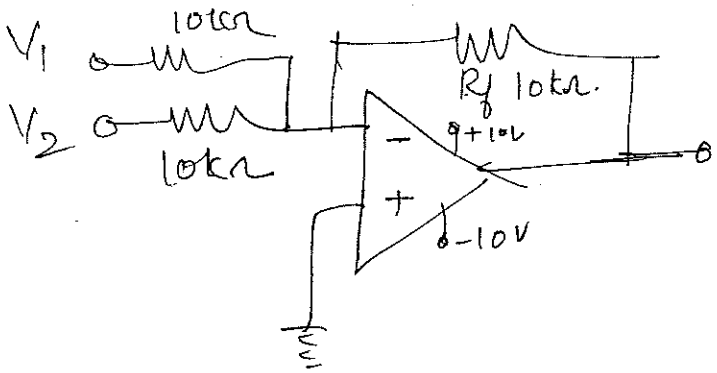
$$= 0.00412\Omega.$$

—(1M)

(1) (c). $V_0 = 2*[(V_1+V_2) - (V_3+V_4)]$

$= 2[A-B]$ ——..

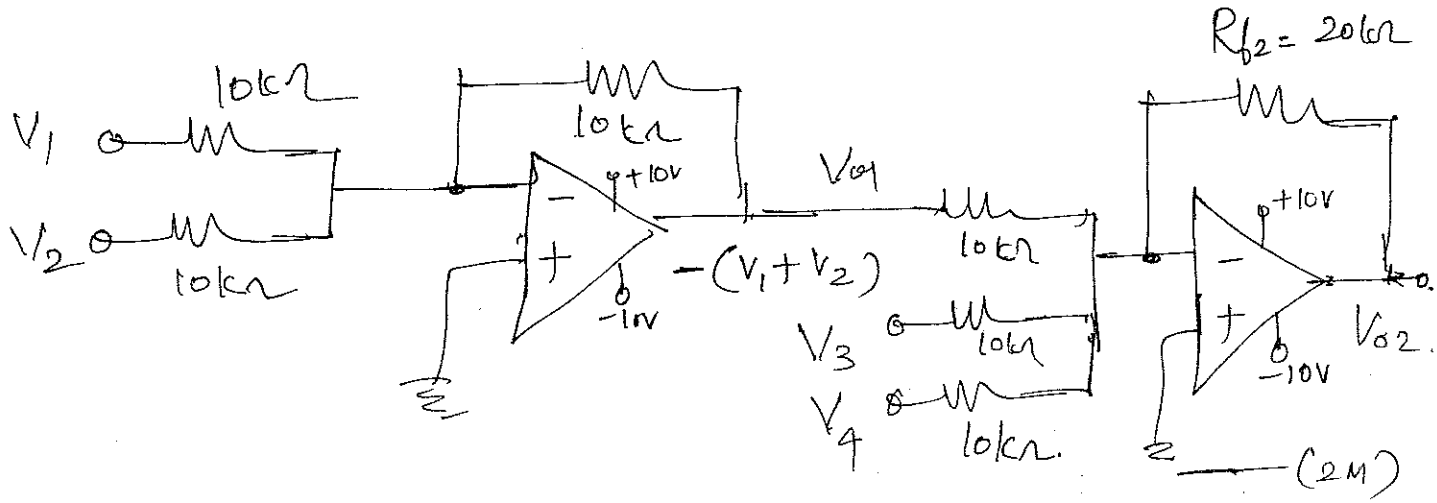
For A use an inverting op amp stage.



$-\frac{R_f}{R_1}(10k\Omega) - \frac{R_f}{R_2}V_2.$

$\Rightarrow -\frac{10k\Omega}{10k\Omega}V_1 - \frac{10k\Omega}{10k\Omega}V_2.$

$V_{01} = -(V_1+V_2)$ ——(1M)



——(2M)

$V_{02} = -\frac{R_f}{R_1}V_{01} - \frac{R_f}{R_2}V_3 - \frac{R_f}{R_3}V_4.$

$= -\frac{20k\Omega}{10k\Omega}(V_1+V_2) - \frac{20k\Omega}{10k\Omega}V_3 - \frac{20k\Omega}{10k\Omega}V_4.$

——(1M)

$\Rightarrow 2[(V_1+V_2) - (V_3+V_4)]$

Pg-5

Q2(a).

$$f_0 = \frac{1.2}{4R_1C_1} \Rightarrow \frac{1.2}{4 \times 12\times10^3 \times C_1} = 100\times10^3.$$

$$C_1 = \frac{1.2}{4\times12\times10^3\times100\times10^3} = 2.5\times10^{-10}\,F.$$

—— (2M)

$$f_L = \frac{8f_0}{V} \Rightarrow \frac{8\times100\times10^3}{[6-(-6)]}$$

$$\Rightarrow \frac{8\times100\times10^3}{12} = 66.67KHZ. \text{ —— (1M)}$$

$$f_C \Rightarrow \pm \left[\frac{f_L}{2\pi(3.6)\times10^3\times C_2}\right]^{1/2}.$$

$$\Rightarrow \pm \left[\frac{66.67\times10^3}{2\pi\times(3.6\times10^3\times C_2\times2}\right]^{1/2}$$

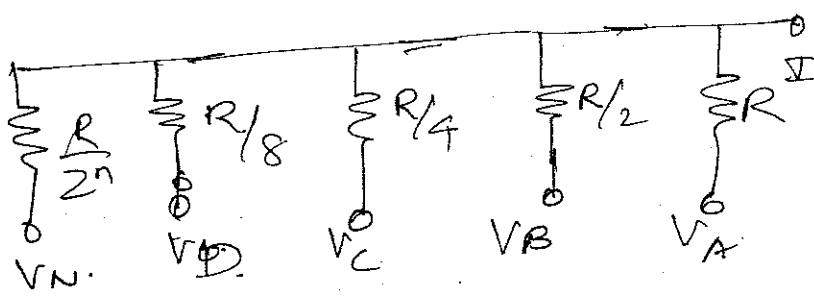
$\times10^{-6}$.

—— (2M)

$$\Rightarrow \pm 1213.97\,HZ.$$

$$\Rightarrow \pm 1.214\,KHZ.$$

(b)



$$V_{analog} \Rightarrow \frac{V_A+2V_B+4V_C+8V_D}{1+2+4+8}$$

$$I_T = \frac{V_A}{R} + \frac{V_B}{R/2} + \frac{V_C}{R/4} + \frac{V_D}{R/8} + \cdots$$

$$\Rightarrow \frac{1}{R}\left[V_A + 2V_B + 4V_C + 8V_D\right]..$$

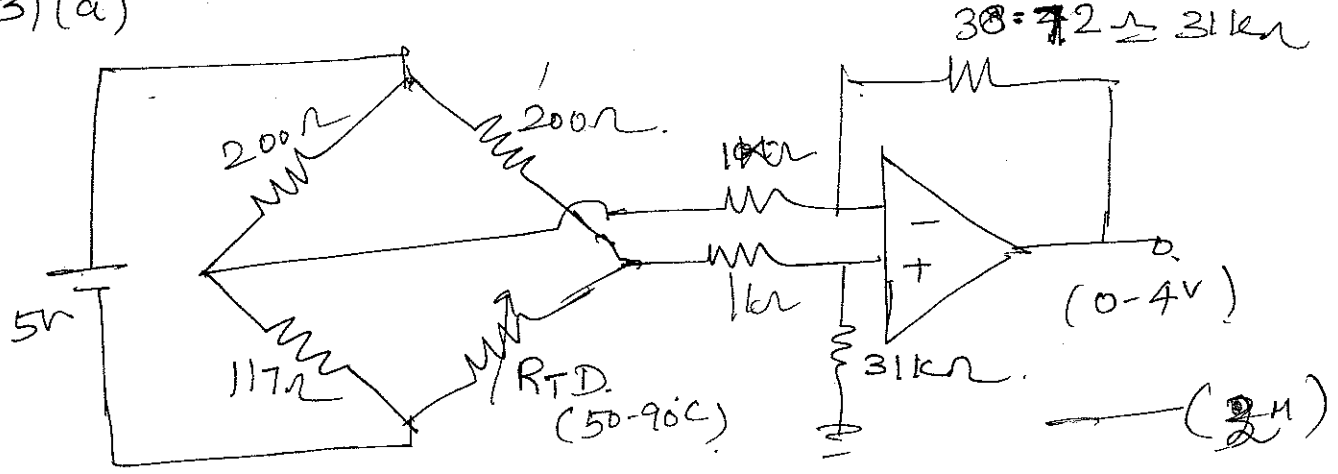
$$Req \Rightarrow \frac{1}{R} + \frac{1}{R/2} + \frac{1}{R/4} + \frac{1}{R/8} + \cdots \Rightarrow \frac{R}{1+2+4+8}.$$

Full derivation — (3M)

(c) Successive Approximation ADC.
Dual slope integrating ADC.
Half flash ADC.
Pipelined ADC.
Tracking (or) Servo ADC.
Delta-sigma ADC.

any 4 → 2M

3)(a)



$$R_t = R_0 [1 + \alpha t)$$

$$R_{50} = R_0 (1 + \alpha (\Delta t)]$$

$$= 100 \left[1 + 0.0034 (50) \right] = 117\Omega.$$

$$R_{90} = 100 \left[1 + 0.0034 (90) \right] = 130.6\Omega.$$

$$\Delta T = P/P_D = 1^\circ C. \Rightarrow \frac{30mW}{30mW} = 1^\circ C.$$

$$P = 30mW = I^2 \times R.$$

$$30 \times 10^{-3} = I^2 \times 117\Omega.$$

$$I^2 \Rightarrow I = 0.0160 A.$$

$$\Rightarrow 16mA.$$

1M

$V_{R\,50} \Rightarrow 16\times10^{-3} \times 117.$

$\Rightarrow 1.873\ V.$

$$\frac{(5 - V_{R\,50})}{I_{R_5}} = R_3.$$

$$R_3 = \frac{5 - 1.873}{16\times10^{-3}} \Rightarrow 195.41\Omega.$$

$R_3 = R_2 = 200\Omega.$ ——— (1M)

Poridge o/p at 50°C ⇒ 0V.

at 90°C ⇒

$$\Rightarrow \left[\frac{130.6}{330.6} \times 5V - \frac{117}{117+200} \times 5V\right]$$

$$\Rightarrow [1.975 - 1.845]$$

$\Rightarrow$ ——— (2M)

$\Rightarrow 0.1302V.$

Poridge output for 50-90° ⇒ 0.1302 V.

we want 5V ⇒ $\frac{5}{0.1302}$

⇒ 38.402Ω

Use R_f ⇒ 39kΩ for Practical ——— (2M)

(b)

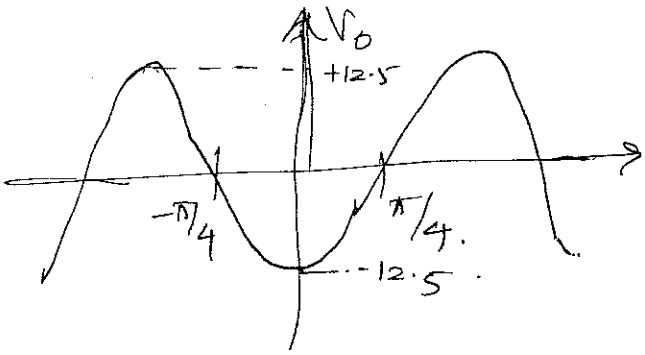
$V_i = 5 \sin \omega t$.

$V_i^2 = 25 \sin^2 \omega t$.

$\Rightarrow \frac{25}{2} [1 - \cos 2\omega t]$.

when Passed through a DC blocking Capacitor.

$V_0 = -12.5 \cos 2\omega t$.



[2M]

(4) (a)

ωt	$V_0 = -12.5 \cos 2\omega t$.
0.	-12.5
$\pi/4$	-12.5
$\pi/2$	-12.48.

4(a) (i) $V_+ = V_Z = 10V \Rightarrow V_- = 10V$ (ideal op-amp)

$$10 = \frac{V_o}{R_1+R_2} \times R_2 \quad V_o = 30V \quad \text{—— (1M)}$$

(ii) For the voltage regulator to operate with minimum V_{in} the pass transistor should be in saturation $V_{CE} = 0.2V$.

Hence $(V_{in})_{min} = 30.2$. —— (1M)

(iii) $IR_3 = \frac{30.2 - 10}{R_3} = 0.5A$

$$R_3 = \frac{20.2}{0.5A} = 40.4\Omega \quad \text{—— (2M)}$$

If the op-amp is not ideal

$$V_o = (V_+ - V_-) \times A + 0.7$$

$$V_- = \frac{V_o}{R_1+R_2} \times R_2 = \frac{V_o}{3}.$$

$$V_+ = V_Z = 10V.$$

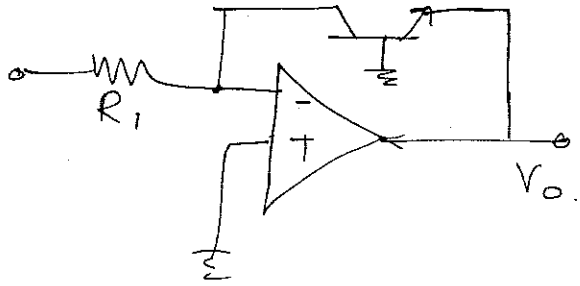
$$V_o = \left(10 - \frac{V_o}{3}\right) \times 1000 + 0.7$$

$$V_o \left[1 + \frac{1000}{3}\right] = 10^4 + 0.7$$

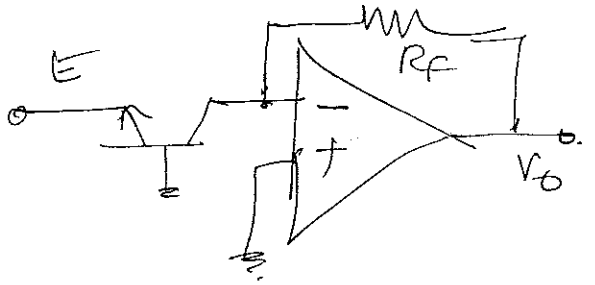
$$V_o = 29.91V.$$

V_o changes by $-0.09V$. —— (2M)

4(b)



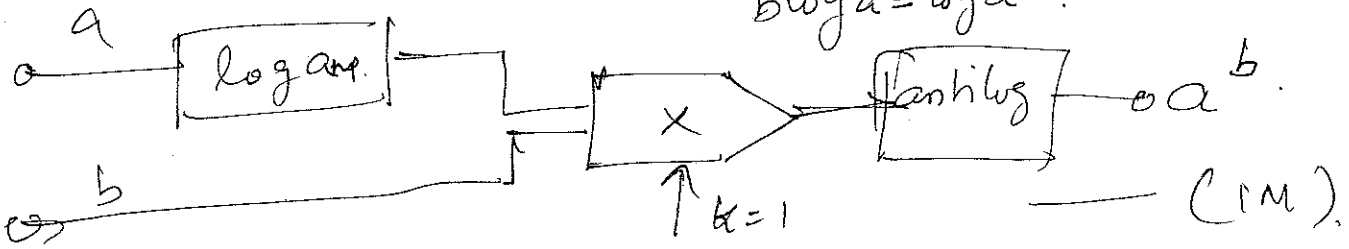
$$V_0 = -\frac{kT}{q} \ln\left(\frac{V_I}{I_S R_1}\right)$$



$$V_0 = \text{antilog}\left(\frac{-q}{KT} V_i\right) I_S R_f$$

—— (2M)

$b \log a = \log a^b$.



—— (1M).

5(a) $V_0 = +8V$ $I_L = 200mA$ $I_{SC} = 400mA$

Here output is more than 7V & I_L is more than 150mA Positive high voltage high Current regulator

$$V_0 = V_{ref}\left(\frac{R_1+R_2}{R_2}\right)$$

$$8 = 7\left(1+\frac{R_1}{R_2}\right).$$

$R_2 = 7R_1$ $R_1 = 1k\Omega$ $R_2 = 7k\Omega$. —— (2M)

$$R_{SC} = \frac{0.6}{I_{SC}} = \frac{0.6}{400\times10^{-3}} = 1.5\Omega$$ —— (1M)

$R_3 = R_1 \| R_2 = 875\Omega$. (1M)

Power wattage $R_{SC} = (I_{SC})^2 R_{SC}$.

$\Rightarrow (400 \times 10^{-3})^2 \times 1.5$.

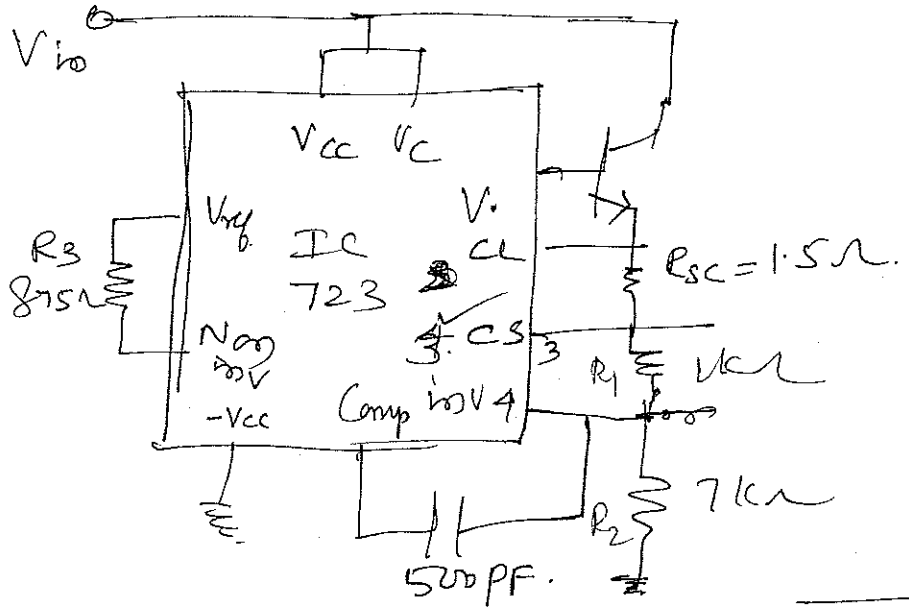
$= 0.24\,W$. ——— (1M)

$I_- = \frac{V_0}{R_1 + R_2} = \frac{8}{8 \times 10^3} = 1\,mA$.

$P_1 = I^2 R_1 = (1 \times 10^{-3})^2 \times 1 \times 10^3 = 1\,mW$.

$P_2 = I^2 R_2 = (1 \times 10^{-3})^2 \times 7 \times 10^3 = 7\,mW$. (1M)

R_1 & R_2 = 1/16th % watt power ratings. (1M)



——— 2M

(b) $i_C = (2.5)(2 + V_{in})^3\,mA$.

$= 2.5 \left[8 + 12 V_{in} + 6 V_{in}^2 + V_{in}^3 \right]$

$= 20 + 30 V_{in} + 15 V_{in}^2 + 2.5 V_{in}^3$.

5(b) $i_c = (2.3)(2+V_{in})^3$.

$\Rightarrow (2.3)\left[8 + 12V_{in} + 6V_{in}^2 + V_{in}^3\right]$

$\Rightarrow 18.4 + 27.6\,V_{in} + 13.8\,V_{in}^2 + 2.3\,V_{in}^3$.

$V_{in} = 10\sin\omega t$.

$= 18.4 + 27.6(10\sin\omega t) + 13.8\left[100 \times \left(\frac{1-\cos 2\omega t}{2}\right)\right]$

$+ 2.3(10)^3\left[\frac{3}{4}\sin\omega t - \frac{1}{4}\sin 3\omega t\right]$

$= 18.4 + 276\sin\omega t + 690 - 690\cos 2\omega t$

$+ 1725\sin\omega t - 575\sin 3\omega t$.

$= 708.4 + 2001\sin\omega t - 690\cos 2\omega t - 575\sin 3\omega t$

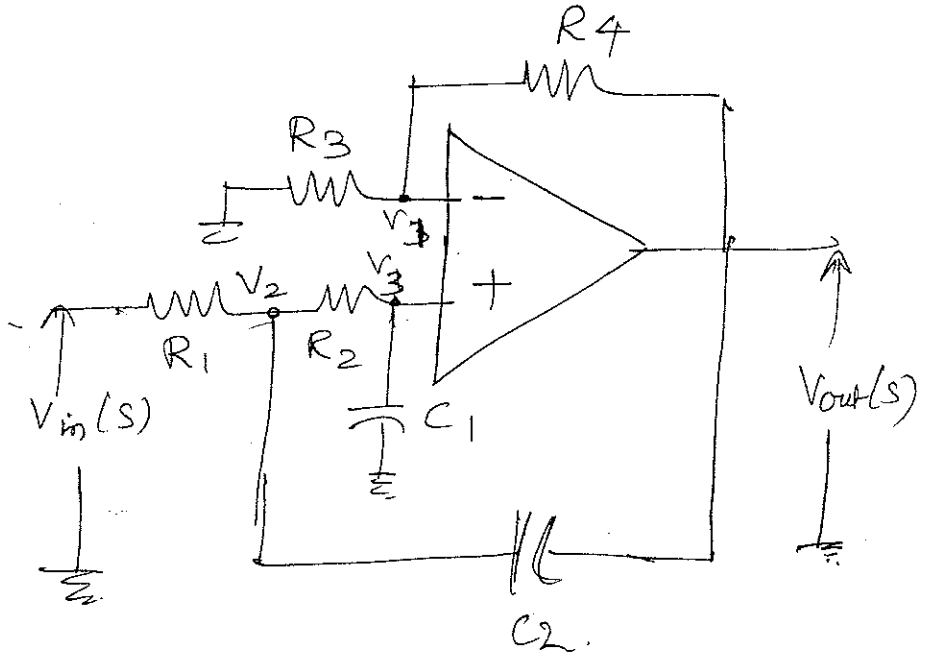
$I_{dc} = 708.4\text{ mA}$. —— (1M)

$I_{ac} = 18.4\text{ mA}$. —— (1M)

$T.H.D = \frac{\sqrt{(690)^2 + (575)^2}}{2001}$

$T.H.D = 44.88\%$. —— (3M)

b(a)



At node 1

$$\frac{V_1(s)}{R3} + \frac{V_1(s) - V_{out}(s)}{R_4} = 0.$$

$$\left(\frac{1}{R_3} + \frac{1}{R_4}\right) V_1(s) = \frac{V_{out}(s)}{R_4} \quad \text{--- Eqn (1)}$$

At node V_3 $\boxed{V_3 = V_1}$.

$$\frac{V_3(s) - V_2(s)}{R_2} + \frac{V_3(s)}{1/C_1 s} = 0. \qquad V_3(s) =$$

$$\frac{V_1(s) - V_2(s)}{R_2} + C_1 s V_3(s) = 0.$$

$$\left(\frac{1}{R_2} + C_1 s\right) V_1(s) = \frac{1}{R_2} V_2(s) \quad \text{--- eq 2}$$

At node V_2. $V_3(s) = V_1(s)$.

$$\frac{V_2(s) - V_{in}(s)}{R_1} + \frac{V_2(s) - V_1(s)}{R_2} + \frac{V_2(s) - V_{out}(s)}{1/C_2 s} = 0.$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2} + C_2 s\right) V_2(s) = \frac{V_{in}(s)}{R_1} + \frac{V_1(s)}{R_2} + C_2 s V_{out}(s)$$

--- eqn (3)

From (1)

$$\left(\frac{R_4+R_3}{R_3R_4}\right) V_1(s) = \frac{V_{out}(s)}{R_4}$$

$$V_1(s) = \frac{\frac{1}{R_4}}{\frac{R_3+R_4}{R_3R_4}} V_{out}(s)$$

$$V_1(s) = \frac{R_3}{R_3+R_4} V_{out}(s)$$

—— eqn (4)

From eqn (2)

$$V_2(s) = R_2\left[\frac{1}{R_2} + C_1 s\right] V_1(s)$$

$$= [1 + R_2 C_1 s]\, V_1(s) \quad \text{—— eqn (5)}$$

and with eqn 4 Sub $V_1(s)$ in the above eqn (5)

$$V_2(s) = [1 + R_2 C_1 s] \frac{(1/R_4)}{R_3 + R_4/R_3 R_4} V_{out}(s)$$

$$V_2(s) = \frac{R_3[1 + R_2 C_1 s]}{(R_3+R_4)} V_{out}(s)$$

—— eqn (6)

~~By sub (4) & (5)~~

Sub eqn (4) & eqn (6) in eqn (3).

$$\Rightarrow \left(\frac{1}{R_1}+\frac{1}{R_2}+C_2 s\right)\frac{R_3(1+R_2C_1 s)}{(R_3+R_4)}V_{out}(s)$$

$$\Rightarrow\left[\left(\frac{1}{R_1}+\frac{1}{R_2}+C_2 s\right)\cdot\frac{R_3(1+R_2C_1 s)}{R_3+R_4}-\frac{1}{R_2}\cdot\frac{R_3}{R_3+R_4}-C_2 s\right]V_{out}(s)$$

$$=\frac{1}{R_1}V_{in}(s)$$

$$\frac{V_{out}(s)}{V_{in}(s)}=\frac{1}{R_1\left[\left(\frac{1}{R_1}+\frac{1}{R_2}+C_2 s\right)\frac{R_3(1+R_2C_1 s)}{R_3+R_4}-\frac{1}{R_2}\cdot\frac{R_3}{R_3+R_4}-C_2 s\right]}$$

$$G(s)=\frac{7.83\times10^{7}}{s^2+1.77\times10^{4}s+5.87\times10^{7}}$$

(8M)

6(b) Positive feedback in oscillator circuits is always phase shifted.

Positive feedback in Comparator circuits has no phase shift at all being direct Coupled.

(2M)

BITS, PILANI – DUBAI
SECOND SEMESTER 2012 – 2013
THIRD YEAR – ECE

Course Code: ECE C364 | Date: 6.05.2013
Course Title: Analog Electronics | Max Marks: 30
Duration: 50 Minutes | Weightage: 15%
Component: Test II (Open Book)

Note: This question paper has 4 questions and 2 pages. Answer all Questions. Semi log graph sheet is provided along with question Paper. Assume suitable data if required

Q1 The cut off frequency of a certain second order Butterworth low pass filter is **2KHZ**.Assume all the capacitor values to be **0.01μF** and feedback resistance R_f connected between pin2 and pin6 of op amp as **15.83kΩ.**Draw a schematic of the circuit and determine suitable values of all resistors used in the filter design. Also draw the frequency response of the filter by expressing gain in decibels for frequencies of 100Hz, 200Hz, 1000Hz, 2000Hz and 10,000Hz and find cut off frequency from the frequency response plot.

(10 Marks)

Q2 Draw a schematic of an op amp based RC phase shift oscillator. The phase shifting network is made of 3 identical RC sections. The op amp has a maximum input bias current of $\mathbf{I_b=50nA}$. Assume that the maximum current through the feedback resistor $R_f = \mathbf{100I_b}$ and the supply voltage for op amp is **12V**. Design the oscillator circuit for an output frequency of **2KHZ.** Determine all component values required. (7 Marks)

P.T.O

Q3 Design an IC555 timer circuit such that a control door is set to open for duration of **0.7msec** after a trigger signal is received. The dc voltage available for the IC is **15volts**.Assume a charging capacitor of **0.1μF**.Draw the complete circuit diagram and determine all external component values used. Modify the above circuit such that the **0.7msec** opening of the door is repeated after every **0.23msec**. Determine the values of any additional components used. (7 Marks)

Q4 Design a full wave precision rectifier using **three** op amps and draw the necessary waveforms at the output of each op amp. Assume $\mathbf{V_{in}}$ **= 4Vp-p** sinusoidal input with frequency of 1KHZ. (6 Marks)

****

Answering Scheme

Test - 2

BITS, PILANI – DUBAI
SECOND SEMESTER 2012 – 2013
THIRD YEAR – ECE

Course Code: ECE C364 | Date: 6.05.2013
Course Title: Analog Electronics | Max Marks: 30
Duration: 50 Minutes | Weightage: 15%
Component: Test II (Open Book)

Note: This question paper has 4 questions and 2 pages. Answer all Questions. Semi log graph sheet is provided along with question Paper. Assume suitable data if required

Q1 The cut off frequency of a certain second order Butterworth low pass filter is **2KHZ**.Assume all the capacitor values to be **0.01μF** and feedback resistance R_f connected between pin2 and pin6 of op amp as **15.83kΩ.**Draw a schematic of the circuit and determine suitable values of all resistors used in the filter design. Also draw the frequency response of the filter by expressing gain in decibels for frequencies of 100Hz, 200Hz, 1000Hz, 2000Hz and 10,000Hz and find cut off frequency from the frequency response plot. (10 Marks)

2M

freq	gain in dB
100	4.000
200	4.006
1KHz	3.743
2KHz	0.995
4KHz	-28.96

gain in mag

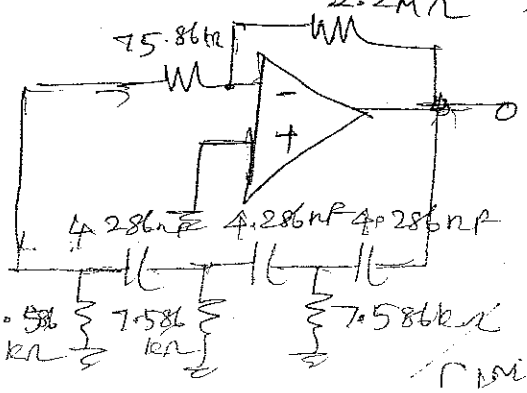
1.586
1.586
1.538
1.121
0.063

CKT diag → [1M]
R = 7.957 ≈ 7.96kΩ [1M]
R_1 = 27.013kΩ [1M]
values [2M] → from graph ⇒ 2kHz
cut off freq → (3M)

Q2 Draw a schematic of an op amp based RC phase shift oscillator. The phase shifting network is made of 3 identical RC sections. The op amp has a maximum input bias current of I_b=**50nA**. Assume that the maximum current through the feedback resistor R_f = **100I_b** and the supply voltage for op amp is **12V**. Design the oscillator circuit for an output frequency of **2KHZ.** Determine all component values required. (7 Marks)

R_f = 2.2MΩ [1M]
R_1 = 75.86kΩ [1M] R = 7.586kΩ [1M]

P.T.O

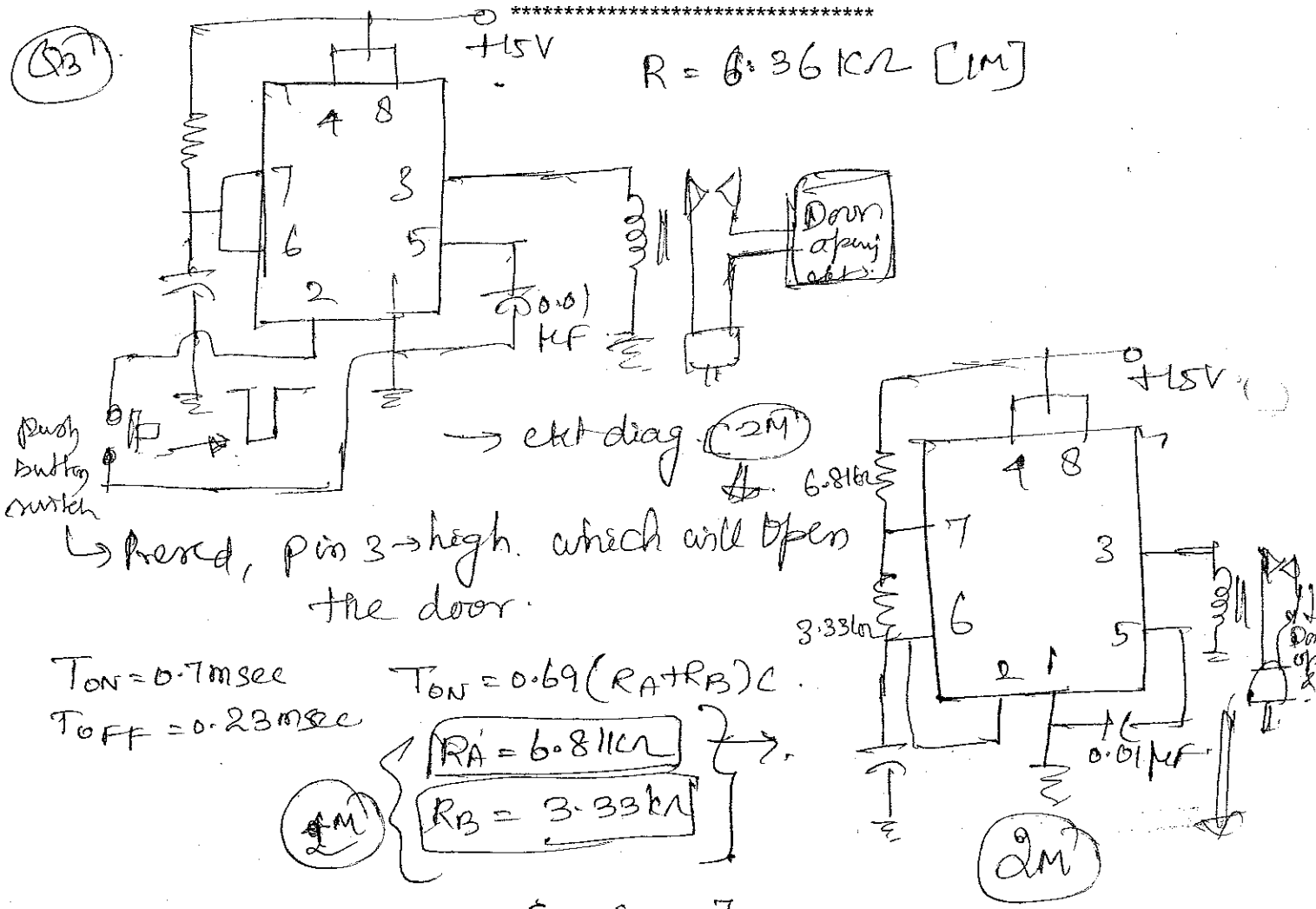


C = 4.33nF (or) = 4.286nF (3M)

[1M]

Q3 Design an IC555 timer circuit such that a control door is set to open for duration of **0.7msec** after a trigger signal is received. The dc voltage available for the IC is **15volts**.Assume a charging capacitor of **0.1μF**.Draw the complete circuit diagram and determine all external component values used. Modify the above circuit such that the **0.7msec** opening of the door is repeated after every **0.23msec**. Determine the values of any additional components used. (7 Marks)

Q4 Design a full wave precision rectifier using **three** op amps and draw the necessary waveforms at the output of each op amp. Assume V_{in} **= 4Vp-p** sinusoidal input with frequency of 1KHZ. (6 Marks)

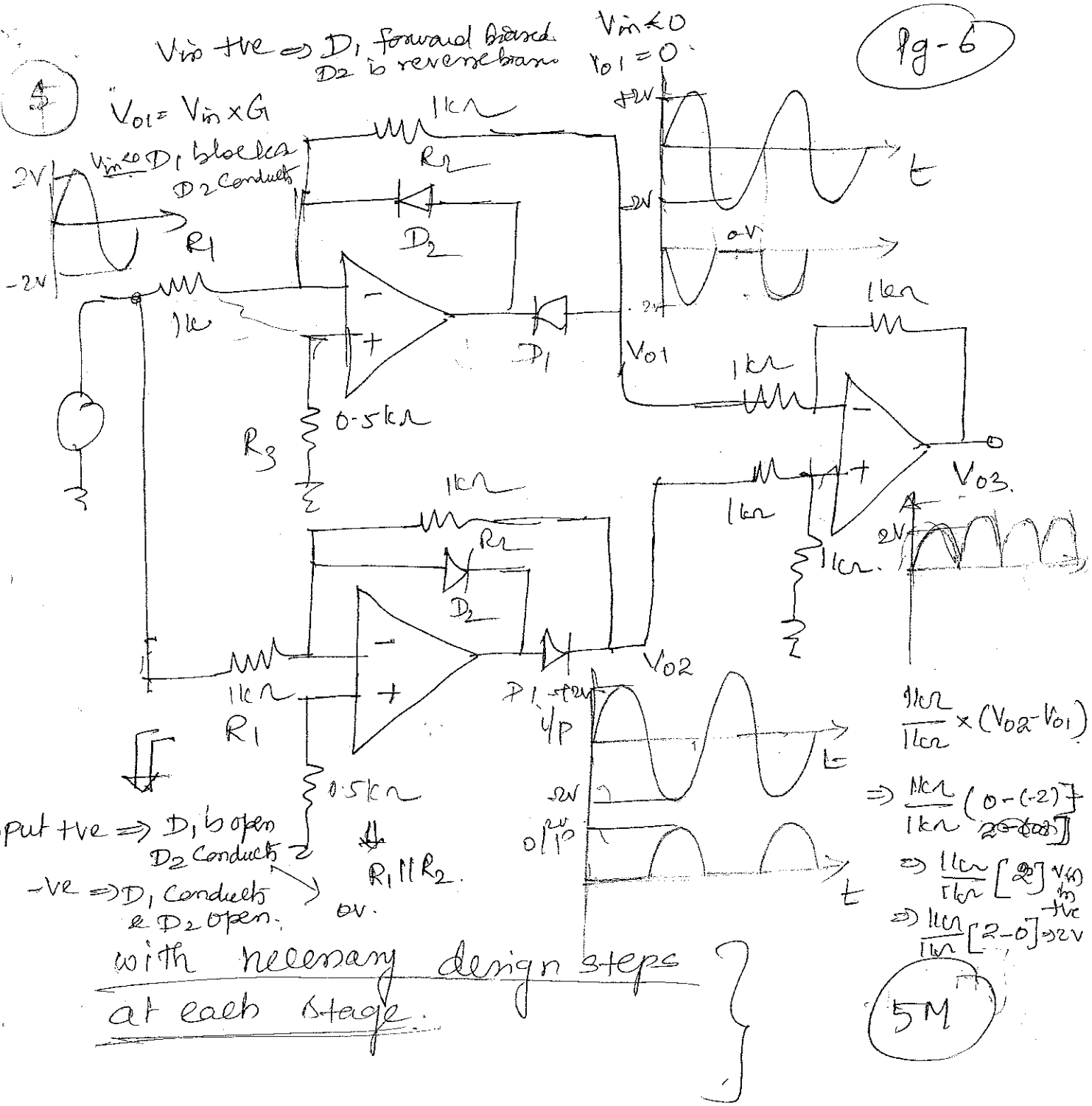


5

$V_{o1} = V_{in} \times G$

Vin +ve ⇒ D_1 forward biased, D_2 is reverse biased

$V_{in} < 0$, $V_{o1} = 0$



Input +ve ⇒ D_1 is open, D_2 conducts

-ve ⇒ D_1 conducts & D_2 open.

0V.

$\frac{1k\Omega}{1k\Omega} \times (V_{o2} - V_{o1})$

$\Rightarrow \frac{1k\Omega}{1k\Omega}(0-(-2))$

$\Rightarrow \frac{1k\Omega}{1k\Omega}[2]$ V_{in} to +ve

$\Rightarrow \frac{1k\Omega}{1k\Omega}[2-0] \Rightarrow 2V$

with necessary design steps at each stage.

5M

$R_1 = 1k\Omega$ $R_2 = 1k\Omega$.

$R_3 \Rightarrow R_1 \| R_2 \Rightarrow$ To minimize input bias current.

R_1 & R_2 based on application betn 1kΩ & 100kΩ

$G = -\frac{R_2}{R_1} \Rightarrow -\frac{1k\Omega}{1k\Omega} \times 4V \Rightarrow -4V_{p-p}$.

$R_3 \Rightarrow R_1 \| R_2 \Rightarrow \frac{1k\Omega \times 1k\Omega}{1k\Omega + 1k\Omega} = 0.5$

BITS, PILANI – DUBAI CAMPUS

SECOND SEMESTER 2012-2013

THIRD YEAR ECE

TEST1 (CLOSED BOOK)

Course Code: ECE C364 Date: 18.03.2013

Course Title: ANALOG ELECTRONICS Weightage:15%

Duration:50Minutes Max Marks: 30

Note: This question paper has **2 Pages** & **6 questions**. Answer all questions.

---

1. Draw the necessary circuit diagram for differentiator circuit and find out the output voltage if a sinusoidal voltage of peak value 6mV and frequency of 1KHZ is applied to the input of a differentiator circuit. Consider feedback resistor R_F =56KΩ and C = 1μF. Sketch the input and output waveforms. [5M]

2. A common emitter npn transistor has β =80.The collector terminal is connected to a 10V power supply through a resistor R_c=5KΩ.A dc bias of 1V is applied to the base terminal through a resistor R_B=2KΩ&the emitter terminal is connected to ground through an emitter resistor 1KΩ.The transistor is in the active mode of operation. Assume V_{BE} =0.7V.Draw the necessary circuit diagram and determine I_C, I_B& V_{CE}. [5M]

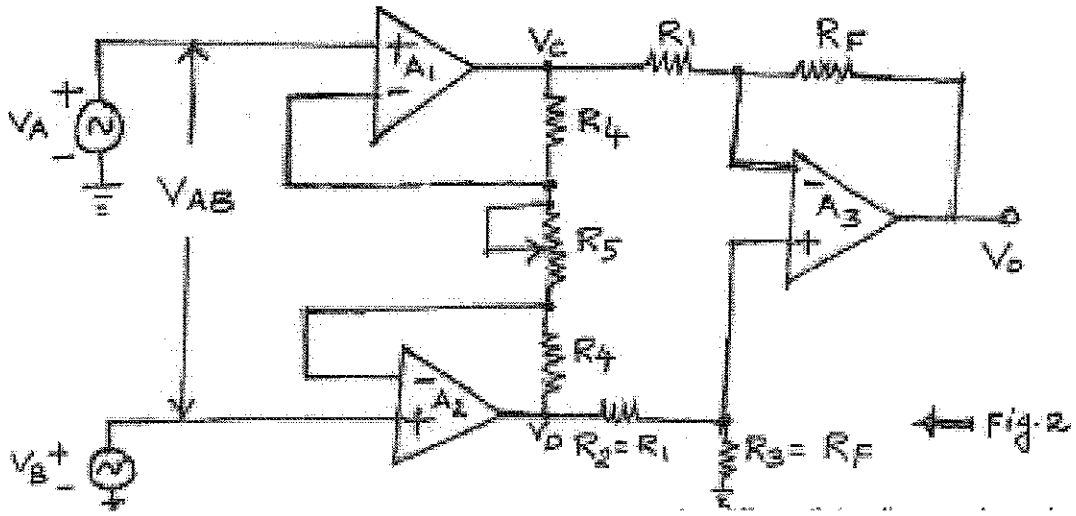
3. An amplifier has open loop gain A=60dB and output impedance Z_o = 8kΩ.A negative feedback when provided to this amplifier modifies its output impedance to Z_{of} =500Ω. Determine the feedback factor. [5M]

4. Design a suitable circuit using **three** ideal op amps and resistors to implement the following expression:

$$V_o = (2v_1 + v_2 - 4v_3)$$

Where $V_o$is the output voltage&$+v_1$, $+v_2$and$+v_3$are dc inputs. [5M]

5. For the circuit shown in Fig.2, design suitable values of resistors (R_4,$R_{5min}$and R_{5max}) tohave variable differential gain in the range of 5 to 200. Use R_5 as 50KΩ potentiometer. Assume R_F =R_1=10KΩ. [5M]



6. For the circuit shown in Fig.3, derive an expression for differential voltage gain and comment on your answer. [5M]

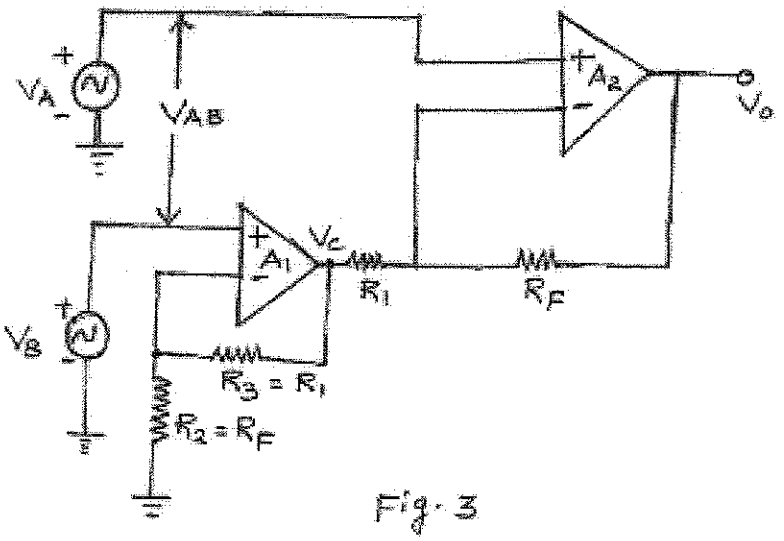


Fig. 3

.....END OF PAPER.....

ANSWERING SCHEME

Qn(5)

$$|A_D| = \left[1 + \frac{2R_4}{R_5}\right]\left[\frac{R_F}{R_1}\right] \longrightarrow (1M)$$

Given $R_5 = 50k\Omega$ potentiometer

$R_F = R_1 = 10k\Omega$.

$$\frac{V_0}{V_B - V_A} = \left[1 + \frac{2R_4}{R_5}\right]\left[\frac{R_F}{R_1}\right]$$

$$A_D = 1 + \frac{2R_4}{R_5}.$$

$$A_{D\,min} = 1 + \frac{2R_4}{R_{5max}}.$$

$$5 = 1 + \frac{2R_4}{50k\Omega}.$$

$$50k\Omega \times 5 = 50k\Omega + 2R_4$$

$$2R_4 = 200{,}000$$

$$\boxed{R_4 = 100k\Omega} \longrightarrow (2M)$$

$$A_{D\,max} = 1 + \frac{2R_4}{R_{5\,min}}.$$

$$200 = 1 + \frac{2 \times 100 \times 10^3}{R_{5\,min}}.$$

$$(200)R_{5\,min} = 1 + 200 \times 10^3.$$

$$\boxed{R_{5\,min} = 1k\Omega.} \quad \text{——— (1M)}$$

$$R_{5\,max} = 50k\Omega \quad \text{——— (1M)}$$

Qn b (5)

First stage → non inverting amplifier

$$V_C = \left[1 + \frac{R_3}{R_2}\right] V_B \quad \text{——— eqn 1}$$

Second stage – difference amplifier.

apply superposition Principle

with V_A acting alone $V_C = 0$.

$$V_{OA} = \left[1 + \frac{R_F}{R_1}\right] V_A \quad \text{——— eq 2.}$$

V_B acting alone

$$V_{OB} = -\frac{R_F}{R_1} V_C. \qquad \frac{R_2}{R_2+R_3}$$

$$V_O = V_{OA} + V_{OB}.$$

$$\Rightarrow \left[1 + \frac{R_F}{R_1}\right] V_A - \frac{R_F}{R_1} V_C.$$

$$\Rightarrow -\frac{R_F}{R_1} \times \frac{R_2}{R_2} \left[1 + \frac{R_3}{R_2}\right] V_B + \left[1 + \frac{R_F}{R_1}\right] V_A.$$

$R_1 = R_3 \quad R_2 = R_F.$

$$\Rightarrow -\frac{R_F}{R_3} \left[\frac{R_F + R_3}{R_1 R_F}\right] V_B + \left[1 + \frac{R_F}{R_1}\right] V_A.$$

$$\Rightarrow -\frac{R_F}{R_1} \left[\frac{R_2 + R_3}{R_2}\right] V_B + \left[1 + \frac{R_F}{R_1}\right] V_A.$$

$$\Rightarrow -\frac{R_F [R_F + R_1]}{R_1 R_F} V_B + \left(1 + \frac{R_F}{R_1}\right) V_A.$$

$$\Rightarrow \quad -\frac{R_F^2 + R_F R_1}{R_1 R_F} V_B + \left(1 + \frac{R_F}{R_1}\right) V_A .$$

$$\Rightarrow \quad -\left(\frac{R_F}{R_1} + 1\right) V_B + \left(1 + \frac{R_F}{R_1}\right) V_A .$$

$$V_o \Rightarrow \left(1 + \frac{R_F}{R_1}\right)(V_A - V_B)$$

$$\boxed{\frac{V_o}{(V_A - V_B)} = 1 + \frac{R_F}{R_1}}$$

Differential voltage gain for a difference amplifier with two op-amps will be same as that obtained for the non-inverting amplifier.

(3) (11)

$V_i(t) = V_m \sin \omega t$.

$V_m \Rightarrow 6mV$. $R_f = 56k\Omega$ $C = 1\mu F$.

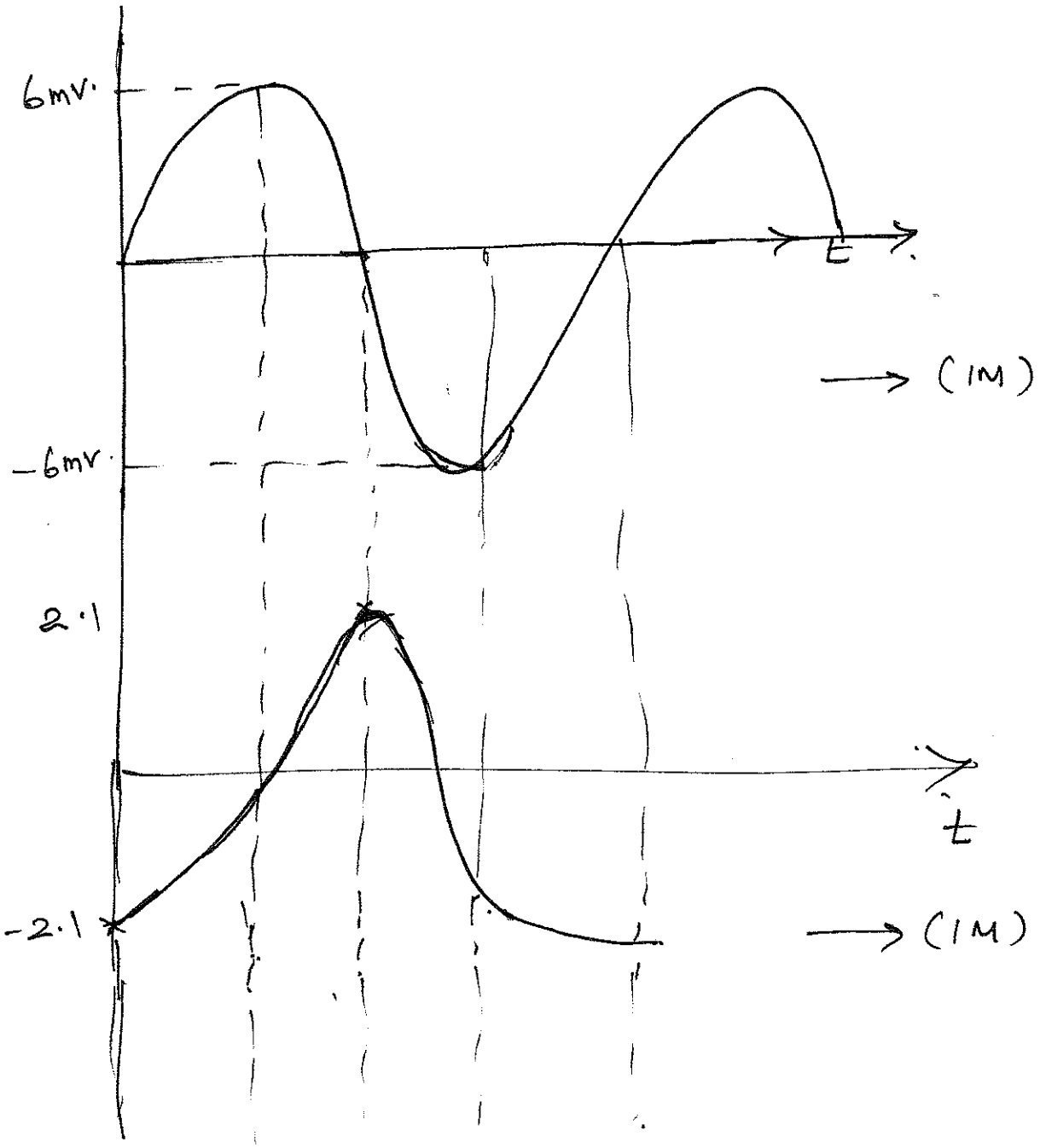
$$V_o = -R_F C_1 \frac{d}{dt} V_i(t). \qquad \text{——— (1M)}$$

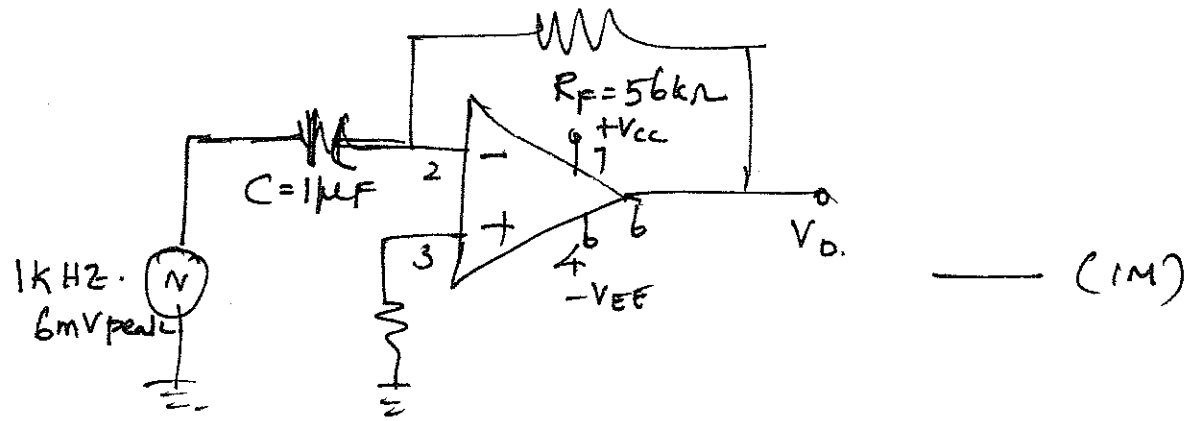
$$\Rightarrow -56 \times 10^3 \times 1 \times 10^{-6} \frac{d}{dt} \left[6 \times 10^{-3} \sin (2\pi \times 1000) t\right]$$

$$\Rightarrow -56 \times 10^{-3} \times 10^{-6} \times 6 \times 10^{-3} \frac{d}{dt} \sin(2000\pi) t$$

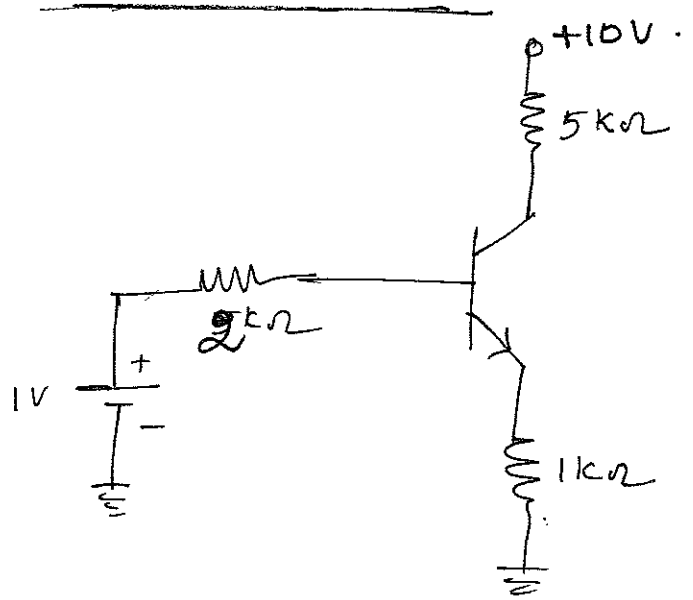
$$\Rightarrow -336 \times 10^{-6} \cos(2000\pi) t \times 2000 \times \pi .$$

$$\Rightarrow 2.11 \cos(2000\pi t) \qquad \text{——— (2M)}$$


6mV.
E
(1M)
-6mV.
2.1
t
-2.1
(1M)


$R_F = 56k\Omega$
+Vcc
7
C = 1μF
2
3
6
4
V_O.
1kHz.
6mVpeak
-VEE
(1M)

(2) Given $\beta = 80$.



⟶ (1M)

~~$1 = 0.7 \Rightarrow$~~

~~$I = 1\times10^{3} \times (101)$~~

$1 = 1\times10^{3} \times (81 + 1) V_{BE} + I_B \times 2\times10^{3}$.

$(1-0.7) = \left[1\times10^{3}\times 81 + 2\times10^{3}\right] I_B$.

$$I_B = \frac{0.3}{1\times10^{3}\times 81 + 2\times10^{3}}$$

$I_B = 3.614 \times 10^{-6}$ A.

$\boxed{I_B = 3.614\ \mu A}$ ——— (1M)

$I_C = \beta I_B = 80 \times 3.614 \times 10^{-6}$.

$\boxed{I_C = 2.8915\times10^{-4} A}$ ——— (1M)

$V_E = I_E R_E = (\beta+1) I_B \times R_E$

$= (81) \times 3.614\times10^{-6} \times 1\times10^{3}$.

$\boxed{V_E = 0.293\ V}$ ——— (½M)

$$V_C = 10 - I_C R_C$$

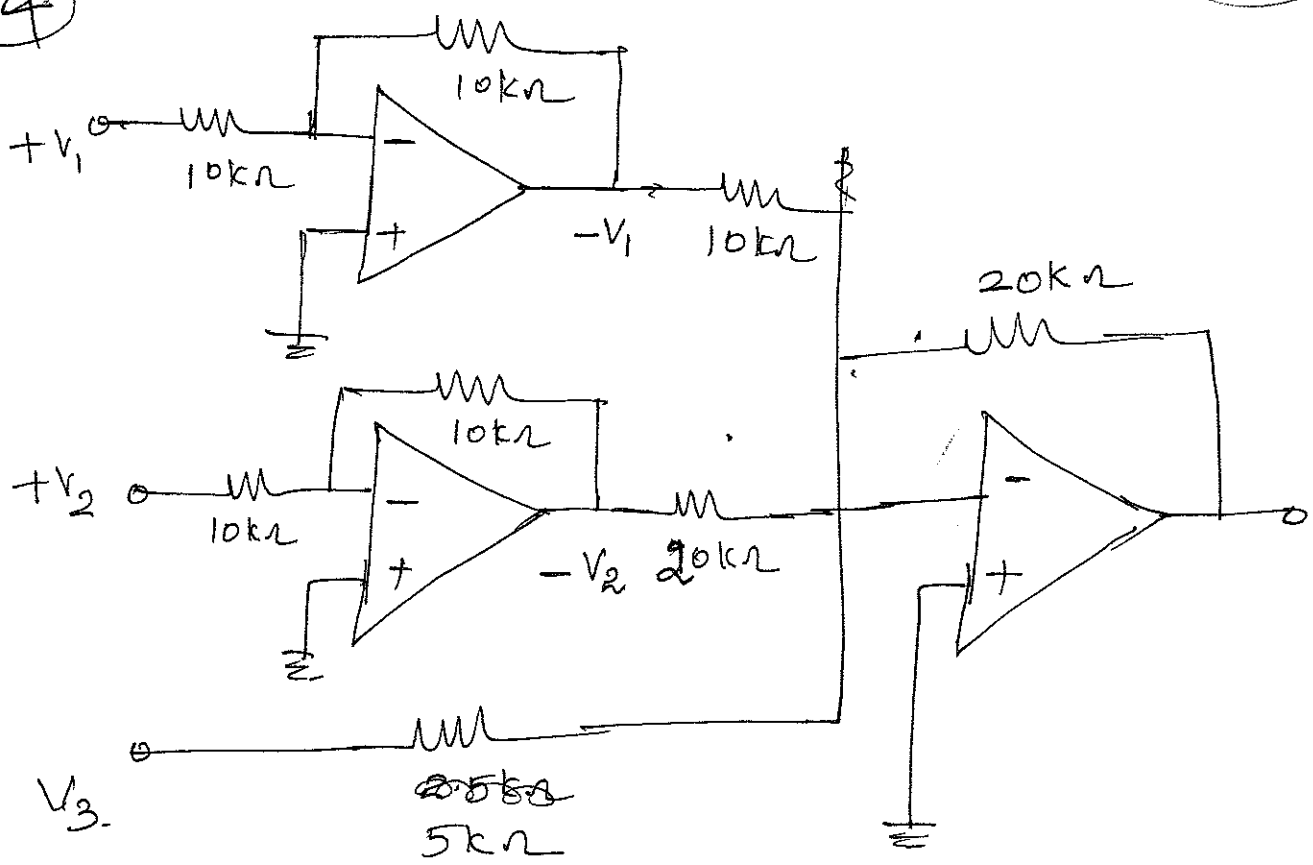
$$= 10 - 2.8915 \times 10^{-4} \times 5 \times 10^3.$$

$$= 8.5543 V. \quad \text{——— (M)}$$

$$V_{CE} = V_C - V_E \quad \text{——— (M)}$$

$$V_{CE} = 8.2613 V$$

(4)



⟶ (4M)

$$V_o \Rightarrow \frac{-20k\Omega}{10k\Omega}(+V_1) - \frac{20k\Omega}{20k\Omega}(-V_2) - \frac{20k\Omega}{5k\Omega}V_3$$

$$\Rightarrow (2V_1 + V_2 - 4V_3) \longrightarrow (1M)$$

Hence the design is achieved

Qn 3

Gain in $dB = 60$

$Z_o = 8k\Omega \qquad Z_{of} = 500\Omega$

$$60 = 20\log_{10} A$$

$$A = 10^3 = 1000.$$

$$Z_o = 8k\Omega$$

$$Z_{of} = \frac{Z_o}{1 + AZ}$$

$$5\Omega = \frac{8,000}{1 + (1000)\beta}$$

$$(1 + 1000\beta)\,5\Omega = 8,000$$

$$\boxed{\beta = 0.015} \longrightarrow (5M)$$

BITS, PILANI – DUBAI

Version A

SECOND SEMESTER 2012-2013

THIRD YEAR ECE

Course Code: ECE C364
Course Title: ANALOG ELECTRONICS
Duration:20minutes Quiz2(Closed Book)

Date:15.04.2013
Weightage:7%
Max Marks: 14

Name: ..... **ID No:** ..... **Sec / Prog:** .....

Instructions: Write your answers in the blank space provided after each question. This question paper has 5 questions. Answer all questions.

1. (a) For the Schmitt trigger circuit shown in figure 1, Calculate the upper and lower threshold voltage levels. Assume $\pm V_{sat} = \pm 13V$, and V_{in}=10Vp-p sinusoidal waveform. Also draw the necessary input and output waveforms. Show clear steps in calculation Part.
   (b) Why hysteresis is desirable in a Schmitt trigger? Write only valid key point in your Answer [5M]

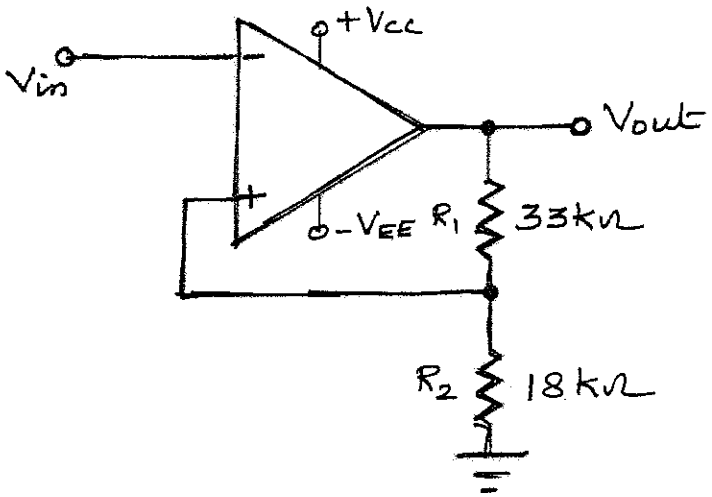


Figure 1

2. For the circuit shown in Figure 2 ,answer the following questions:
   (i) Sketch an input and output waveforms. Assume V_{IN}=2V peak sinusoidal of frequency 1KHZ.
   (ii) Sketch the Transfer characteristics
   (iii) What is the use of resistor R_3? Write only key points in your answer. [3M]

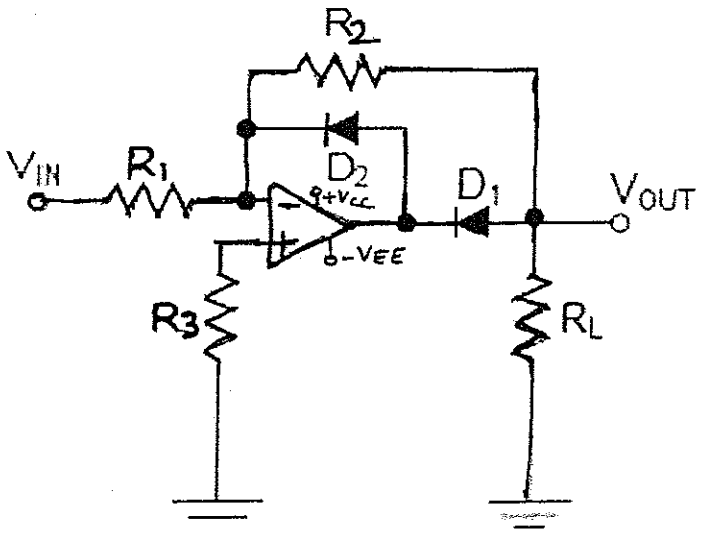


Figure 2

3. Determine the output voltages and sketch the transfer characteristics of logarithmic amplifier when input voltages of +1V, +5V and +10V are applied. Assume saturation current of transistor as 3.3×10^{-14} A. & thermal voltage as 26mV at room temperature. Consider input resistance connected to pin 2 of op amp as 100kΩ. [2M]

4. What is the purpose of using logarithmic amplifiers and analog multipliers with respect to signal processing? Write only key points in your answer. [2M]

5. Draw a suitable circuit diagram using op amp such that when input given in Fig.3(a) is applied, it should produce the output waveform given in Fig.3(b). [2M]

ANSWER :

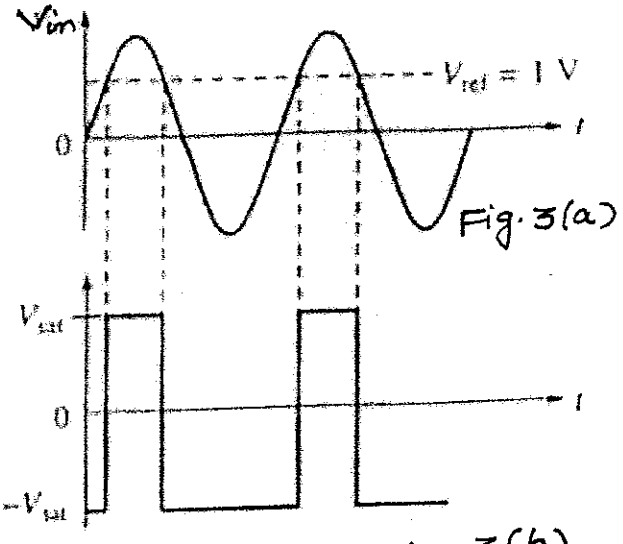


Fig. 3(a)

Fig. 3(b)

BITS, PILANI – DUBAI

Version B

SECOND SEMESTER 2012-2013

THIRD YEAR ECE

Course Code: ECE C364
Course Title: ANALOG ELECTRONICS
Duration:20minutes **Quiz 2(Closed Book)**

Date: 15.04.2013
Weightage:7%
Max Marks: 14

Name: ..... **ID No:** ..... **Sec / Prog:** .....

Instructions: Write your answers in the blank space provided after each question. This question paper has 5 questions. Answer all questions.

1. For the circuit shown in Figure 1 ,answer the following questions:
   (i) Sketch an input and output waveforms. Assume V_{IN}=2V peak sinusoidal of frequency 1KHZ.
   (ii) Sketch the Transfer characteristics
   (iii) What is the use of resistor R_3? Write only key points in your answer [3M]

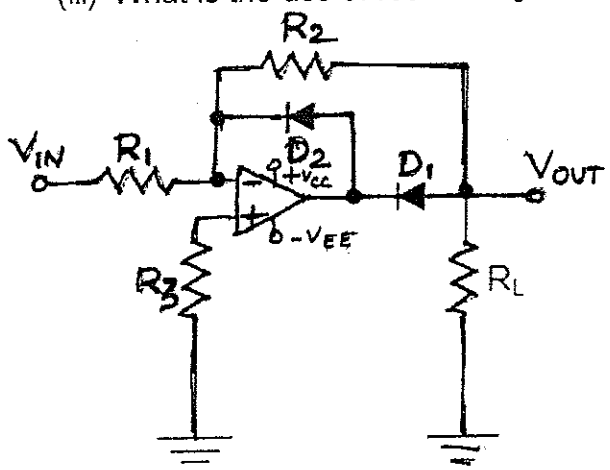


Figure 1

2. Draw a suitable circuit diagram using op amp such that when input given in Fig2(a) is applied, it should produce the output waveform given in Fig.2(b). [2M]

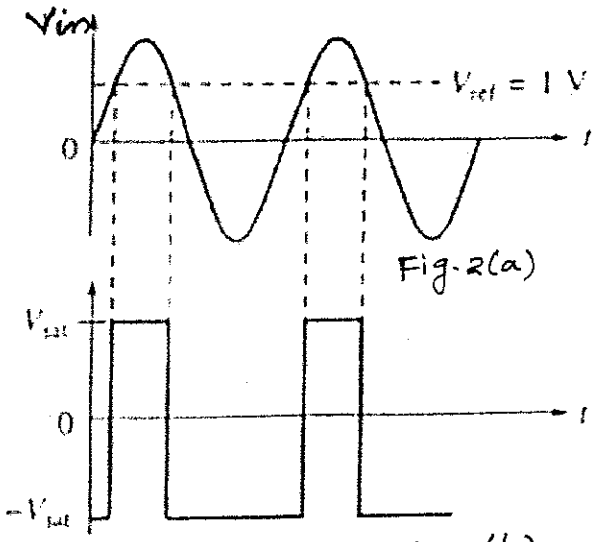


Fig.2(a)

Fig.2(b)

3. What is the purpose of using logarithmic amplifiers and analog multipliers with respect to signal processing? Write only key points in your answer. [2M]

4. Determine the output voltages and sketch the transfer characteristics of logarithmic amplifier when input voltages of +2V, +4V and +9V are applied. Assume saturation current of transistor as 3.3×10^{-14}A & thermal voltage as 26mV at room temperature. Consider input resistance connected to pin 2 of op amp as 100kΩ. [2M]

5 (a) For the Schmitt trigger circuit shown in Figure 3, Calculate the upper and lower threshold voltage levels. Assume $\pm V_{sat}=\pm 11V$ and $V_{in}=10V_{p-p}$ sinusoidal waveform. Also draw the necessary input and output waveforms. Show clear steps in calculation part.

(b) Why hysteresis is desirable in a Schmitt trigger? Write only valid key point in your answer [5M]

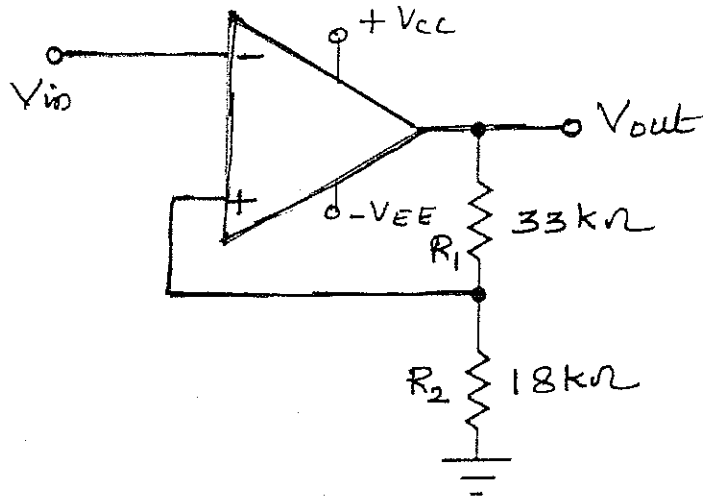


Figure 3

qu:3-2

Answering scheme.

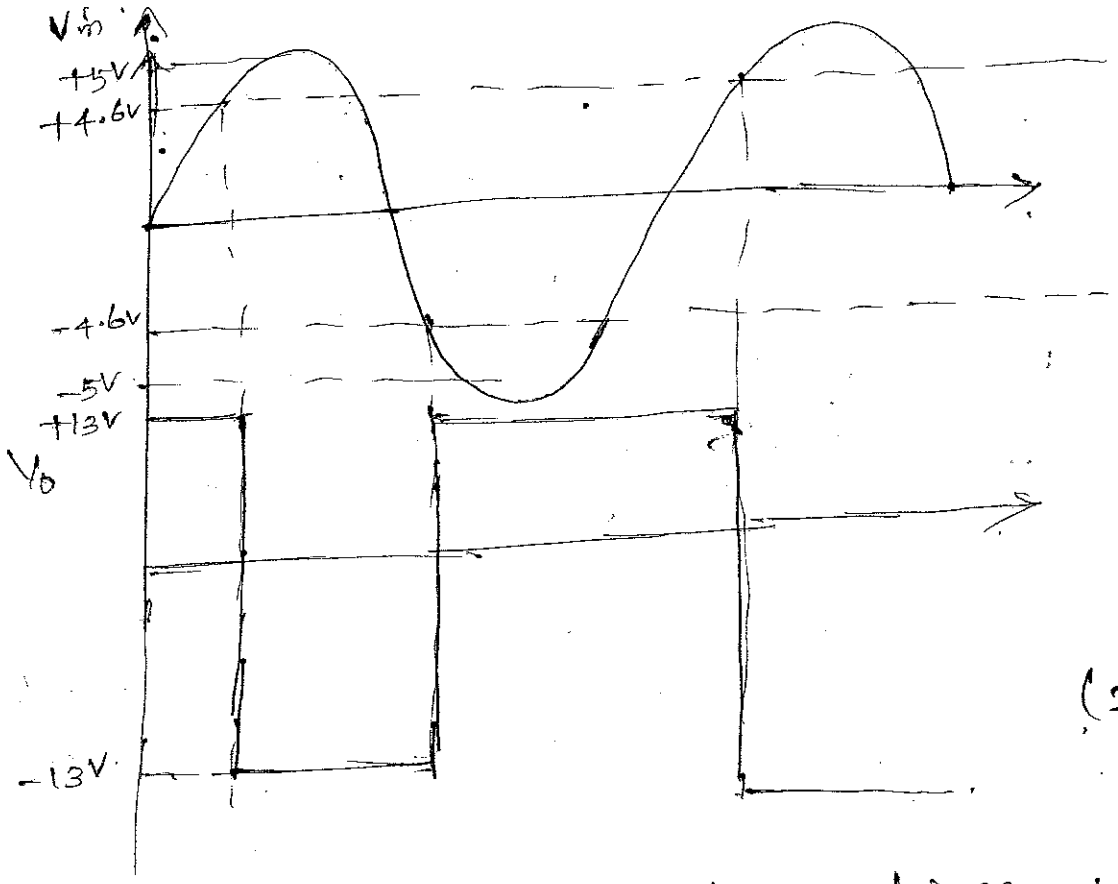
Version A

(1) $V_{UT} = \frac{R_2}{R_1 + R_2} \times V_{sat}$

$= \frac{18\,k\Omega}{18 + 33} \times (13V)$

$= 4.59V$

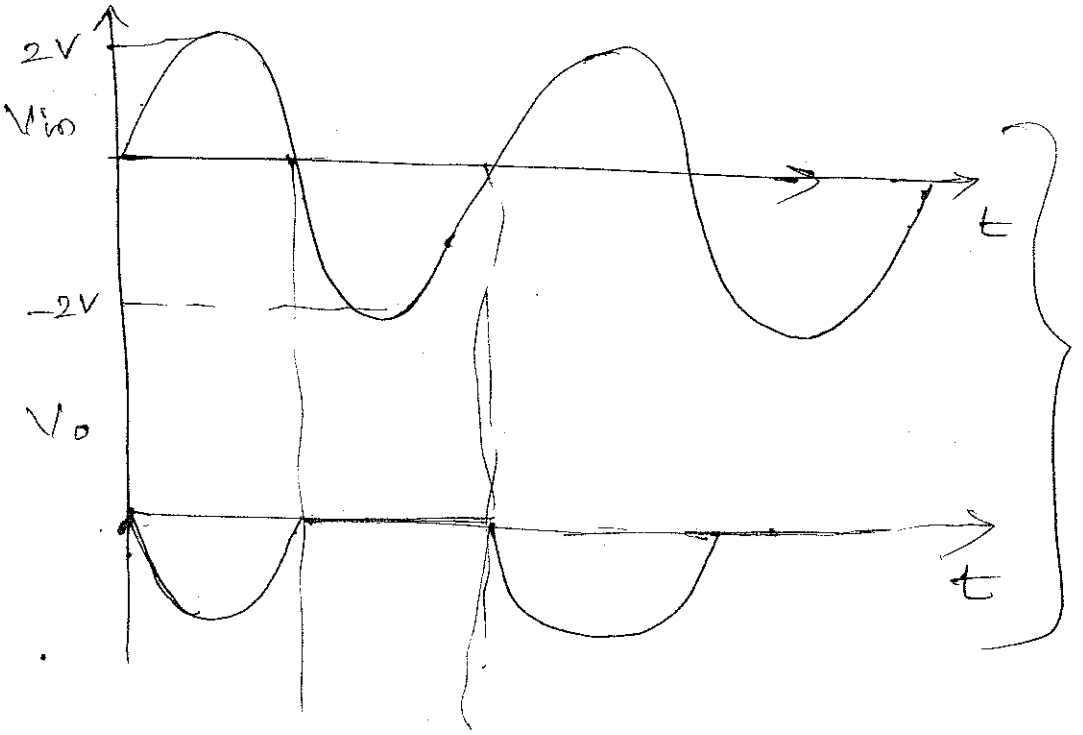
$V_{LT} = -4.59V$ (2M)



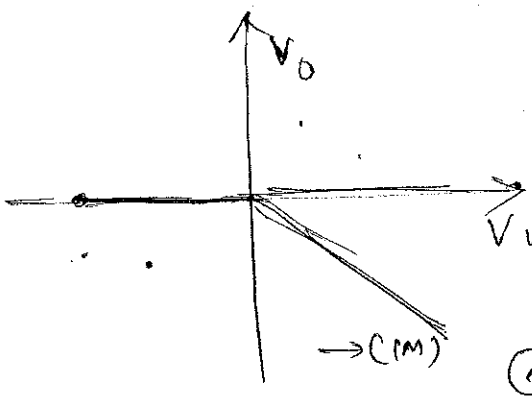
(2M)

Hysteris is Preferred in schmitt trigger because it Prevents noise from causing false triggering. (1M)

(2)

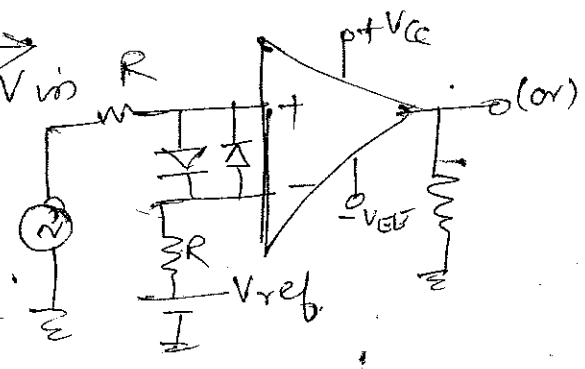


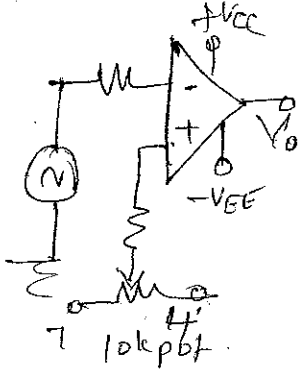
(1M)



Qn 5

Voltage level detector





(2M)

R_3

(1M)

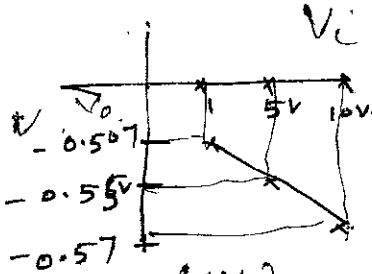
⇒ To minimize error caused by input bias current

(3) $V_o = -V_T \ln\left(\frac{V_i}{R_s I_s}\right)$ 1V, 5V, 10V

$= -0.026 \ln\left(\frac{1}{100 \times 10^3 \times 3.3 \times 10^{-14}}\right) = -0.507$ V

⇒ -0.549 V (for V_i = 5V)

⇒ -0.567 V. (for V_i = 10V) (1M)



(1M)

(4) For signal processing, many transducers produce output voltage that vary nonlinearly with physical quantity being measured. Often it is desirable to linearize output of such devices. Log amp & multipliers are used.

(2M)

BITS, PILANI – DUBAI

Version A

SECOND SEMESTER 2012-2013

THIRD YEAR ECE

Course Code: ECE C364
Course Title: ANALOG ELECTRONICS
Duration:20minutes

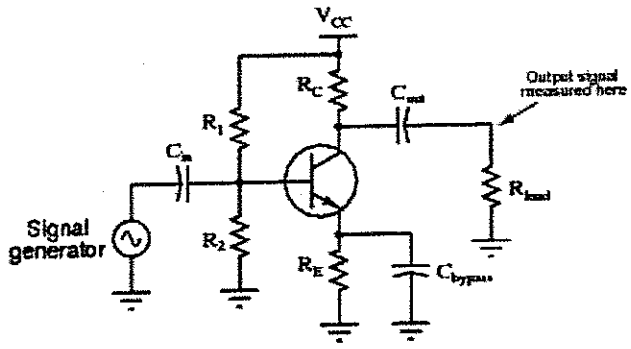
Date:11.03.2013
Weightage:8%
Max Marks: 16

Name: ..... **ID No:** ..... **Sec / Prog:** .....

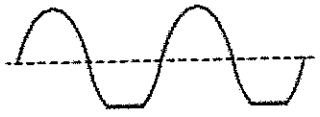
Instructions: Write your answers in the blank space provided after each question. This question paper has 8 questions. Answer all questions.

1. Bipolar junction transistors are classified as *minority carrier* devices. Explain (in brief) why? Write only key points in your answer. [2M]

2. Suppose you were troubleshooting the following amplifier circuit, and found the output signal to be "clipped" on the negative peaks:



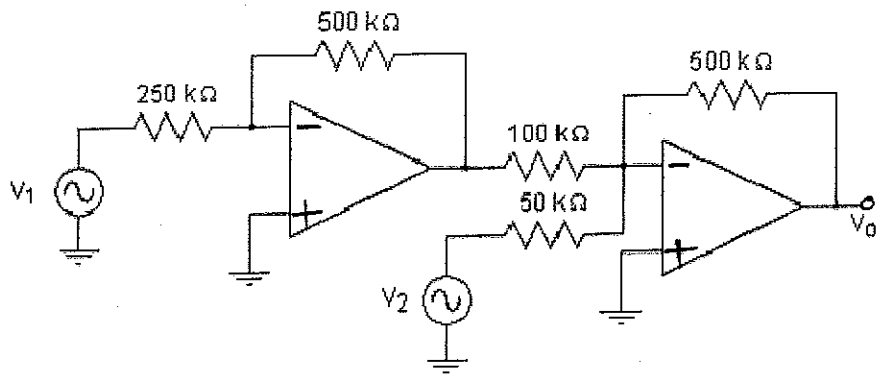
Output signal:



If you knew that this amplifier was a new design, and might not have all its components properly sized, what type of problem would you suspect in the above circuit? How will you overcome the problem? Give your answer as specific as possible. [2M]

P.T.O

3 Calculate the output voltage for the following circuit if V_1 = 300 mV and V_2 = 700 mV. Show clear steps in your answer.



[2M]

4. You are provided with two IC op amps with following characteristics:
Op-amp 1: Z_{in} =5MΩ, Z_{out} =100Ω, A_v =50,000
Op-amp 2: Z_{in} =10MΩ, Z_{out} =75Ω, A_v =150,000
Which one of them you can choose for satisfying the basic requirements of practical op-amps? Justify your answer. [2M]

5. Determine the output voltage shown in Fig.1when $V_1 = -V_2 = 1$ V. Show Clear steps in your answer. [2M]

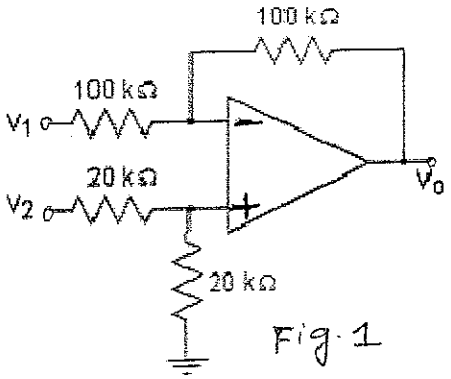
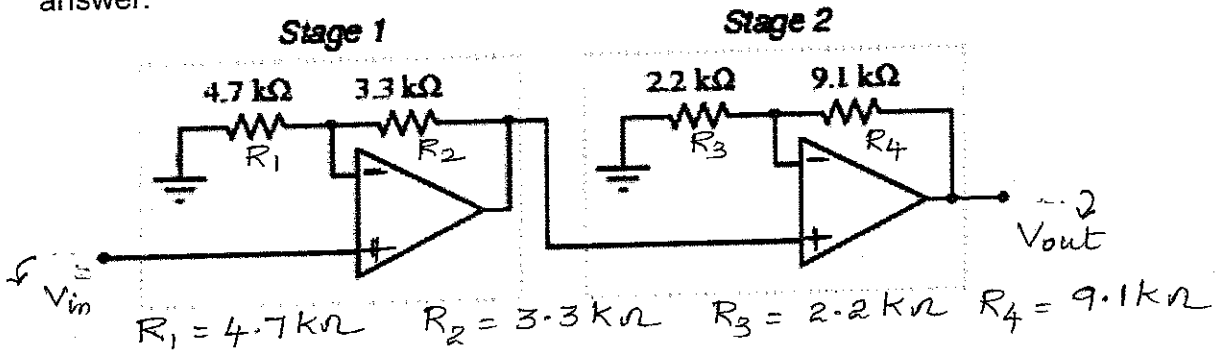


Fig. 1

6. Calculate the voltage gain for each stage of this amplifier circuit (both as a ratio and in units of decibels), then calculate the overall voltage gain: Show clear steps in your answer. [2M]



$R_1 = 4.7k\Omega$ $R_2 = 3.3k\Omega$ $R_3 = 2.2k\Omega$ $R_4 = 9.1k\Omega$

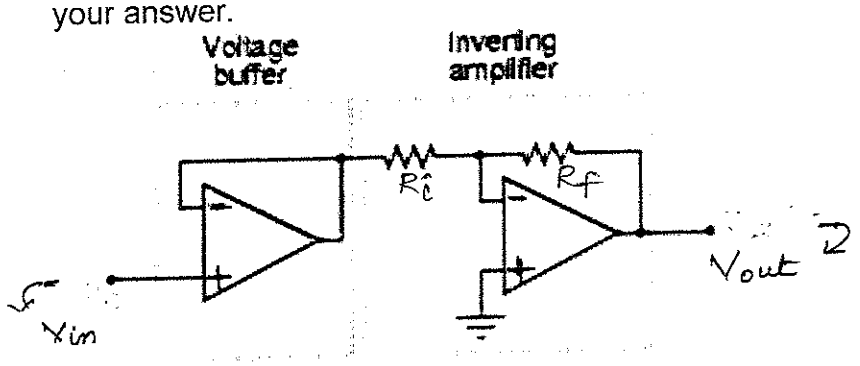
P.T.O

7. Design a suitable op-amp based circuit to obtain the following expression:

$$V_0 = -3(V_1 + V_2 + V_3)$$

Show clear design steps in your answer with diagram. [2M]

8. What possible benefit is there by adding a voltage buffer to the front end of an inverting amplifier, as shown in the following schematic? Write only key points in your answer. [2M]



Answering Scheme

BITS, PILANI – DUBAI **Version A**

SECOND SEMESTER 2012-2013

THIRD YEAR ECE

Course Code: ECE C364
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Duration:20minutes

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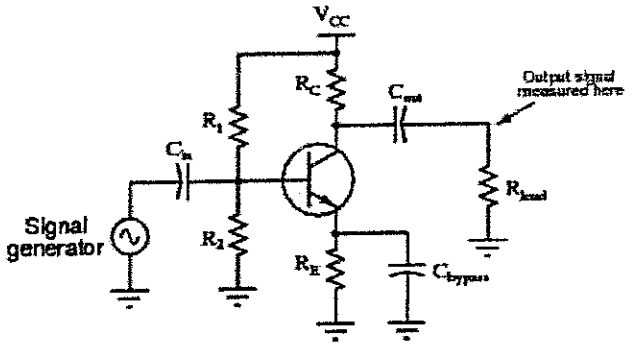
Name: ..... **ID No:** ..... **Sec / Prog:** .....

Instructions: Write your answers in the blank space provided after each question. This question paper has 8 questions. Answer all questions.

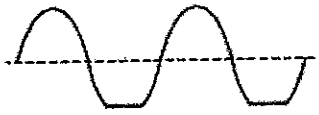
1. Bipolar junction transistors are classified as *minority carrier* devices. Explain (in brief) why? Write only key points in your answer. [2M]

Conduction through BJT depends on charge carriers being injected into the base layer of the transistor and these charge carriers are always the minority type with respect to the doping of the base. [2M]

2. Suppose you were troubleshooting the following amplifier circuit, and found the output signal to be "clipped" on the negative peaks:



Output signal:



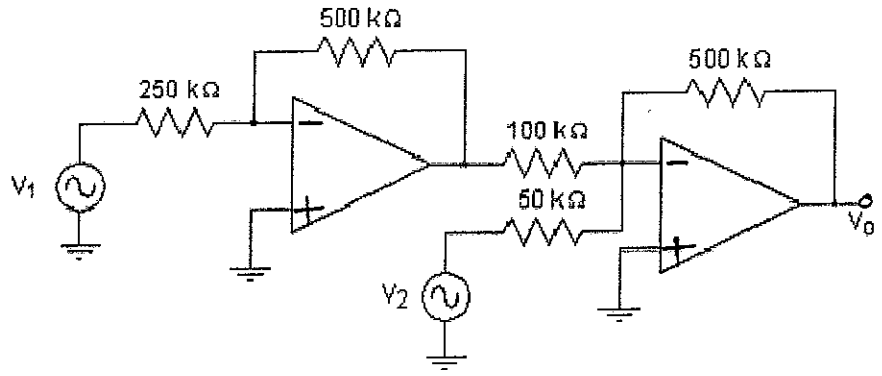
If you knew that this amplifier was a new design, and might not have all its components properly sized, what type of problem would you suspect in the above circuit? How will you overcome the problem? Give your answer as specific as possible. [2M]

Problem :- The amplifier suffers from improper biasing. [1M]

To overcome this Problem :- Change the value of R_1 or R_2. [1M]

P.T.O

3 Calculate the output voltage for the following circuit if V_1 = 300 mV and V_2 = 700 mV. Show clear steps in your answer.



[2M]

Stage 1 $V_1' = -\frac{500k\Omega}{250k\Omega} \times V_1 = -600mV$ ⟶ (1M)

$V_o = -\frac{500}{100k\Omega}(-600mV) - \frac{500k\Omega}{50k\Omega}(700mV)$

$= -4000\,mV$

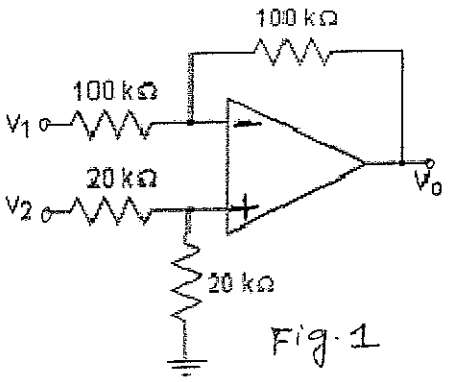
$\Rightarrow -4V$ [1M]

4. You are provided with two IC op amps with following characteristics:
Op-amp 1: Z_{in} =5MΩ, Z_{out} =100Ω, A_v =50,000
Op-amp 2: Z_{in} =10MΩ, Z_{out} =75Ω, A_v =150,000
Which one of them you can choose for satisfying the basic requirements of practical op-amps? Justify your answer. [2M]

Op amp 2. ——— (1M)

Justification :- The characteristics of Practical op-amp includes high voltage gain, high input impedance and low output impedance which can be fulfilled by Op-amp2. (1M)

5. Determine the output voltage shown in Fig.1when $V_1 = -V_2 = 1$ V. Show Clear steps in your answer. [2M]



Fig·1

when $V_2 = 0$.

$V_{01} = \frac{-100k\Omega}{100k\Omega} V_1$ ⟶ ½ M.

$V_1 = 0$

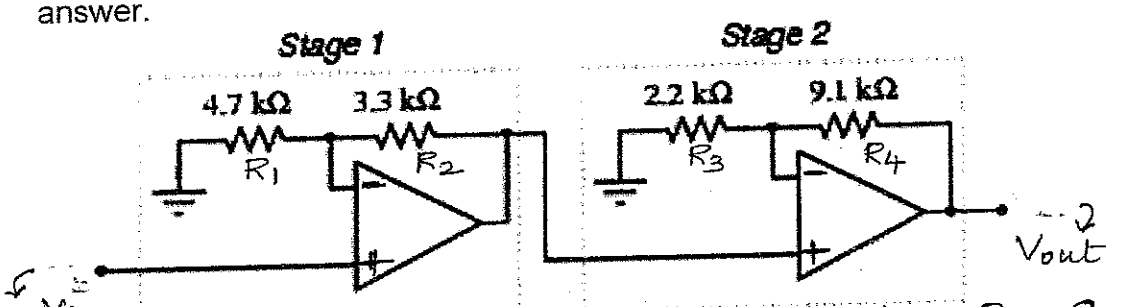
$V_{02} = \left(1 + \frac{100k\Omega}{100k\Omega}\right) V_2'$.

$V_{02} = 1 + 1 \times \frac{20}{40} \times V_2 = V_2$. ⟶ ½ M.

$V_0 = V_{01} + V_{02} = -V_1 + V_2$

$= -2V$ ⟶ (1M)

6. Calculate the voltage gain for each stage of this amplifier circuit (both as a ratio and in units of decibels), then calculate the overall voltage gain: Show clear steps in your answer. [2M]



$R_1 = 4.7k\Omega$ $R_2 = 3.3k\Omega$ $R_3 = 2.2k\Omega$ $R_4 = 9.1k\Omega$

I stage $A_V = 1 + \frac{R_f}{R_{in}} = 1.702 = 4.62dB$

II stage $A_V = 1 + \frac{9.1k\Omega}{2.2k\Omega} = 5.136 = 14.213dB$.

(½M, ½M)

Overall Voltage gain $A_V = 8.743$

$= 18.833dB$ ⟶ (1M)

P.T.O

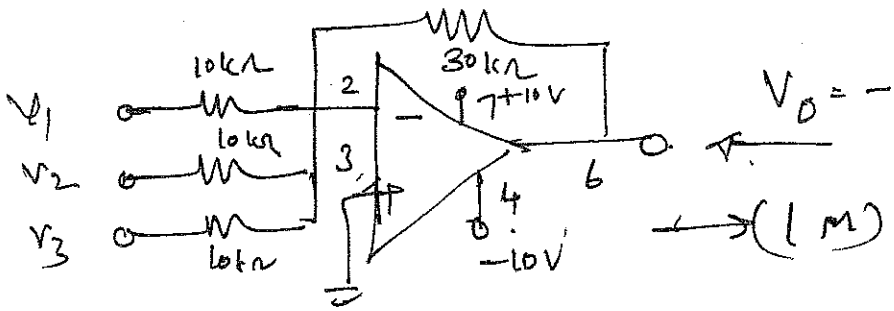
7. Design a suitable op-amp based circuit to obtain the following expression:

$$V_0 = -3(V_1 + V_2 + V_3)$$

Show clear design steps in your answer with diagram. [2M]

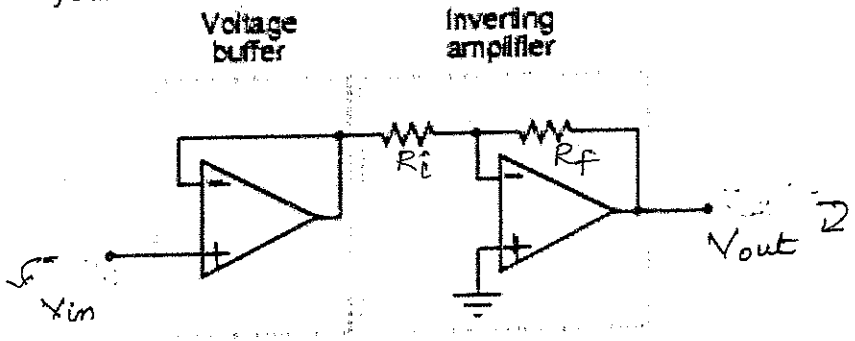
$\frac{R_f}{R} = 3 \quad R_f = 3R.$

$R_1 = R_2 = R_3 = R = 10k\Omega \quad R_f = 30k\Omega.$ → (1M)



$V_0 = -3(V_1 + V_2 + V_3)$ → (1M)

8. What possible benefit is there by adding a voltage buffer to the front end of an inverting amplifier, as shown in the following schematic? Write only key points in your answer. [2M]



Key Points Voltage buffer raises the amplifier input impedance without altering Voltage gain. → (2M)