BITS PILANI, DUBAI CAMPUS

II SEMESTER 2012-13

Comprehensive Examination

COURSE: CS C342 ADV COMP ORGANIZATION YEAR: III YEAR COMPUTER SCIENCE

DATE: 03-06-2013 (AN) WEIGHTAGE: 40 % (40 MARKS) NO. PAGES : 2 PAGES

Note: Answer all the Questions. Draw the diagrams neatly without over writing.

1. Give the MIPS code for the C language assignment statement given below:

   A[300] = h + a[300]; (1 Marks)

2. Why don't MIPS have a "subtract immediate" instruction? (2 Marks)

3. Explain the *ori* instruction with an example? (2 Marks)

4. List down the registers that are used for the following MIPS action: (3 Marks)

   (i) Registers that are used to pass parameters.

   (ii) Registers in which to return values

   (iii) Register to return to the point of origin

5. Give the MIPS statement that gives unsigned Quotient and remainder. (1 Mark)

6. Give the algorithm for floating point addition? (2 Marks)

7. If a Java Program runs in 10 seconds on Lenovo Computer, which has a 4 Ghz clock. We are trying to help the designer to build a computer X that runs the same Java program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer X to require 1.2 times as many clock cycles as computer Lenovo for this program. What clock rate should we tell the designer to target so that it runs the same program in 6 seconds? (3 Marks)

8. Consider the computer with three instruction classes and the CPI for these instructions are shown the table below:

	CPI for this Instruction Class		
	A	B	C
CPI	1	2	3

Execute the code of the same program using two different compilers and obtain the following data:

Code from	Instruction counts (in billions) for each instruction class		
	A	B	C
Compiler X	5	1	1
Compiler Y	10	1	1

Assume that the computer Clock rate is 4 Ghz. Which code sequence will execute faster according to MIPS (Millions Instruction Per Second)? According to Execution Time? (5 Marks)

9. What do you mean by Delayed Branch? Explain it. (2 Marks)
10. Give the Data Path Diagram for the R-Type Instruction *add $t1, $t2, $t3* with all its signal inputs / outputs and control signals. (3 Marks)
11. Give all the control line signal value for *beq* instruction. (2 Marks)
12. Give the simplified pipeline data path diagram for the following set of MIPS Instructions: (3 Marks)

    sub $2, $1, $3
    and $12, $2, $5
    or $13, $6, $2
    add $14, $2, $2
    sw $15, 100($2)

    Check whether they are dependent, if so; show them in the data path diagram.
13. Consider a cache with 64 blocks and a block size of 16 bytes. What block number does byte address 1200 map to? (2 Marks)
14. If the design has 4 independent cache memory modules like L1, L2, L3 & L4, how does the data available with them are read by the Processor and what are the combinational logic elements are used or what type elements you will be recommending for this design? (2 Marks)
15. What do you mean by dependability and how it interrupted and restored? Explain and how they are measured? (2 Marks)
16. What do you mean by Asynchronous bus? What is the advantage and disadvantage of this type bus? (2 Marks)
17. Explain shared memory multiprocessor. Give their advantages and disadvantages? (2 Marks)
18. What are the difference between cluster computing and Grid computing? (1 Marks)

-----All The Best-----

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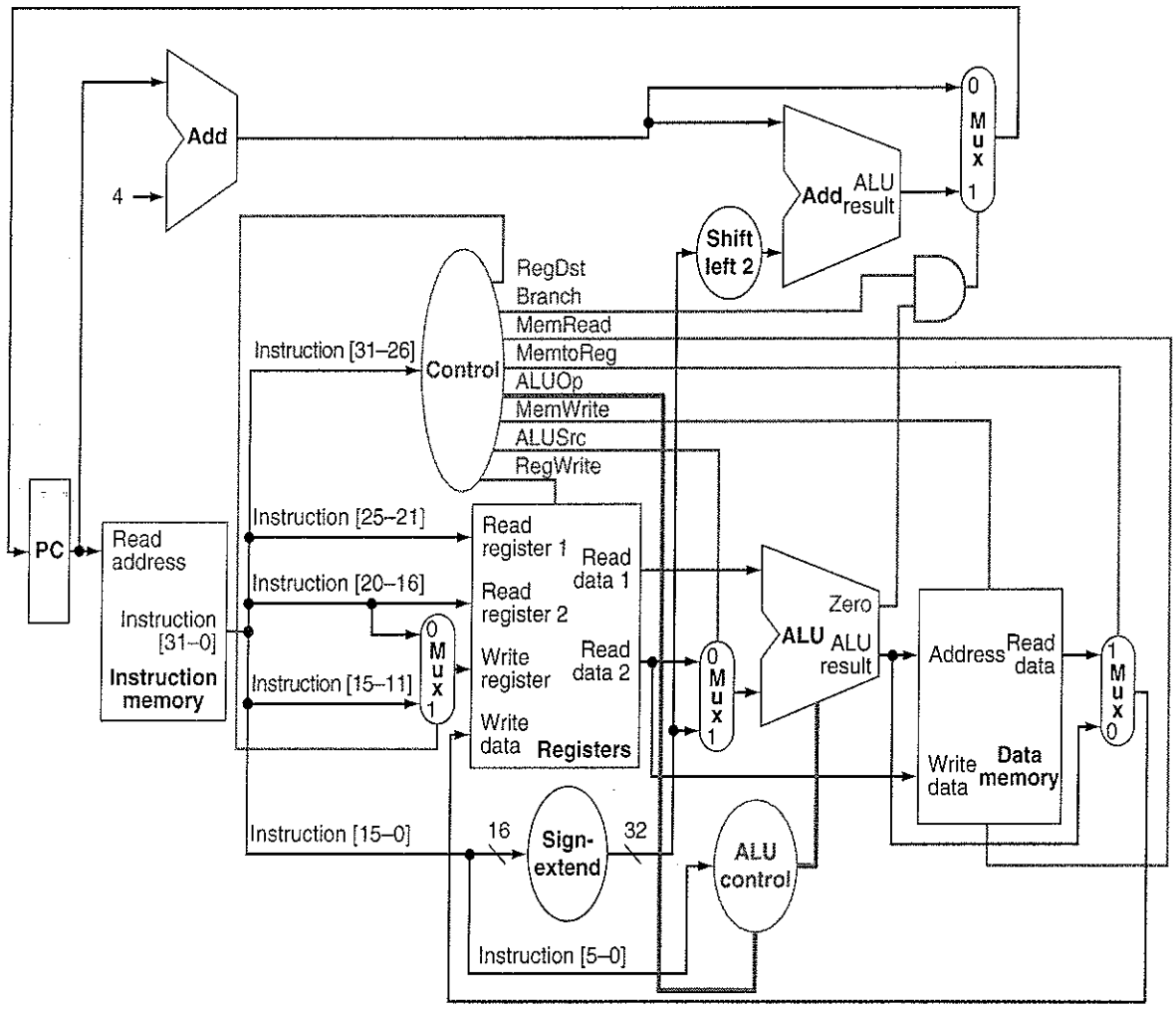
II SEMESTER 2012-13

COURSE	:	**CS C342 ADV COMP ORGANIZATION**
YEAR	:	III YEAR CS
COMPONENT	:	TEST – 2 (OPEN BOOK)
WEIGHTAGE	:	20% (20 MARKS)
DATE & DURATION	:	17-04-2013 & 50 MINS.
NO. OF PAGES	:	2 PAGES

Note: Answer all the Questions.

Draw the datapath design diagram neatly without overwriting. Mention your view and assumption clearly wherever required. Text Book, Class Notes and printed materials are allowed.

1. What does "Shift Left 2" represent in the datapath design? Explain it to the point. (3 Marks)
2. The diagram given below is the complete datapath design of the Processor. Use only the required component from the datapath design and give your answers for the following:

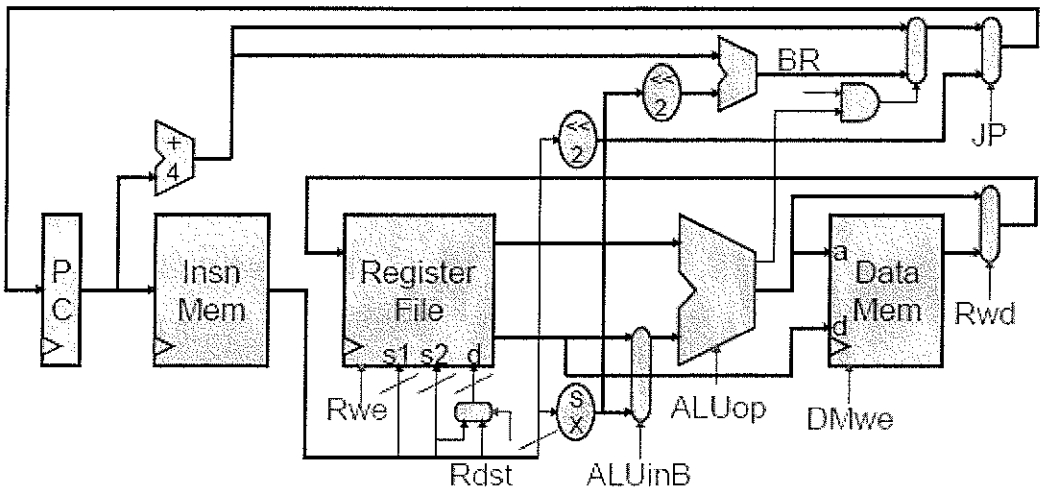


(i) Redraw the design that show the operation of an " addi " MIPS instruction. (3 Marks)

(ii) Redraw the datapath design that shows the operation of " jal " MIPS Instruction. (3 Marks)

(iii) Redraw the datapath design that shows the operation of "bne" MIPS Instruction. (3 Marks)

3. Design shown below is the datapath processor design with the control signals. What will be the value to "set" these control signals for the lw instruction? (2 Marks)



4. What are the combinational logic elements are used to construct the control unit block of a processor datapath design? Draw the control unit design using those combinational logic elements and justify your answer why you have selected these combinational logic elements? (3 Marks)
5. Explain when does the hit value is set to "1" and show that using a simple design with cache memory, combinational logic elements. (3 Marks)

***** *All the Best* *****

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II SEMESTER 2012-13

A

COURSE	:	CS C342 ADVANCED COMPUTER ORGANIZATION
YEAR	:	III YEAR COMPUTER SCIENCE
COMPONENT	:	QUIZ – 2 (CLOSED BOOK)
MARKS	:	7 MARKS
DATE & DURATION	:	8-5-2013 & 20 MINS.

ID. NO.: _____ **NAME:** _____

1. What does the following statement represent "When a planned instruction cannot execute in the proper clock cycle because the hardware does not support the combination of instructions that are set to execute"? (½ Mark)

2. A technique of resolving a hazard by retrieving the missing data element from the internal buffers rather than waiting for it to turn up from programmer-visible register or memory is called as: (½ Mark)

3. Why does stalls are initiated in a pipelined data path design? (1 Mark)

4. What do you mean by Branch Hazard? Define it. (1 Mark)

5. Give the difference between Static Prediction and Dynamic Prediction? (1 Mark)

6. Check whether the given statement is true, if true justify your answer in one or two lines only; "pipelining does not reduce the time it takes to complete an individual instruction, but increases the number of simultaneously executing instructions". (1 Mark)

7. What do you mean by Branch History Table? (½ Mark)

8. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32 – bit address? (1 ½ Marks)

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B

II SEMESTER 2012-13

COURSE	:	CS C342 ADVANCED COMPUTER ORGANIZATION
YEAR	:	III YEAR COMPUTER SCIENCE
COMPONENT	:	QUIZ – 2 (CLOSED BOOK)
MARKS	:	7 MARKS
DATE & DURATION	:	8-5-2013 & 20 MINS.

ID. NO.: _____ **NAME:** _____

1. When a hardware cannot support the mixtures of instructions that we want to execute in the same clock cycle, we call this as : (½ Mark)

2. Adding extra hardware to retrieve the missing item early from the internal resources is called as: (½ Mark)

3. Why does stalls are initiated in a pipelined data path design? (1 Mark)

4. What do you mean by Control Hazard? When did it arise? (1 Mark)

5. What does the following statement represents, " A method of resolving a branch hazard that assumes a given outcome for the branch and proceeds from that assumption rather than waiting to ascertain the actual outcome". (1 Mark)

6. What do you mean by Branch History Table? (½ Mark)

7. Check whether the given statement is true, if true justify your answer in one or two lines only; "pipelining does not reduce the time it takes to complete an individual instruction, but increases the number of simultaneously executing instructions". (1 Mark)

8. How many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32 – bit address? (1 ½ Marks)