BITS PILANI, DUBAI CAMPUS

II SEMESTER 2011 – 2012

Course Code: EEE C391 | TEST-2 (Open Book) | Date: 06.05.2012

Course Title: DECO | Max.Marks:25

Duration: 50 minutes | Weightage: 12.5%

Instructions: 1.ANSWER all questions in sequence of their order.
2. Make assumptions, if any, but explicitly indicate the assumptions made

1.

A sequential circuit has two JK flip flops and one input x and one output S. The circuit is described by following flip flop input equations $J_A = x$, $K_A = B'$, $J_B = x$ and $K_B = A$ and the output $S = A'B$

i) Draw the circuit diagram. ii) Derive the state equations A(t+1) and B(t+1). 2 +2

iii) Draw the state diagram. +3

2. Design an universal 4 bit shift register using D flip flops whose function table is as shown below.

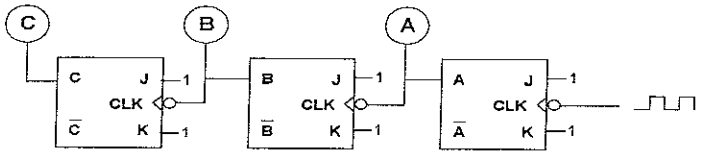
Mode control		Function
0	0	Clear the register
0	1	Load new data
1	0	Shift right
1	1	No Change in data

4

3. A three bit up counter is as given below. Modify the circuit to 4

(i) A **down counter** with no additional logic gate

(ii) An **up/down counter** using additional EX-OR gates only



4.

How many address lines are required to address a 4K x 8 memory? What would be the starting and ending addresses of the Memory? What would be the maximum value of data which can be stored in a memory location. 4

5. Design a full adder using PLA and develop its programming table 6

****

BITS PILANI, DUBAI CAMPUS

II SEMESTER 2011 – 2012

Course Code: **EEE C391/ECE C391** **TEST-1** Date: 18.**03.2012**

Course Title: **DECO** Max.Marks:25

Duration: **50 minutes** Weightage: **12.5%**

Instructions: 1.ANSWER all questions in sequence of their order.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Calculators are not allowed

---

1. Find the following by direct conversion 2+1+2

   a) $(132 \frac{37}{64})_{10} = (\quad\quad\quad\quad)_2$

   b) $(11100.010101)_2 = (\quad\quad\quad\quad)_H$

   c) Compute $(783)_H - (78)_H$ using 16's complement

2. Implement the following function 2+2
   $F(A,B,C) = AB'C'+A'BC'+ABC + A'B'C + A(B'C'+BC)$ using two level EX- OR logic gates only.

3. Draw and explain a 4-bit binary word adder circuit using full adders. Modify the circuit to perform addition or subtraction using additional external logic gates. Explain the logic of your design. 2+1+1

4. Simplify the following function F(A,B,C,D) along with the don't care condition d(A,B,C,D) 2+1+1+2
   $F(A,B,C,D) = \sum(5,6,7,8,9,) + d(10,11,12,13,14,15)$.
   Identify prime implicants and essential prime implicants.
   Implement the function using minimum no. of NOR gates alone.

5. Develop the truth table of the function given below and realize it using only 2 to 4 line active high decoders with active low enable pin and external two input OR gates 2+2+2
   $f(x,y,z) = xy + xz'+y'z$

****

NAME: ID NO:

BITS, PILANI – DUBAI CAMPUS

II SEMESTER 2011 – 2012

III Yr ECE/EEE

Version B

Course Code: **EEE C391/ECE 391** **Quiz-1** Date: **28.02.2012**

Course Title: **Digital Electronics and Computer Organization** Max Marks: 10

Duration: **20 minutes** Weightage: **5%**

Instructions: 1.ANSWER all questions at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. All questions except Q2 carry one marks each.
4.. Write on back side if the space is insufficient.

1. Find out the base of number system if $(101)_b=(37)_{10}$

2. Write SOP expression for the following truth table and prove that $\overline{Y} = A \oplus B$ (2M)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

3. Prove that $\overline{\overline{A}B + \overline{B}C + AB + \overline{B}\overline{C}} = 0$

4. Implement the following function using only NAND gates $Y = AB + \overline{A}\overline{B}$

NAME: ID NO:

BITS, PILANI – DUBAI CAMPUS

II SEMESTER 2011 – 2012

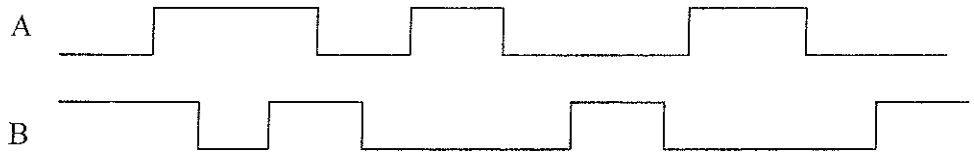
III Yr ECE/EEE

Version B

5. Convert the following Binary code into its equivalent to Gray code (0110)

6. Realize 3 inputs NAND gate by using only 3 inputs NOR gates with positive logic

7. In a circuit the inputs A & B are applied to an AND gate. For the input signals shown below, draw the expected output waveform from the AND gate, Y.



Y

8. Define Noise margin for a digital IC.

9. Prove that positive logic AND is equivalent to negative logic OR