BITS PILANI – DUBAI CAMPUS

II SEMESTER 2011 – 2012 COMPREHENSIVE EXAM

Course Code: EEE / INSTR C364 Date: 12.JUNE.12 Duration : 3 hours
Course Title: ANALOG ELECTRONICS Max Marks: 70 Weightage: 35%

Instructions: Answer ALL Questions. All symbols have their usual significance. Make suitable approximations and assumptions wherever necessary. Answer Section A and B in two separate booklets

PART - A

Q1 For the circuit shown in Fig.1, find the input resistance $R_{in} = V_i/I_i$ in terms of other resistances in the circuit. [6M]

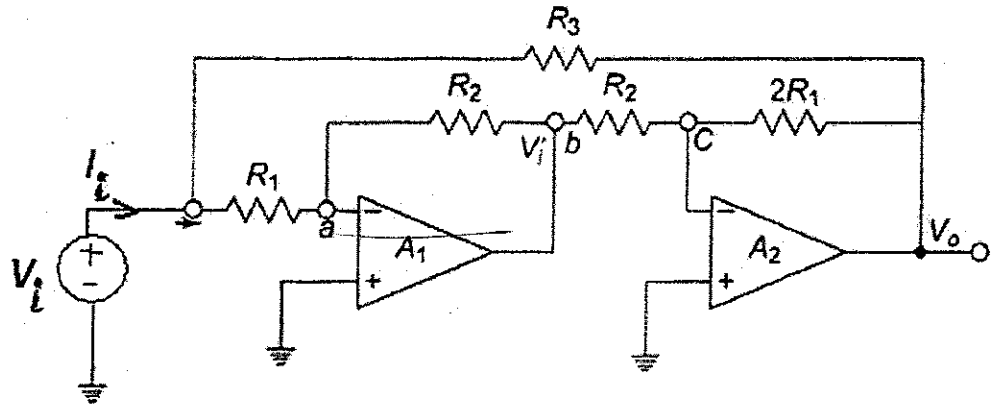


Fig.1

Q2 For the circuit shown in Figure 2, Compute Voltage Gain $(G_V) = \frac{V_{out}}{V_{in}}$ [8M]

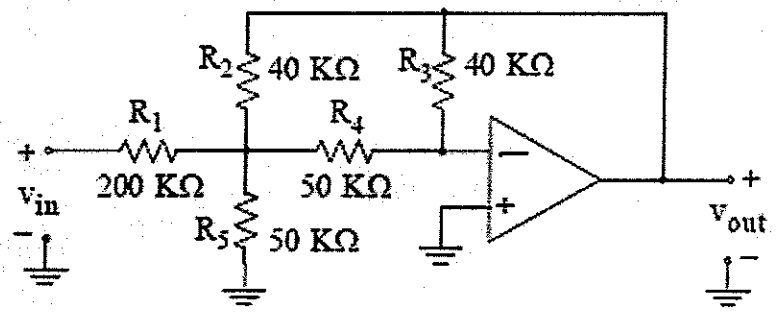


Fig.2

Q3	For the circuit shown in Figure 3, assume R_3 =20kΩ and R_4 = 2 kΩ. V_{in} is a sinusoidal signal with peak value of ±5V and V_{sat} of the opamp is $\pm 13V$. Draw the input-output waveforms and transfer characteristics of the circuit.	[6M]

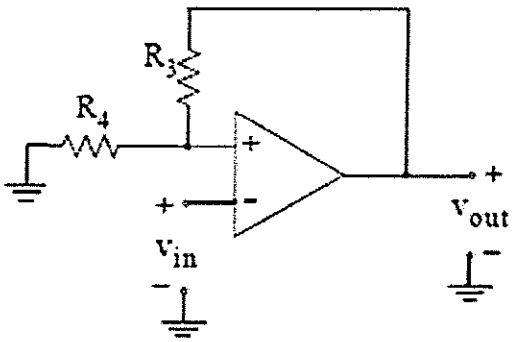


Figure 3

Q4	State if the circuit of figure 4 functions as a low pass or a high pass filter. Write down the voltage transfer function.	[8M]

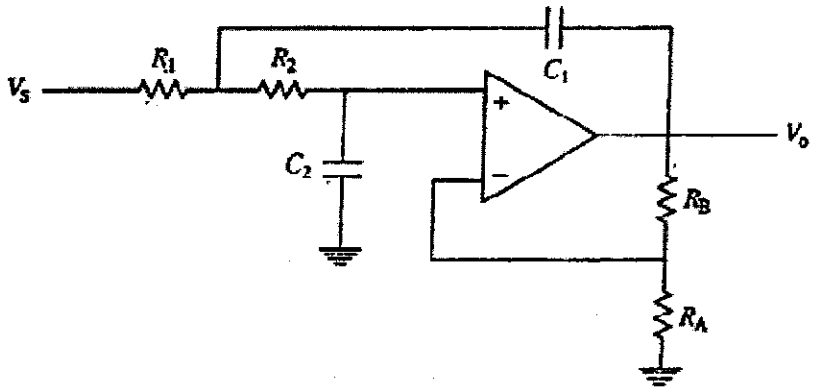


Figure 4

When all resistances are expressed in MΩ and all capacitances in μF, it is observed that the numerical values of R_1, R_2, R_A, C_1 and C_2 are same. Design the circuit to provide a cut off frequency ω_c = 500 rads/sec. What is the low frequency voltage gain of the circuit, for a maximally flat response. Does the property of the circuit change if all resistances are increased by a factor of 3 and all capacitors are decreased by a factor of 3? Explain with reasons.

Q5	In a certain amplifier, the total collector current (in mA) is given by $i_c = (5)(3 + V_{in})^3$, where V_{in} (in mV) = $3\sin\omega t$. Determine the quiescent collector current, average collector current and the total harmonic distortion for the amplifier. Given: $sin3\theta = 3sin\theta - 4sin^3\theta$	[7M]

PART - B

Q6 Design an IC 723 based positive voltage regulator to give +8 V output at 200mA. Incorporate short circuit protection to limit current at 400mA. Find all resistor values used in the design along with their power ratings. Draw the complete circuit diagram. Assume C=500pF, R_1 (connected between pin 3 and pin 4) = 1kΩ and V_{ref}=7V. [7M]

Q7 An opamp based circuit is used to obtain an output as shown in figure 5(b) for an input as shown in Figure 5(a) [8M]

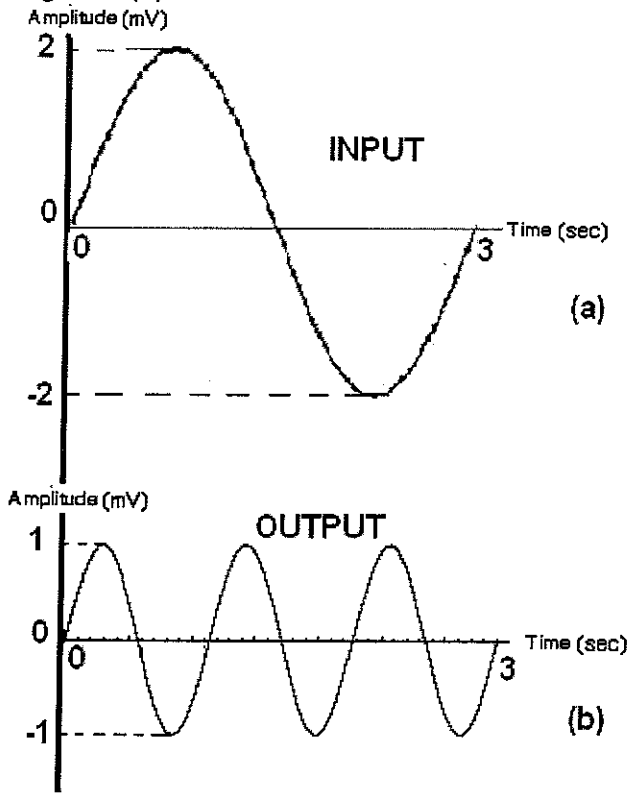


Figure 5

Design the opamp circuit using two analog multipliers and one difference amplifier. The multiplier block provides an output $V_z = V_x.V_y$, where V_x and V_y are the respective inputs to the multiplier. The difference amplifier is designed to produce an output $V_d = K_1.V_a - K_2.V_b$, where K_1 and K_2 are suitable constants and V_a and V_b are the corresponding inputs.

Q8 Design an IC 555 timer in the astable mode to generate a square wave of 2KHz frequency, giving output equal to 5 V for 1 msec and output equal to 0 V for next 1 msec repeating periodically. Connect one red LED and one green LED so that they flash alternately every 1 msec. Assume that LEDs have ratings of 0.7 V and 50mA. Draw the circuit for the above specifications. Assume Vcc = 5 V, and C=0.1μF. Also sketch output voltage and capacitor voltage waveforms. [7M]

Q9 For the Class A Power Amplifier of Fig 6, let Vcc = 15V, I = 100mA and R_L = 100Ω. If the output voltage is 10V peak sinusoid ,find the following [7M]

(a) power delivered to the load

(b) the average power drawn from the supplies and

(c) the power conversion efficiency. Why is the efficiency for Class A lower than Class B or Class AB?

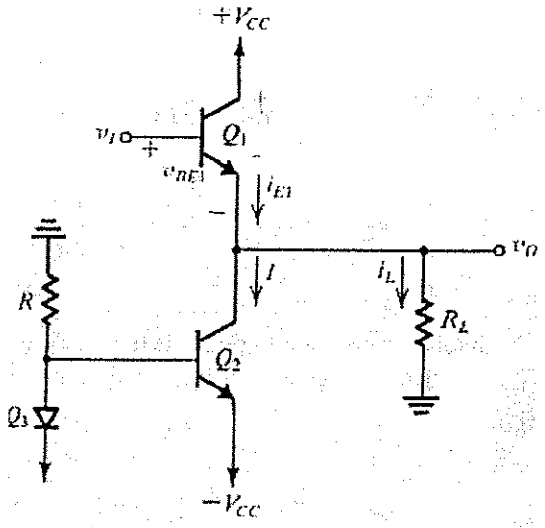


Figure 6

Q10 There are two temperature sensors A and B, in a room. Sensor A has a response of 12 mV/°C while that of Sensor B is x mV/°C. The outputs of these sensors are used as inputs to a non-inverting opamp as shown in Figure 7. When the resistor R is chosen as 400 Ω, the output V_o in mV displays the room temperature in °C. [6M]

(a) Determine x.

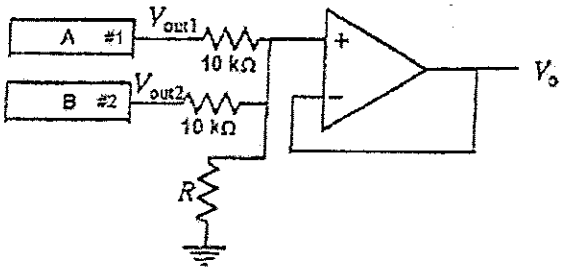


Figure 7

(b) Design a non inverting opamp based adder circuit that will modify V_o to give a display in Farenheit scale.

End of Paper

BITS PILANI DUBAI CAMPUS
ECE/INSTR C364 – ANALOG ELECTRONICS - Test 2

Sem2, 2011 2012 | OPEN BOOK | Time Allowed: 50 mins
Total Marks : 30 | Weightage: 15%

INSTRUCTIONS

This paper contains **SIX (6)** questions. Answer **ALL** questions. Unless specifically stated, all symbols have their usual meanings. Make appropriate assumptions wherever applicable

1. A Phase Locked Loop has free running frequency of 550 KHz and bandwidth of the low pass filter is 15 KHz. Will the loop acquire lock for an input signal of 700 KHz? Justify your answer. Assume that the phase detector produces sum and difference frequency components.

(4 marks)

2. Using a 0.1μF capacitor and an IC 555 timer, design the astable circuit to obtain a square wave with 1 KHz frequency and 70% duty cycle. Specify the values of any resistors used in the design.

(5 marks)

3. Design a monostable multivibrator using IC 555 timer to produce a quasi stable state of duration of 200 ms. Select a suitable trigger signal. Draw the input and output waveforms and mark the necessary timings. Assume C = 0.2 μF.

(4 marks)

4 In a certain power amplifier circuit, the output current $i_c = G_1\, i_b + G_2\, i_b^2$ for an input signal is given by $i_b = (I_1 \cos\omega_1 t + I_2 \cos\omega_2 t)$. G_1, G_2, I_1 and I_2 are constants. Show that the output will contain a DC term and sinusoidal terms of frequencies $\omega_1, \omega_2, 2\omega_1, 2\omega_2, (\omega_1 + \omega_2)$ and $(\omega_1 - \omega_2)$.

(5 marks)

5. Identify the circuit in Figure.1, and analyze its output voltage when (i) $V_i > 0$ V and (ii) when $V_i < 0$ V. Draw a simplified circuit diagram for the above two cases. (iii) Assuming the input to be a 1 V peak – peak sinusoid, sketch the input and output waveforms. Consider ideal diodes.

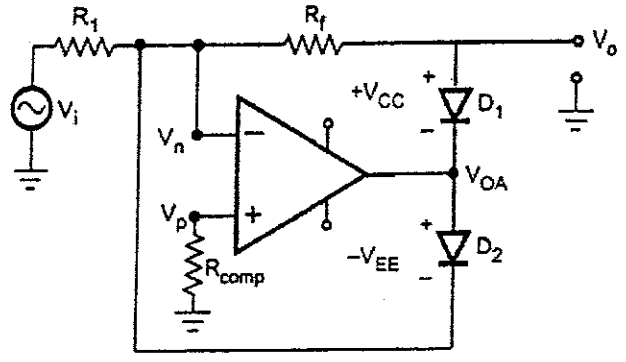


Figure 1

(5 marks)

6. A 10V, 2W zener diode requires a minimum reverse current of 5 mA to keep the diode in breakdown. Assume V_{zk} = 10V.The diode is used in a regulator circuit shown in Figure 2. V_{in} can vary from 15 V to 20 V.

(a) The diode is expected to operate under minimum conditions when V_{in} is minimum. Design a suitable value of R_s so that the regulator circuit can operate under minimum conditions.

(b) With R_s designed as in (a) above, if V_{in} increases to 20 V, determine the operating point for the zener and the power dissipated in R_s.

(c) What value of R_s will you chose if the diode operates in its maximum conditions?

(7 marks)

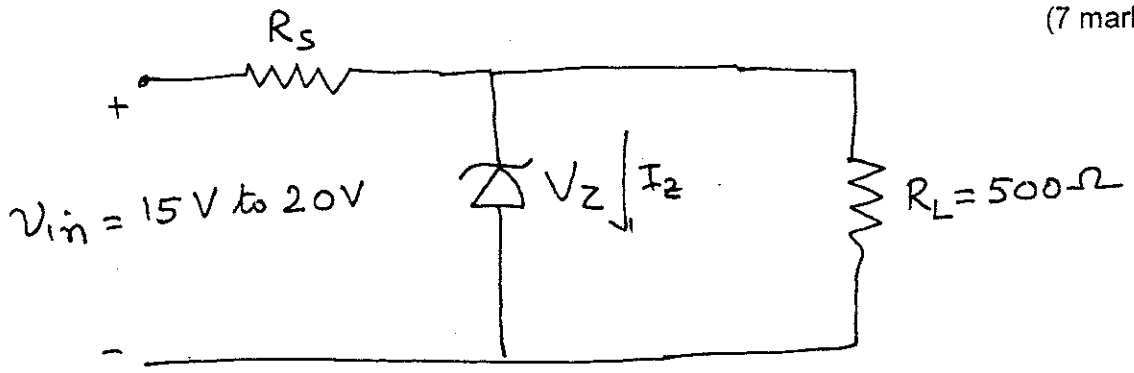


Figure 2

End of Paper

BITS PILANI DUBAI CAMPUS
ECE / INSTR C364 ANALOG ELECTRONICS - Test 1

Sem2, 2011 - 12 CLOSED BOOK Time Allowed: 50 mins
Total Marks : 30 Weightage: 15%

INSTRUCTIONS

This paper contains **SIX (6)** questions and has TWO (2) pages. Answer **ALL** questions. Unless specifically stated, all symbols have their usual meanings. Assume suitable data if required

---

1. An inverting opamp circuit has an input resistance R_1 = 5 kΩ and feedback resistor R_f= 47 kΩ. An oscilloscope is connected between the output terminal and ground to record the output voltage. Assume that the supply voltages are ± 10 V. A signal source is applied at the input. Draw the entire opamp circuit, showing all relevant op-amp pin numbers. Sketch the input and output waveforms for the following cases:
(a) A 2V peak-peak sinusoidal input signal and an ideal opamp,
(b) A 3V peak-peak triangular waveform and an ideal opamp, and
(c) A 2V peak-peak sinusoidal input and a non-ideal opamp having an input offset voltage of 2 mV.

(6 marks)

2. For the inputs and output as indicated in the circuit shown in Figure 1, calculate the differential gain. Hence find the value of R_G required to provide the necessary output.

(5 marks)

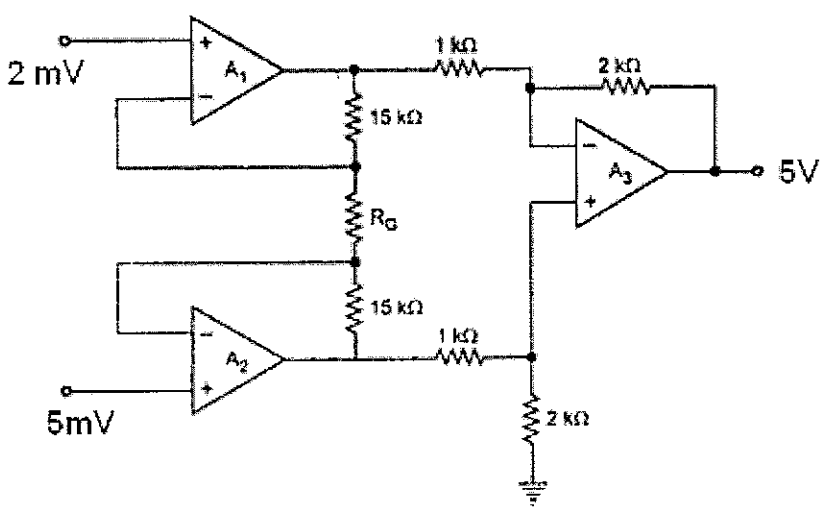


Figure 1

3. Implement the following expression

$$V_0 = 2*[V_1 + V_2 - (V_3 + V_4)]$$

using only two inverting opamps. Assume that the dc inputs V_1, V_2, V_3 and V_4 cannot be modified before they are applied to the opamp inputs. The input

P.T.O

resistance for the opamp circuit is required to be 10 KΩ. The opamp supply voltages are ± 10 V. All the applied inputs are in volts. Draw the complete circuit and state any limitations on the inputs applied.

(6 marks)

4. In the opamp circuit shown in Figure 2, it is desired that

$$V_0 = \frac{V_2}{3} - 2v_1$$

Find the value of R to achieve V_0. Suppose $v_1 = 1V$ and $v_2 = 10\ V$ and a load resistor of R_L = 10 KΩ is connected at the output terminal, determine the power dissipated by the load.

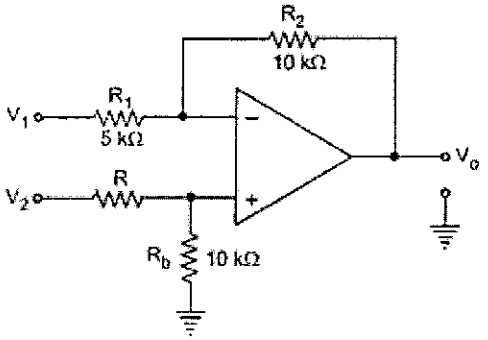


Figure 2

(5 marks)

5. The cutoff frequency of a certain second-order Butterworth low-pass filter is 5 KHz. Assume all capacitor values to be 0.01 μF. The resistors associated with the capacitors are identical. Draw a schematic of the circuit and determine suitable values of all resistors used in the filter design. Determine the passband gain of the filter. It is desired to change the cut off frequency of this low-pass filter to 7 KHz by using the frequency scaling technique. Which circuit elements would you change and to what value?

(6 marks)

6. Consider the circuit of Figure 3 as a feedback amplifier. In the circuit, R_L is the load resistor. Determine the nature of output sampling and input mixing. Hence find the feedback topology. Consider R_L = 10 KΩ and R_2 = 1 KΩ. Calculate the feedback factor β.

(2 marks)

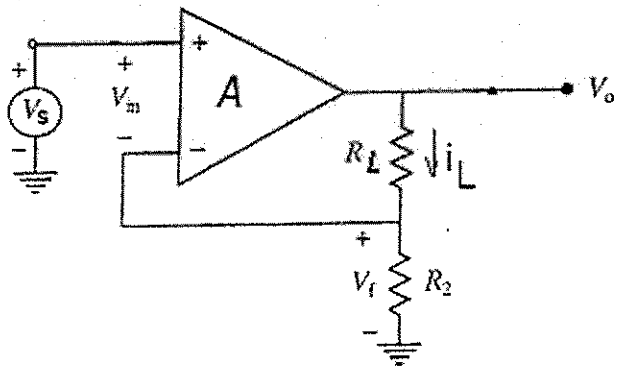


Figure 3

The End

BITS PILANI DUBAI CAMPUS **SET B**

ECE / INSTR C364 ANALOG ELECTRONICS - Quiz 2

Sem2, 2011 - 12 CLOSED BOOK Time Allowed: 20 mins
Total Marks : 10 Weightage: 5%

INSTRUCTIONS : Answer ALL questions

1 For an op amp circuit shown below, all transistors have the same reverse saturation current I_s. Assume room temperature and V_T (= kT/q) value at room temperature is 0.025 V. Inputs v_1 and v_2 are in volts.

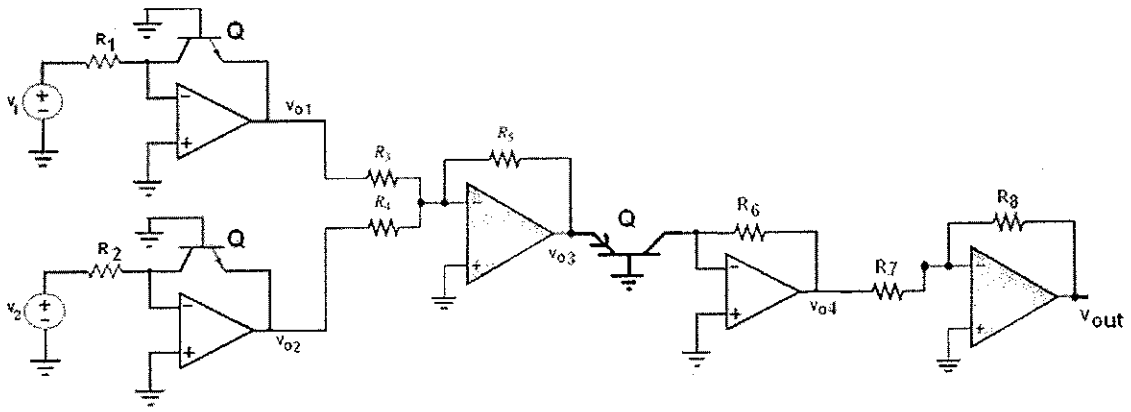


Figure 1

In the above figure, $R_1 = R_2 = R_6 = R$ and $R_3 = R_4 = R_5$ Complete the following table

Find the expressions for v_{o1} and v_{o2}. Assume v_{o1} and v_{o2} to be much greater than V_T	Ans:
It is desired to have v_{o3} in the form of $K_1 \ln[(v_1.v_2)/K_2^2]$. Determine the suitable expression for K_1 and K_2	Ans
Find the expression for v_{o4}. Assume v_{o3} to be much greater than V_T	Ans:
If $v_{out} = v_1.v_2$ obtain the expression for the ratio (R_8/R_7)	Ans:

(1+2+1+2 = 6 marks)

2 Determine the voltage Vo at node A for the following circuit (Fig.2), assuming a silicon diode (0.7 volts typical forward drop). (1 mark)

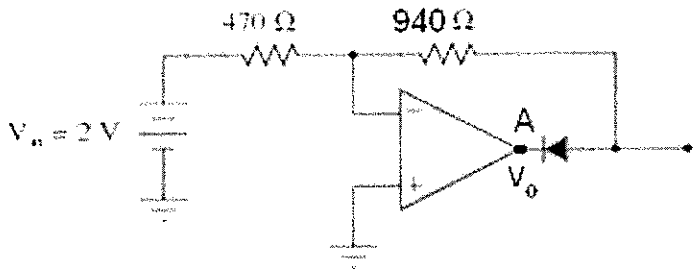
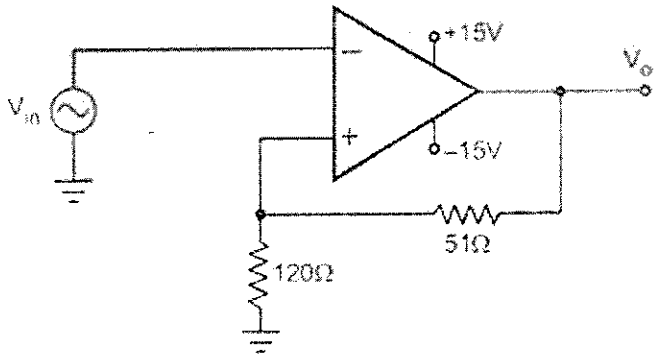


Figure 2

3 In Figure 3, v_{in} = 12sinwt. Calculate the upper and lower threshold voltage levels. Assume Vsat = 0.9 Vcc.Sketch the input and output waveforms.



(3 marks)

NAME: ID. NO. ECE / INSTR C364

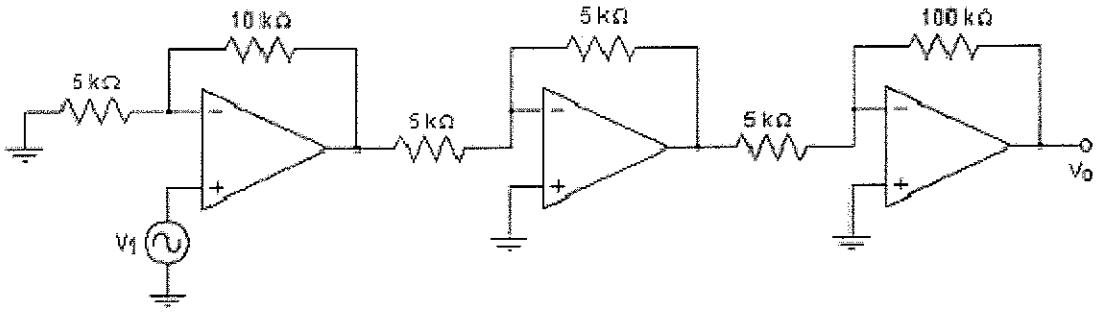
SET A

BITS PILANI DUBAI CAMPUS
ECE / INSTR C364 ANALOG ELECTRONICS - Quiz 1

Sem2, 2011 - 12 CLOSED BOOK Time Allowed: 20 mins
Total Marks : 10 6 Mar 2012 Weightage: 5%

INSTRUCTIONS : Answer ALL questions

1. For an opamp circuit shown below, the output V_o is expected to be 10.08 V. Calculate the input voltage V_I if
(a) the opamps are ideal, and
(b) the opamps have an input offset voltage of V_{os} = 5 mV.



(5 marks)

2. A unity gain amplifier circuit employs an opamp which has a slew rate of 10^6 V/s. A symmetrical square wave of peak-peak value 10 V is applied at the input. Sketch the input and output waveforms if the frequency of the input is
(a) 5 kHz and (b) 62.5 kHz. Find the peak – peak value of the output for each case. Comment on the nature of the output.

(5 marks)

The End

NAME: ID. NO. ECE / INSTR C364

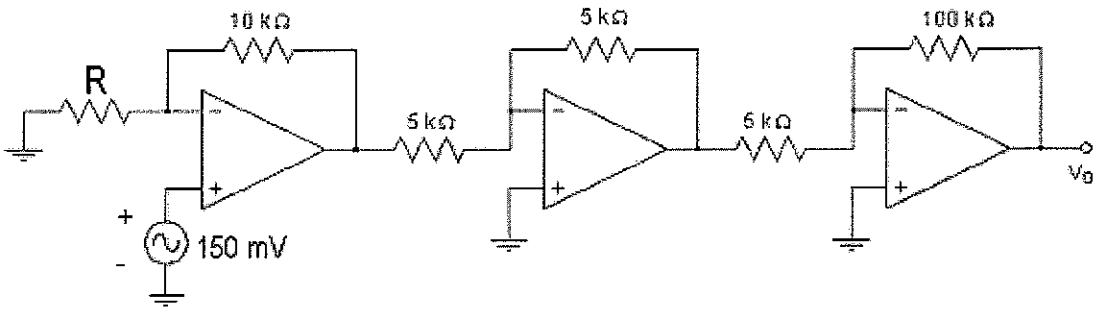
SET B

BITS PILANI DUBAI CAMPUS
ECE / INSTR C364 ANALOG ELECTRONICS - Quiz 1

Sem2, 2011 - 12 CLOSED BOOK Time Allowed: 20 mins
Total Marks : 10 6 Mar 2012 Weightage: 5%

INSTRUCTIONS : Answer ALL questions

1. For an opamp circuit shown below, the output V_o is expected to be 10.08 V. Calculate the resistance R if
   (a) the opamps are ideal, and
   (b) the opamps have an input offset voltage of V_{os} = 10 mV.



(5 marks)

2. A unity gain amplifier circuit employs an opamp which has a slew rate of 10^6 V/s. A symmetrical square wave of peak-peak value 10 V is applied at the input. Sketch the input and output waveforms if the frequency of the input is (a) 10 kHz and (b) 125 kHz. Find the peak – peak value of the output for each case. Comment on the nature of the output

(5 marks)

The End