BITS PILANI, DUBAI CAMPUS

DIAC, DUBAI

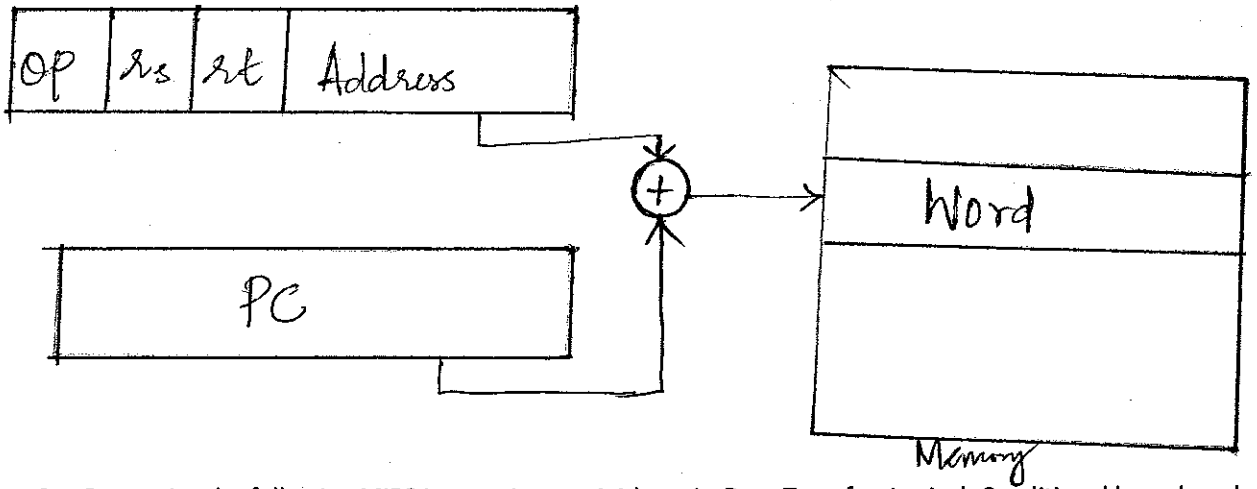
II SEMESTER 2011-12

COURSE	:	CS C342 ADVANCED COMPUTER ORGANIZATION
YEAR	:	III YEAR COMPUTER SCIENCE
COMPONENT	:	COMPREHENSIVE EXAMINATION
DATE & DURATION	:	07-06-2012 & 3 HOURS
WEIGHTAGE (%)	:	40 % (40 MARKS)
NO. OF PAGES	:	2 PAGES

NOTE: Answer all the questions. Give proper design wherever required.

1. Consider a Network Message Transfer program runs on a MAC computer takes 10 seconds and the clock frequency of the machine is 3 GHz clock. You have been asked to help the system architecture designer to build a computer X, which will run the same program in 5 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer X to require 1.2 times as many clock cycles as MAC computer for this program. What clock rate should you advice the designer to target? 4 Marks
2. Rewrite the below given formula for calculating the CPU time using clock rate; if the formula for calculating CPU Time = Instruction count * CPI * clock cycle Time. 2 Marks
3. Assume that the variable h is associated with register **r3** and the base address of the memory **X** is in **r4** ? What is the MIPS assembly code for the C assignment statement given below? 2 Marks

   X[12] = h + X[8];
4. Convert the 16 bit binary version of **-3** to 32-bit binary number? 1 Mark
5. What the does the following illustration represent? 2 Marks



6. Categories the following MIPS Instructions as Arithmetic, Data Transfer, Logical, Conditional branch and Unconditional Jump. 3 Marks

   i) jal 2500
   ii) sltiu $s1, $s2, 20
   iii) beq $s1, $s2, 25
   iv) lui $s1, 20
   v) sh $s1, 20($s2)
   vi) addi $s1, $s2, 20

7. Give the improved version of Division Hardware. What are changes you have observed when compared with the initial version of the Hardware design. 3 Marks

8. Draw a datapath diagram that perform the following: 2 Marks

   i) Fetching the instructions
   ii) Incrementing the program counter
   Why do you need to increment the program counter? Show them clearly in the datapath diagram.

9. Using the following components, draw a datapath diagram that will demonstrate the branch instruction. The component are: 4 Marks

   i) ALU
   ii) Two Adders
   iii) PC
   iv) Instruction Memory
   v) Register
   vi) Sign Extend
   vii) Shift left2

10. Give the asserted effect of each of the seven control signals in a full-fledged datapath diagram? 7 Marks

11. Give the graphical representation of forwarding and stalling effect if needed for the following MIPS code?

    lw $s0, 20($t1) 2 Marks
    sub $t2, $s0, $t3

12. What is formula for calculating the "Time between Instructions pipelined" in a single cycle MIPS execution? 1 Mark

13. Give the pipelined diagram for the given set of instructions: 2 Marks

    lw $s2, 20($s1)
    and $s4, $s2, $s5
    or $s8, $s2, $s6
    add $s9, $s4, $s2

14. Let us consider a cache with 64 blocks and a block size of 16 bytes. To what block does byte address 1200 map? 2 Marks

15. Assume the miss rate of an Instruction cache is 3% and the miss rate of the data cache is 5 %. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed and assume the frequency of all loads and stores is 36%. 3 Marks

BITS PILANI, DUBAI CAMPUS

International Academic City, Dubai

Second Semester 2011 – 2012

Advanced Computer Organization CS C342 (III year CS)

Test – 2 (Open Book)

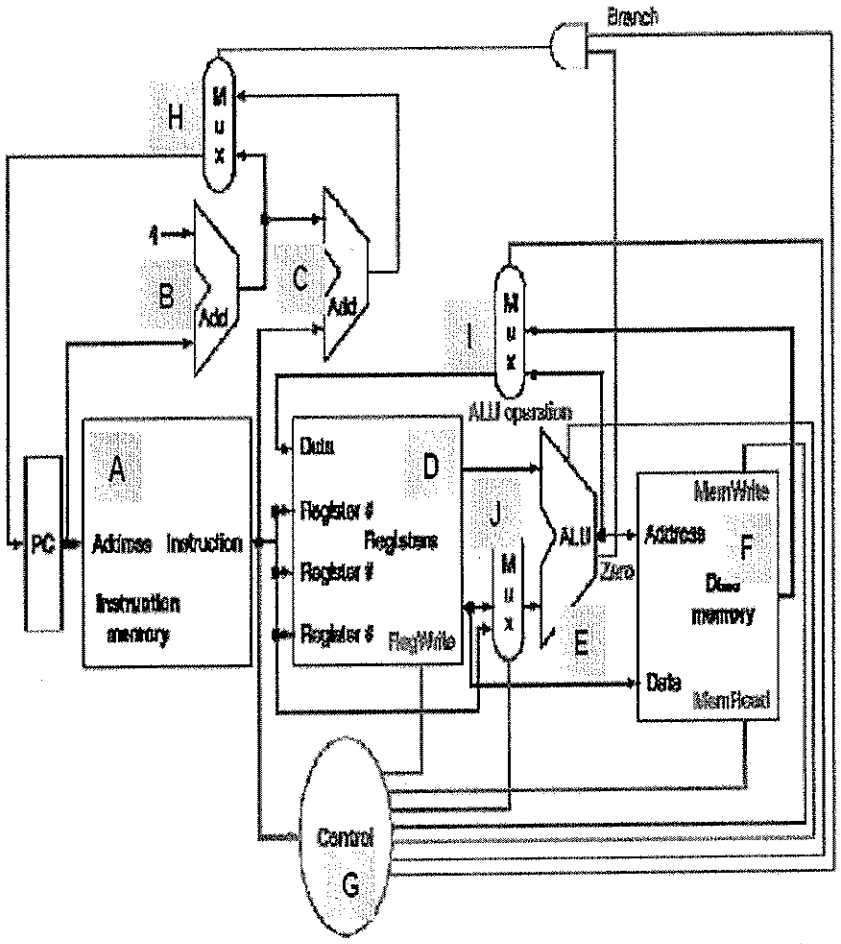
Duration: 50 minutes | Weightage: 20%

Date: 26.04.2012 | MAX Marks: 20 Marks

No. of pages: 02

ANSWER ALL QUESTIONS

1. For questions (a), (b) and (c), consider the following simplified MIPS datapath **3 x2 = 6 M**



The datapath supports the following instructions: add, sub, and, or, slt, beq, lw and sw.

a) Referring to the labels **A** through **J** in the datapath diagram above, which components are required during the execution of a **lw** instruction? (Ignore the PC for this question.)

b) What is the critical path for the **lw** instruction? Mention them in terms of the labels as per the above diagram.

c) Referring to the labels **A** through **J** in the datapath diagram above, which components are required during the execution of a **beq** instruction? And also mention what are the components not required for this instruction?

2. What do mean by state elements and combinational elements? List two components for state and combinational elements. Which element in the data path diagram is called data selector? **2 M**

3.
   a. Write the format, description and the sequence of steps involved in the execution of the **jal** instruction. **1.5 M**
   b. Draw the single cycle data path of the **jal** instruction. Add necessary data paths and control signals to the single cycle data path of MIPS and justify the need for the modifications, if any. **3.5 M**

4. For each of the **pipelined code sequence** given in (a) and (b) below identify whether a data dependence exists or not. If there exists a data dependence which leads to a data hazard mention the type of action required to overcome it. **2 x 2 = 4 M**

   a)
   ```
   lw  R1, 45(R2)
   add R5, R1, R7
   sub R8, R6, R7
   or  R9, R6, R7
   ```

   b)
   ```
   lw  R1, 45(R2)
   add R5, R6, R7
   sub R8, R6, R7
   or  R9, R1, R7
   ```

   c) Consider the following MIPS assembly code: **3 M**

   ```
   add $s3, $s2, $s3
   lw $s4, 100($s3)
   sub $s7, $s6, $s2
   xor $s6, $s4, $s3
   ```

Assume there is no forwarding or stalling circuitry in a pipelined processor that uses the standard 5-stages (IF, ID, EX, Mem, WB). Instead, we will require the compiler to add no-ops (no –operations) to the code to ensure correct execution. (Assume that if the processor reads and writes to the same register in a given cycle, the value read out will be the new value that is written in.) Rewrite the code to include the no- ops (no – operations) that are needed. Do not change the order of the four statements. Use as few no- ops as possible.

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BITS PILANI, DUBAI CAMPUS
II SEMESTER 2011-12

COURSE	:	**CS C342 Advanced Computer Organization**
Year	:	**III Year Computer Science**
Component	:	**Test I**
Date & Duration	:	**11-03-12 (Sunday) & 50 Mins.**
Weightage (%)	:	**25 % (25 Marks)**
Nature of Component	:	**Closed Book**

Note: Answer all the Questions.

1. What do you mean by Multi-Core Processors? (2 Mark)
2. What is the use of datapath in a central processing unit? (2 Marks)
3. If Computer **Y** executes a program in 8 seconds and computer **X** executes the same program in 15 seconds, how much faster is **Y** than **X**? (3 Marks)
4. Let **MM** is the name of the computer and it has a clock cycle time of 250 ps and a CPI of 2.0 for executing a program, and **ZZ** is another computer has a clock cycle of 500ps and the CPI of 1.2 for executing the same program. Which computer is faster for the above mention program and how much? (3 Marks)
5. Consider two different implementation of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

Processors	Clock rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	1.5 Ghz	1	2	3	4
P2	2 Ghz	2	2	2	2

Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? (4 Marks)

6. Give the MIPS assembly code for the following high level assignment statement
A[12]= h + A[8]; (2 Marks)
7. What is the decimal value of this 32 bit two's complement number? (1 Marks)
$$11111111111111111111111111111100_{two}$$
8. Give the four design principles for hardware design? (2 Marks)
9. Explain the MIPS PC-relative addressing mode with a neat diagram. (2 Marks)
10. Explain the multiplication algorithm and the refined version of the multiplication hardware block diagram. (4 Marks)

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II SEMESTER 2011-12

COURSE	**: CS C351 ADVANCED COMPUTER ORGANIZATION**	
YEAR	**: III CS**	
COMPONENT	**: QUIZ 2**	**DATE: 22-5-2012**
MARKS	**: 7 MARKS**	
DURATION	**: 20 MINS**	

Name: _____

Id. No.: _____

Version: A

Note: Answer all the questions.

1. The _____ states that the program accesses a relatively small portion of their address space at any instant of time, just as you accessed a very small portion of the library's collection. (½ Mark)
2. The _____ is the fraction of memory accesses not found in the upper level, it is also used as a measure of the performance of the memory hierarchy. (½ Mark)
3. The time required to fetch a block into a level of the memory hierarchy from the lower level, including the time to access the block, transmit it from one level to the other, insert it in the level that experienced the fail to notice, and then pass the block to the requestor. This is called _____.

   a) Hit time b) miss penalty c) seek time d) access time (½ Mark)
4. The _____ is the fraction of memory accesses found in the upper level; it is often used as a measure of the performance of the memory hierarchy. (½ Mark)
5. The Direct-mapped cache is cache structure in which each memory location is mapped to exactly one location in the cache. (True / False) (½ Mark)
6. A Tag field is used to select the block and a cache index is used to compare with the value of the tag field of the cache. (True / False) (½ Mark)
7. The total number of bits in a direct-mapped cache is _____.

   a) 2^n * (block size +tag size + value field size) (1 Mark)

   b) 32-(n-m++2)

   c) 2^n*(2m*32+(32-n-m-2)+1)

   d) None of the above

8. How many total bits are required for a direct-mapped cache with 16KB of data and 4-word blocks, assuming a 32 bit address? (2 Marks)

9. If we have a cache block of four words and one-word-wide bank of DRAMs, the miss penalty would be 65 memory bus cycles. Calculate the number of bytes transferred per bus clock cycle for a single miss? (1 Mark)

BITS PILANI, DUBAI CAMPUS

II SEMESTER 2011-12

COURSE	**: CS C351 ADVANCED COMPUTER ORGANIZATION**	
YEAR	**: III CS**	
COMPONENT	**: QUIZ 2**	**DATE: 22-5-2012**
MARKS	**: 7 MARKS**	
DURATION	**: 20 MINS**	

Name: _____

Id. No.: _____

Version: B

Note: Answer all the questions.

1. The _____ is the fraction of memory accesses not found in the upper level, it is also used as a measure of the performance of the memory hierarchy. (½ Mark)
2. The time required to fetch a block into a level of the memory hierarchy from the lower level, including the time to access the block, transmit it from one level to the other, insert it in the level that experienced the fail to notice, and then pass the block to the requestor. This is called _____.

   a) Hit time b) miss penalty c) seek time d) access time (½ Mark)
3. The _____ is the fraction of memory accesses found in the upper level; it is often used as a measure of the performance of the memory hierarchy. (½ Mark)
4. The _____ states that the program accesses a relatively small portion of their address space at any instant of time, just as you accessed a very small portion of the library's collection. (½ Mark)
5. The Direct-mapped cache is cache structure in which each memory location is mapped to exactly one location in the cache. (True / False) (½ Mark)
6. If we have a cache block of four words and one-word-wide bank of DRAMs, the miss penalty would be 65 memory bus cycles. Calculate the number of bytes transferred per bus clock cycle for a single miss? (1 Mark)
7. A Tag field is used to select the block and a cache index is used to compare with the value of the tag field of the cache. (True / False) (½ Mark)

8. The total number of bits in a direct-mapped cache is _____.

   a) 2^n * (block size +tag size + value field size) (1 Mark)

   b) 32-(n-m++2)-1

   c) 2^n*(2m*32+(32-n-m-2)+1)

   d) All of the above

9. How many total bits are required for a direct-mapped cache with 16KB of data and 4-word blocks, assuming a 32 bit address? (2 Marks)

BITS Pilani, Dubai Campus

II Semester 2011-12

Course	:	CS C342 Advanced Computer Organization
Year	:	III Year Computer Science
Component	:	Quiz 1 (Closed Book)
Weightage	:	8 % (8 Marks)
Duration & Date	:	20 mins. & 3-3-2012(Tuesday)

A

Name: _____ Id. NO.: _____

1. What is the processor elements involved in the process fetching the instructions? (1 ½ Mark)

Ans:

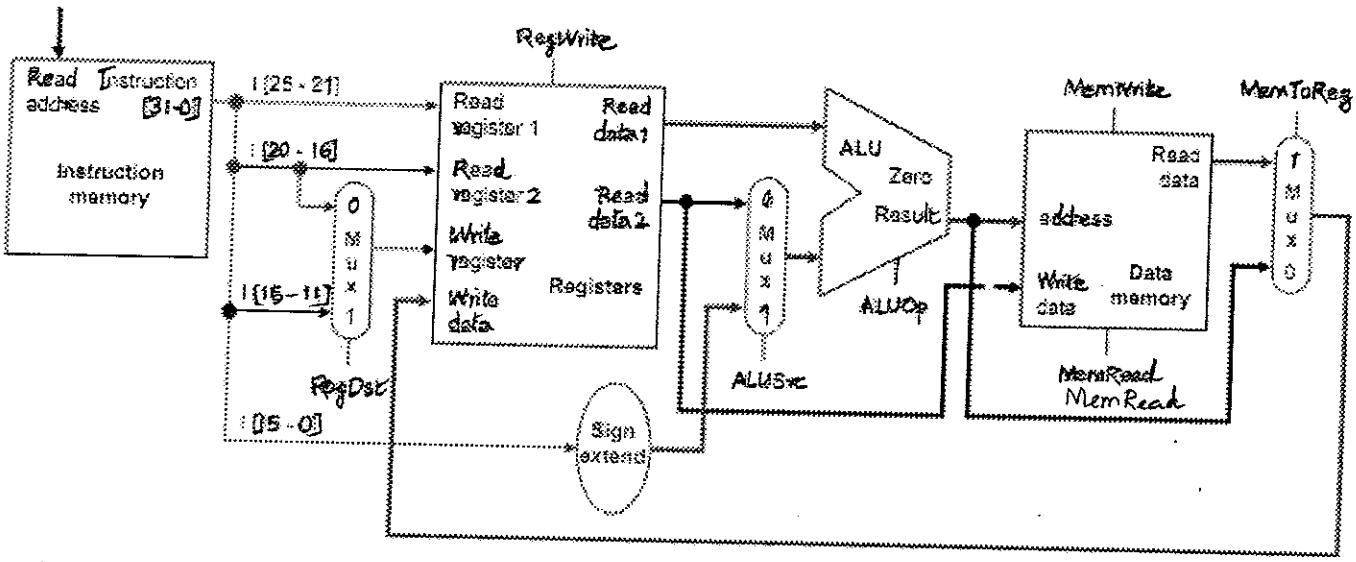
2. What is the processor elements used to access R-Type instructions? (½ Mark)

Ans:

3. Give the datapath diagram for executing an R-Type instruction using the following components: (1 ½ Marks)

Ans:

4. What does the following datapath diagram represent? (1 ½ Marks)



Ans:

5. What are the 13 bits inputs used to generate control signals in a single-Cycle MIPS Procesor *like RegDst, RegWrite, ALUScr, ALUOP, MemWrite, MemRead, MemToReg & PCScr* ? (1 ½ Marks)

Ans:

6. For executing a beq instruction three stages are involved, mention them? (1 ½ Marks)

Ans: