BITS PILANI, DUBAI CAMPUS

SECOND SEMESTER 2010- 2011

THIRD **YEAR (COMPREHENSIVE EXAMINATION)**

Course Code: EEE C461 / INSTR C461 — Date: 26-05-2011
Course Title: POWER ELECTRONICS — Max Marks: 40
Duration: 12.30 -3.30 PM (3 Hours) — Weightage: 40%

- *Answer all the questions*
- *Any missing data can be suitably assumed*

1. Explain the following with respect to a Thyristor — 5
   a) Two transistor model
   b) I-V Characteristics
   c) Turn On Characteristics with proper waveforms
   d) Turn Off characteristics with proper waveforms

2 a) Explain turn-off operation of a GTO and derive an expression for turn-off gain — 4

   b) Draw the circuit diagram of an electrically isolated base drive circuit, which makes use of small high frequency pulse transformer, where modulation of high frequency is done with low frequency control signal — 2

3. Design a Class A or self commutation circuit for a thyristor to conduct for 0.5msec after it has been fired using positive gate pulse at $\alpha=0^{\circ}$. Assume zero initial conditions and $R_L=100\Omega$, L=10mH. — 5
   If input voltage V=300V, what is the peak value of the thyristor current.

4. With a neat circuit diagram explain boost converter? Derive an expression for average value of the inductor current at the boundary between continuous and discontinuous time conduction. — 6
   In a step up converter consider all the components to be ideal Let V_d be 8-16 V, V_o=24V (regulated), f_s=20kHz and C=470 μF. Calculate L_{min} that will keep the converter operating in a continuous conduction mode if $P_o \geq 5W$.

5	With a neat circuit diagram and waveforms , explain 3 phase ac – dc fully controlled rectifier	4
6	With a neat circuit diagram and waveforms explain the Cuk converter and derive the expression for (v_o/v_d)	5
7	With a neat circuit diagram and waveforms explain single phase full bridge inverter with RL load	4
8	A single phase full bridge inverter using thyristor is connected to RL load. For a dc source voltage of Vs and output frequency f=1/T , derive the expressions for the steady state load current as a function of time for first two half cycles.	5

********WISH YOU ALL THE BEST**********

BITS PILANI, DUBAI CAMPUS

SECOND SEMESTER 2010- 2011

THIRD **YEAR (TEST-2 OPEN BOOK)**

Course Code: EEE C461 / INSTR C461
Course Title: POWER ELECTRONICS
Duration: 50 minutes

Date: 08-05-2011
Max Marks: 20
Weightage: 20%

- *Answer all the questions*
- *Any missing data can be suitably assumed*
- *Only prescribed text book and handwritten notes are allowed.*

1. Figure1 shows a self commutating circuit. The inductance carries an initial current of 200 A, and the initial voltage across the capacitor is V, the supply voltage. Determine the conduction time of the SCR and the capacitor voltage at turn off. 3

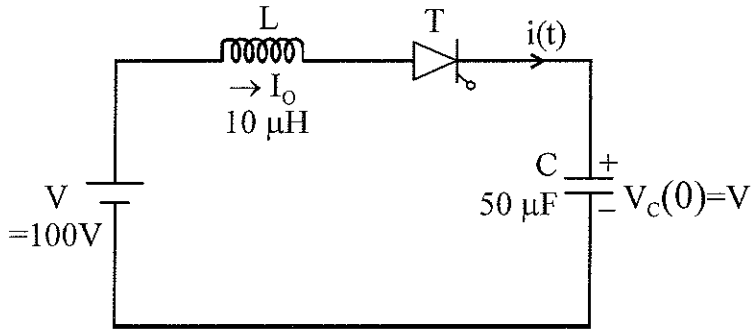

Figure 1.

2 Derive an expression for ΔV_0 (peak-peak) for a step down converter in a discontinuous conduction mode in terms of the circuit parameter. 4

3. In a Buck boost converter V_d=12V, V_0=15V, L=150μH, C=470μF, and f_s=20KHz. Calculate ΔV_0 if the I_0 is equal to $\frac{1}{2} I_{oB}$ 3

4. In a single phase rectifier shown in Figure2. V_s=200V at 60Hz, L_s=10 mH and V_d=150V, draw the waveform for i_d and indicate the values of θ_b, θ_f, I_{dpeak}. Also calculate the average value of I_d. 3

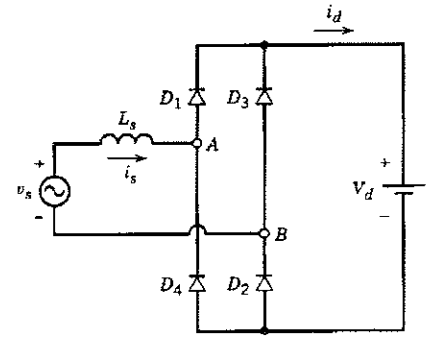

Figure 2

5. In a single phase rectifier circuit shown in Figure3. Vs=150V at 60Hz, Ls= 5mH, and I_d=15A. 3
Calculate u (commutation interval) , V_d and P_d. What is the percentage voltage drop in V_d due to L_s.

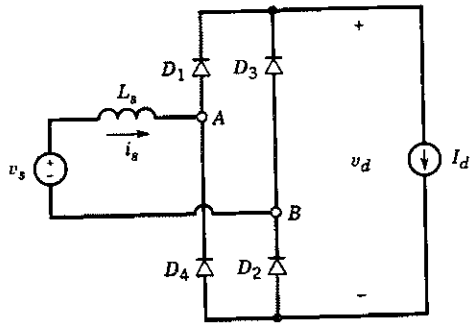

Figure 3.

6. In a step up converter , consider all components to be ideal. Let V_d be 8-16 V, V_o=24V (regulated), f_s=20KHz, and C=470μF, Calculate L_{min} that will keep the converter operating in a continuous conduction mode if $P_0 \geq 5W$ 2

7 In a three phase converter shown in Figure7 V_{LL}=460V at 60Hz and L_s=25μH. Calculate the commutation angle u if V_d=525V and P_d=500kW 2

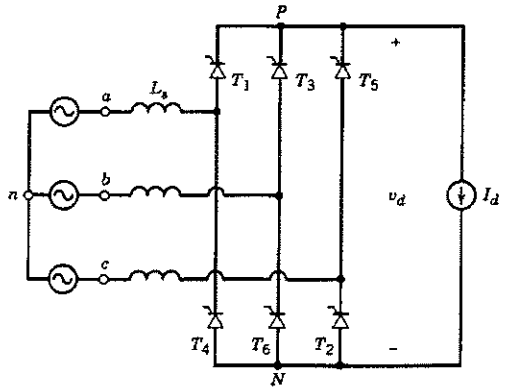

Figure 7.

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SECOND SEMESTER 2010- 2011

THIRD YEAR (TEST-1)

Course Code: EEE C461 / INSTR C461 | Date: 20-03-2011

Course Title: POWER ELECTRONICS | Max Marks: 25

Duration: 50 minutes | Weightage: 25%

- *Answer all the questions*
- *Any missing data can be suitable assumed*

1. With a two BJT model and corresponding mathematical current expressions, explain the working principle of a thyristor 4

2. Explain the major differences between a thyristor and a GTO? Explain turn on and turn off characteristics of a GTO. 3

3. What is quasi-saturation region in power BJT? Explain 3

4. Explain the working principle of an IGBT with its structure. Draw an MOSFET-BJT equivalent for the IGBT. 4

5. Consider a Schottky diode that has an n type drift region with a donor doping density of $10^{15}/cm^3$ and a drift region length of 20μm. The diode is to carry 100 A of current in the ON state with a maximum drift region drop of 2V. What should be the cross section area of the diode be. 4

6. Following are the specification of a thyristor operating from a peak supply of 500V. 4

   Peak current = 125A

   $(di/dt)_{max}$=30 A/μs

   $(dv/dt)_{max}$=100 V/ μs

   Design a snubber circuit if the minimum load resistance is 20Ω

7. Derive an expression for the turn-off gain of a GTO 3

**********WISH YOU BEST OF LUCK**********

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SECOND SEMESTER 2010- 2011

THIRD **YEAR (QUIZ-II)**

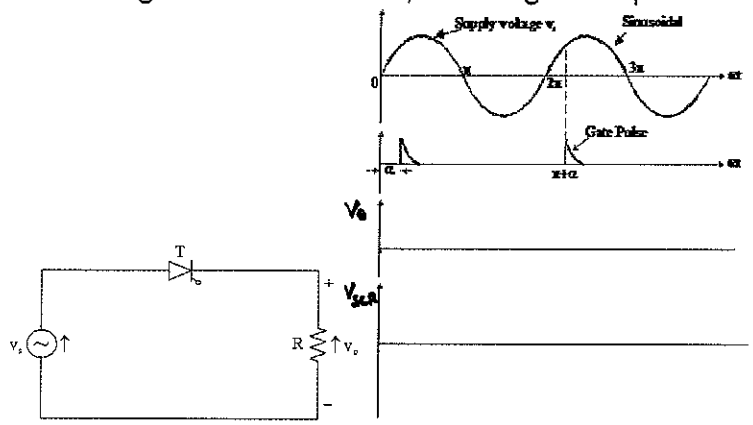
Course Code: EEE C461 / INSTR C461 | Date: 13-03-2011
Course Title: POWER ELECTRONICS | Max Marks: 7
Duration: 20 minutes | Weightage: 7%

Name: . . . . . **ID No:** . . . . . **Sec / Prog:** . . . . . .

SET A

Important Note: Strictly write the Answers in the space provided.

1 For the following thyristor circuit , sketch the waveforms for the load voltage (v_o) and voltage across the SCR, for the given input. 1M



2 Calculate the conduction time of SCR in the circuit employing series resonant commutation (self commutation or class A commutation), if the supply voltage is 200 V, C = 1μF, L = 10 mH and R_L = 200 Ω. Assume that the circuit is initially relaxed. 0.5M

Ans:_____

3 Draw the circuit diagram of a dc coupled base current drive circuit for power BJT using comparator and BJT. 2M

4 Consider all the components to be ideal in a step down dc-dc converter. Assume V_o=5V, f_s=50KHz, L=2mH, and C=220μH. Check whether the converter is working in continuous conduction mode or discontinuous conduction mode if V_d=10.6V and I_o=100mA. (Give proof) 1M

Proof:

Answer: _____

5 Consider following for the boost converter, V_d=12V, V_o=24V, I_o=0.5A, L=150μH, C=470μF, and f_s=20kHz. Identify which one of the following case the converter is working. (Give proof) 1M

Proof:

a) Boundary case
b) Continuous conduction case
c) Discontinuous conduction case

6 For a Cuk converter Vd=10V and output is regulated to be constant at 5V, what is the duty ratio. 0.5M

Answer: _____

7 Draw the circuit diagram of the step-up dc-dc converter 1

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Duration: 20 minutes — Weightage: 7%

Name: ..... **ID N :** ..... **Sec / Pr g:** .....

SET B

Important Note: Strictly write the Answers in the space provided.

1 Draw the circuit diagram for the load commutation of a thyristor

1M

2 Calculate the conduction time of SCR and the peak SCR current that flows in the circuit employing series resonant commutation (self commutation or class A commutation), if the supply voltage is 100 V, C = 2μF, L = 500 mH and R_L = 300 Ω. Assume that the circuit is initially relaxed. 0.5M

Ans:_____

3 Draw the schematic diagram of an Optocoupler based drive circuit.

2M

4 Given the following for the Buck-Boost converter, V_d=12V, V_o=15V, I_o=250mA,L=150μH, fs=20KHz. Check whether the converter is working in continuous conduction mode or discontinuous conduction mode. (Give proof) 1M
Proof:

Ans: _____

5 Write any one advantage and disadvantage of Cuk converter over buck boost converter. 1M

Advantage:

Disadvantage:

6 Write the expression for the conversion ratio of buck converter working in discontinuous conduction mode in terms of the duty ratio. 0.5M

Ans:

7 Draw the circuit diagram of a step down converter. 1

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SECOND SEMESTER 2010- 2011

THIRD YEAR (QUIZ-1)

Course Code: EEE C461 / INSTR C461
Course Title: POWER ELECTRONICS
Duration: 20 minutes

Date: 09-03-2011
Max Marks: 8
Weightage: 8%

Name: ..... **ID No:** ..... **Sec / Prog:** .....

SET A

1 What is the required drift region thickness (W_d), for a non punch through power diode with breakdown voltage of 2000V 1M

_____ μm

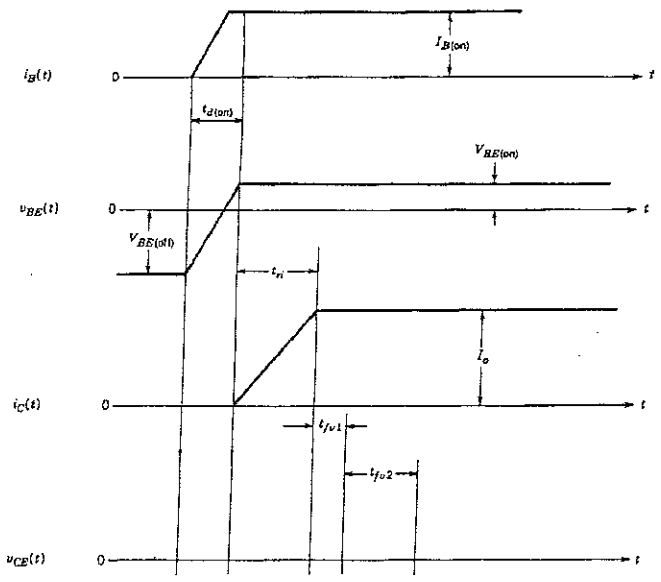
2 The thickness of the drift region in power diode depends on _____ 0.5M

3 The reverse recovery time of a diode is t_{rr}=3μs and the rate of fall of the diode current is di/dt = 30A/ μs. Determine the storage charge Q_{RR} and the peak inverse current I_{RR} 2M

Q_{RR}=

I_{RR}=

4 Following is the turn on characteristic of a power BJT. Draw the corresponding $v_{CE}(t)$ 1M



5 The major observable difference between the i-v characteristics of a power BJT and those of logic level BJT is the region labeled _____ 0.5M

6 In an n-channel power MOSFET, the effect of parasitic npn BJT can be minimized by _____ 0.5M

7 Draw the two BJT model of a Thyristor and indicate the various currents. 1M

8 When the thyristor is in forward blocking state, both the transistors in the two BJT model of a thyristor is in _____region 0.5M

9 Which of the following device can be turned on and turned off using its gate connection? Ans: _____ 0.5M
   a) Thyristor
   b) Power Diode
   c) GTO
   d) Power BJT

10 The width of the p2 layer in GTO thyristor is _____ than that of conventional thyristor. 0.5M

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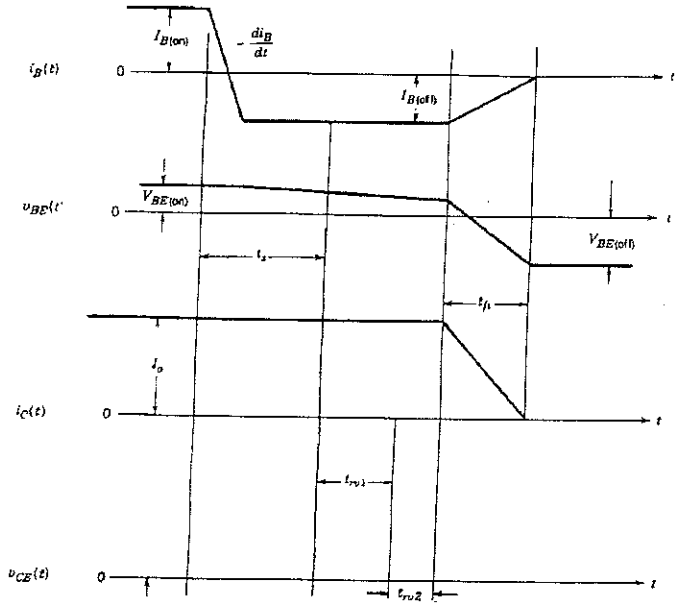
Name: ..... **ID No:** ..... **Sec / Prog:** .....

SET B

1 Following is the turn off characteristic of a power BJT. Draw the corresponding $v_{CE}(t)$ 1M



2 A non punch through diode is to have a breakdown voltage of 2500V. Estimate the doping density of the drift region. 0.5M

_____

3 In an n-channel power MOSFET, the effect of parasitic npn BJT can be minimized by _____ 0.5M

4 Draw the two BJT model of a Thyristor and indicate the various currents. 1M

5 IGBT is a _____ controlled device 0.5M

6 In power BJT, as the excess charge carrier built up in the drift region being to occur, the _____ region of the i-v characteristics is entered. 0.5M

7 In Non punch through IGBT, inclusion of n+ buffer layer is necessary. 0.5M

Indicate above statement is TRUE or FALSE Ans: _____

8 What is the required drift region thickness (W_d), for a punch through power diode with breakdown voltage of 5000V 1M

_____ μm

9 When the thyristor is in ON state, both the transistors in the two BJT model of a thyristor is on _____ region 0.5M

10 The reverse recovery time of a diode is t_{rr}= 5μs and the rate of fall of the diode current is di/dt = 50A/ μs. Determine the storage charge Q_{RR} and the peak inverse current I_{RR} 2M

Q_{RR}=

I_{RR}=