# BITS, PILANI DUBAI CAMPUS

International Academic City, Dubai

## Year III – Semester II 2010– 2011

**COMPREHENSIVE EXAMINATION**

**Course No.: ECE / EEE / CS C 391** **Course Title: DECO**

Date: 8th JUNE, 2011 Time: 3Hours Max. Marks = 120

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Clearly indicate the assumptions made if any

**Answer questions Part A and Part B separately**

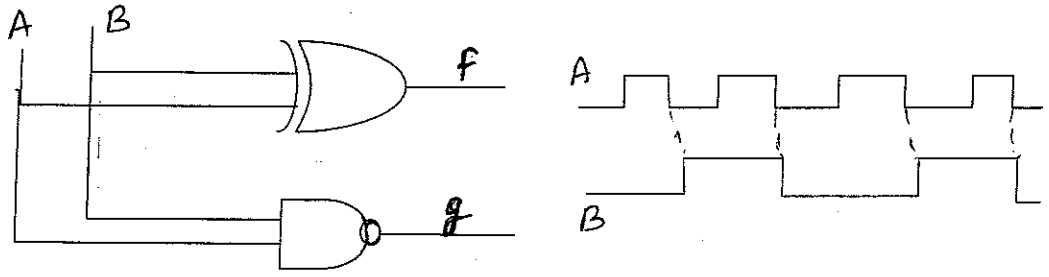
**Calculators are not allowed**

**PART A**

1 a) Express the following numbers in decimal:
(i) $(10110.0101)_2$ (ii)$(16.5)_{16}$ (iii) $(26.24)_8$ (3 x 2M)

b) What are the maximum and minimum numbers that can be represented using 8 bits in two's complement form (2M)

c) Draw the output waveforms of **f** and **g** for the inputs A and B shown in figure (4M )




2. Draw the K-map for the five variable function given by
F(A, B, C, D, E) = (AB'+CD')E+BC'(A+B) (4M)
Also Draw the simplified multi-level NOR and multi-level NAND circuits for the same (3 +3M)

3 a) Use a 4 x 1 multiplexer to implement the following function. It is required that minimum external logic gates to the MUX are to be used. The data select inputs are A and B. Assume A is the MSB.
F ( A,B,C,D ) = Σ (0,4,5,7,8,9,13,15) (5M)

b) Use a 4 x 16 line active low decoder and two input external NAND gates to implement the above function given in Q3 a). (5M)

4 a) List the PLA programming table for the four bit gray to binary code converter. Optimize the no. of product terms for true outputs. (5M)

b) Draw a neat circuit and explain the function of each component of a tristated TTL NAND gate circuit (5M)

5 a) Design a 4 input priority encoder with input $D_0$ having the highest priority and input $D_3$ having the lowest priority. (5M)

b) Design a full adder using half adders and basic logic gates. (5M)

6. Describe the following bus standards employed in a Computer System:

a) Parallel bus standard - General Purpose Interface Bus (GPIB) (6 M)

b) Serial bus standard - RS 232C. (2 M)

(contd .....)

## PART B

7 a) Draw and explain the **logic diagram** to illustrate the working of a 3bit x 2 bit multiplication. Show the working of the circuit using the data 7 and 3 (5M)

b) Explain the working of the integer division algorithm used in computers using **Non-restoration method**. Show the working of 14 / 3 in steps (5M)

8 a) Draw the logic diagram of a 4 x 1 multiplexer using basic logic gates and write its HDL description. (6M)

b) A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are equal to 1, equal to 0 otherwise. Write a Verilog user-defined primitive for a four –bit majority function. (4M)

9. Design a Synchronous counter using JK Flip-flops that goes through the following binary repeated sequence: 0, 3, 1, 7, 6, 4. Show that when binary states 010 and 101 are taken to be don't care conditions, the counter may not operate properly. Find a way to correct the design. (10M)

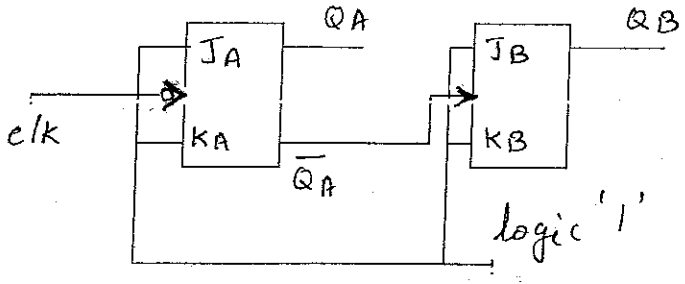
10. The specification of a 7400 IC is given below. Find the Fan-out, Power dissipation, Propagation delay and Noise Margin of the IC (4 x 2.5M)

$I_{OH}$ = 1 mA; $I_{OL}$ = 20mA; $I_{IH}$ = 0.05 mA; $I_{IL}$ = 2 mA;
$I_{CCH}$ = 10mA; $I_{CCL}$ = 20 mA; $t_{PHL}$ = 3ns; $t_{PLH}$ = 4ns;
$V_{CC}$ = 5 V; $V_{OH}$ = 2.7 V; $V_{OL}$ = 0.5V; $V_{IH}$ = 2V; $V_{IL}$ = 0.8 V

11.a) Design a four bit universal shift register using D flip flops and multiplexers which will perform the following operations based on the function table given below. (5M)

| No. | $C_1$ $C_0$ | Function |
|---|---|---|
| 1 | 0 0 | Clear the register |
| 2 | 0 1 | Shift right |
| 3 | 1 0 | Shift left |
| 4 | 1 1 | Load new data |

b) For the asynchronous sequential circuit shown in figure below, draw the complete timing diagram for eight clock pulses showing the clock inputs, $Q_A$, and $Q_B$ waveforms. Assume that $Q_A$ and $Q_B$ are initially cleared. (5M)




12. Given the following state table of a Mealy model sequential circuit with one input, one output and four states, develop the following: (10M)

i) State diagram
ii) Flip Flop input equations (assume that the state memory uses D flip-flops)
iii) Output equation iv) Logic diagram

| S(t) | S(t+1),z | |
|---|---|---|
| | x = 0 | x = 1 |
| A | B,0 | A,0 |
| B | B,0 | C,0 |
| C | D,0 | A,0 |
| D | B,0 | C,1 |

# BITS – PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai

II semester III Year 2010-2011

**Digital Electronics & Computer Organisation - CS / EEE/ ECE C 391**

Test -1I **( Open Book)**

**01– 05 – 11** **Time : 50min.** Max. Marks : 37.5 **Weightage : 12.5 %**

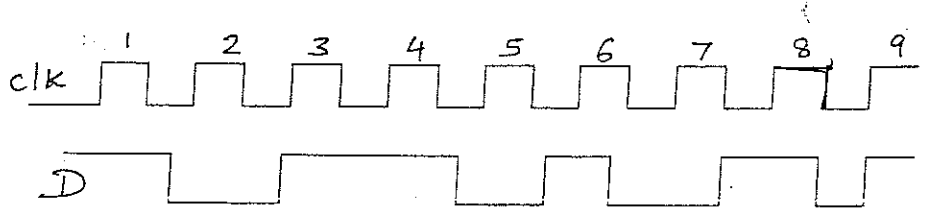
( Answer all questions. Clearly state the assumptions made if any.)

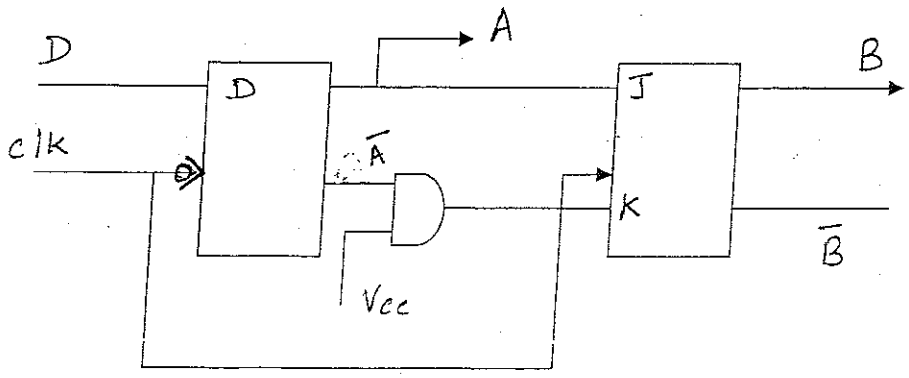
1. The following is a truth table of three-input, four-output combinational circuit: Tabulate the PAL programming table for the circuit. (10)

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| x | y | z | A | B | C | D |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |

2. Given are 128 x 8 ROM ICs with enable input. Show the external connections necessary to construct a 512 x 8 ROM with four such ICs and an active low decoder. ( 9 )

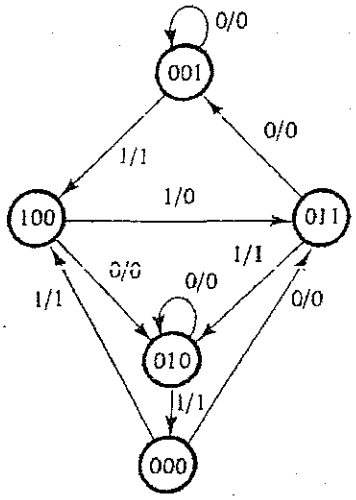
3. In the sequential circuit given below, the input applied to the D flip flop along with the clock pulse applied is shown in Figure 1. Draw the output A and B of the circuit. Assume that the outputs A and B were at zero initially. ( 8 )




(P.T.O)

4. A Sequential Circuit has three flip-flops A, B, C; one input x and one output y. The state diagram is shown below. Design the circuit by treating the unused states as don't care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. Use T flip-flops in the design. Also draw the sequential circuit diagram. ( 10.5 )




********** GOOD LUCK **********

# BITS PILANI, DUBAI CAMPUS

Dubai International Academic City

II semester III Year 2010-2011

**Digital Electronics & Computer Organisation**

EEE C 391 / ECE C391 / CS C391

Test -1 **( Closed Book)**

**10 – 03 – 11** **Time : 50min.** Max. Marks : 37.5 **Weightage : 12.5 %**

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Clearly state all the assumptions made.

**Calculators are not allowed. Assume positive logic**

1. What is the largest binary number that can be expressed with 14 bits? What are the equivalent decimal and hexadecimal numbers. [5 M]

2. Express the Boolean function F = xy + x'z as sum of min terms and product of max terms [5 M]

3. An engine has 4 fail safe sensors. The engine should keep running unless any of the following conditions arise:
   - If sensor B is activated
   - If sensor A and sensor C are activated simultaneously
   - If sensor C and sensor D are activated simultaneously

   a) Derive the truth table for the system
   b) Derive the reduced SOP expression of the above truth table using K-Map simplification. [3+3 M]

4. Simplify the Boolean function: $F(w,x,y,z) = \Sigma(1,3,10) + \Sigma_d(0,2,8,12)$ and implement the circuit using NOR gates alone. [6 M]

5. Explain the construction of a 4 x 1 Mux with three-state buffers and a 2 x 4 decoder. Also show how this circuit can be used as a Half subtraction circuit? . [2+3 M ]

6. Implement a full adder with an active low decoder and two input AND gates alone. Assume x, y and z as adder inputs and it produces outputs S and C. [5 M]

7. Design a logic circuit using basic logic gates to compare two single bit words. Also Write the Boolean expression for a comparator circuit which will compare two four bit words to give the outputs A>B, A<B and A=B [2.5+3 M]

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