BITS PILANI DUBAI CAMPUS

ECE / INSTR C364 ANALOG ELECTRONICS COMPREHENSIVE EXAMINATION

Sem2, 2010 - 11 CLOSED BOOK Time Allowed: 3 Hours
Total Marks : 70 Weightage: 35%

INSTRUCTIONS

1. This paper contains **NINE (9)** questions in two parts A and B, and has FOUR (4) pages. Answer **ALL** questions. Unless specifically stated, all symbols have their usual meanings. Assume suitable data if required.

PART A (Answer all questions in this PART in a separate answer book)

1 (a) Use only one non inverting opamp circuit to implement the following expression:

$$V_0 = V_1 - (V_2 + V_3 + 2)$$

V_1 ,V_2 and V_3 represent dc inputs, and V_o represents the output voltage. In your design, consider the feedback resistor R_f to be 6 kΩ. All other resistors used in the circuit have identical values. Draw the complete circuit diagram

[4 Marks]

(b) Determine the output voltage for the circuit shown in Figure 1. If V_1 = 1 V, V_2 = 2 V, V_3 = 3 V and V_4 = 4 V, how much is V_o ? Limit your calculations to up to four decimal places.

[4 Marks]

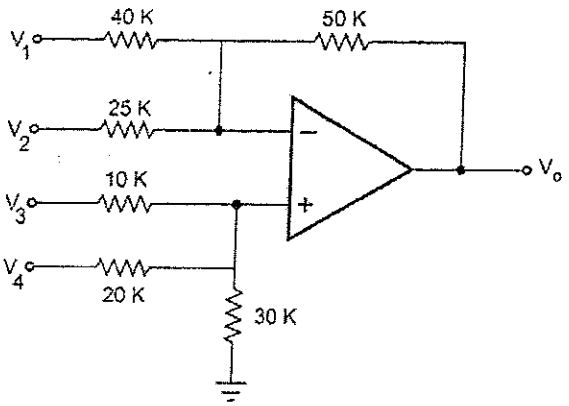

Figure 1

2 (a) Design the circuit of an astable multivibrator using IC555 timer to produce a symmetrical square wave of 1KHz . If V_{cc} = 12 V, draw the waveforms of output and voltage across timing capacitor. Choose C = 0.1μF.

[4 Marks]

(b) Design an opamp based wide band-pass filter using high-pass and low-pass sections. Consider f_L = 200 Hz, f_H = 1 KHz and an overall passband gain of 4. Assume C = 0.05 μF for first order high pass section and C = 0.01 μF for first order low pass section. Draw the complete circuit diagram.

[5 Marks]

3 (a) Explain *Barkhausen criterion* for an oscillator circuit. How will the oscillator circuit's performance be affected if the magnitude of loop gain falls below 1, or goes much above 1?

[2 Marks]

(b) Draw a schematic of an op amp based RC phase shift oscillator. The phase shifting network is made of 3 identical RC sections. The op amp has a maximum input bias current of I_b = 50 nA. Assume that a maximum current through the feedback resistor R_f is $I_{Rf} = 100.I_b$ and the supply voltage for opamp is ± 12 V. Design the oscillator circuit for an output frequency of 1 KHz. Determine all component values required.

[6 Marks]

4. A PLL circuit using IC 565 is shown in Figure 2. Find the values of R_1 and C_2 for the following specifications: Free running frequency is 4.5 KHz, lock range is 2 KHz, Capture range is 100 Hz and supply voltage is ± 10 V.

[5 Marks]

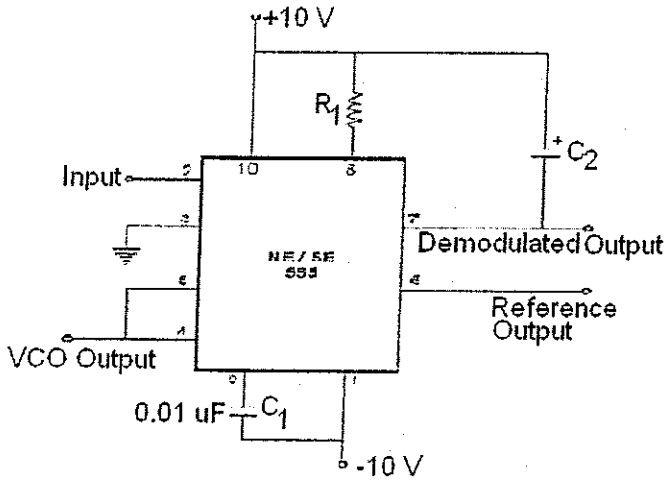

Figure 2

5. In Figure 3, the power supply has an output resistance of 0.2 Ω. The voltmeter reads 51 V when switch S is open. What will be the reading when the switch is closed? Determine the % voltage regulation for the power supply.

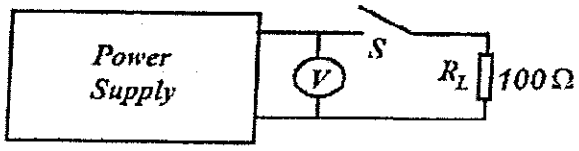

Figure 3

(6 marks)

PART B (Answer all questions in this PART in a separate answer book)

6. Consider the circuit shown in Figure 4. Assume that all opamps are ideal. Also assume that the diodes when forward biased have a voltage drop of 0.7 V and when reverse biased, they are considered open. The load R_L is 10 kΩ.

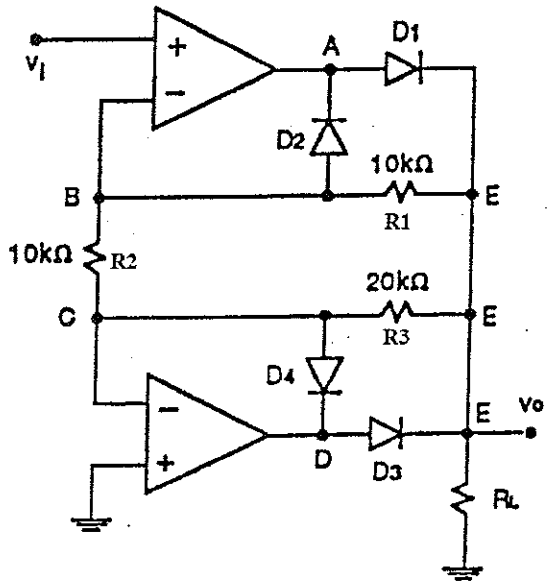

Figure 4

(a) A dc input of $v_I = +5$ V is applied. Determine the voltages at nodes A, B, C, D and E. Also determine the currents through R1, R2 and R3 and through the diodes. Give your answers in a tabular form as below:

V_B	V_C	$V_E = V_0$	V_A	V_D	I_{R2}	I_{R1}	I_{R3}	I_{D2}	I_{D1}	I_{D3}	I_{D4}

(b) The applied dc input is now $v_I = -5$ V. What would be $V_E = V_0$ now?

(c) Based on the output response to an input, what action does the circuit of Figure 2 perform?

(12 marks)

7. Two IC temperature sensors A and B deliver outputs 10 mV/°C and 12 mV/°C respectively.. The outputs of these sensors are used as inputs to a noninverting opamp as shown in Figure 5. The resistor R is of unknown value. When the room temperature is 20°C the output V_o reads 20 mV. Determine the value of R.

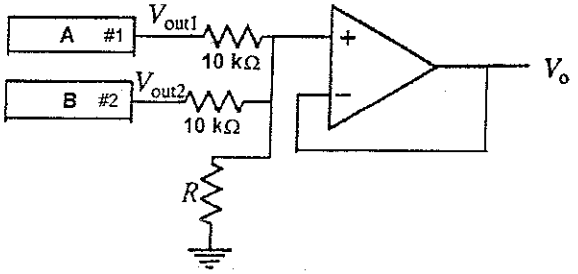

Figure 5

(6 marks)

8. In the circuit of Figure 6, determine the output voltage v_b. Assume that the diode equation is $I_D = I_S.\exp[(V_D/V_T) - 1]$. Give your answer without any simplification

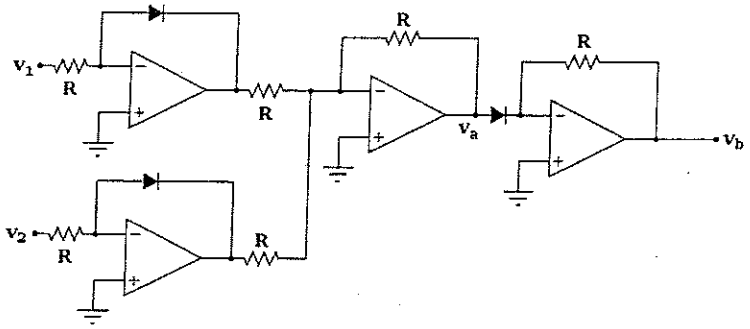

Figure 6

What modification to the circuit is needed to function as a multiplier?

[6 marks]

9. Design a class AB output stage as shown in Figure 7 to meet the following design criteria: The average power delivered to the load is to be 5 W. The peak output voltage is 80% of V_{CC} and the minimum value of diode current is to be no less than 5 mA

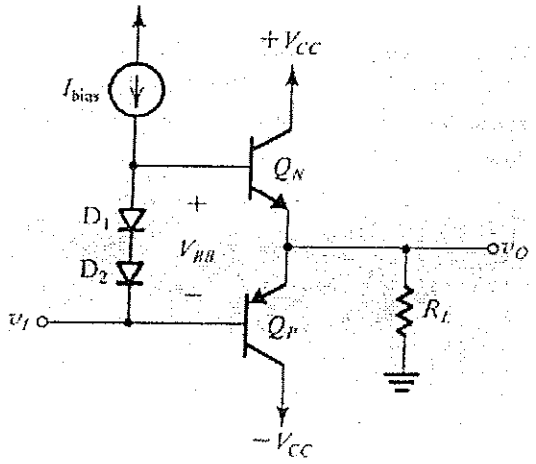

Figure 7

Assume the following: Reverse saturation current of diodes, $I_{SD} = 3x10^{-14}$ A, reverse saturation current of transistors, $I_{SQ} = 10^{-13}$ A, $\beta_{NPN} = \beta_{PNP} = 75$, $R_L = 8\ \Omega$. In the design determine the following: (a) Peak output voltage, V_P (b) V_{CC}, (c) maximum emitter current in Q_N (d) the minimum value of I_{bias} that you would choose, (e) the corresponding value of total diode voltage drop V_{BB} under zero input signal condition and (f) the quiescent collector current I_{CQ} of Q_N and Q_P.

(10 marks)

The End

BITS PILANI DUBAI CAMPUS
ECE / INSTR C364 ANALOG ELECTRONICS - Test 2

Sem2, 2010 - 11 OPEN BOOK Time Allowed: 50 mins
Total Marks : 30 Weightage: 15%

INSTRUCTIONS

1. This paper contains **FOUR (4)** questions and has TWO (2) pages. Answer **ALL** questions. Unless specifically stated, all symbols have their usual meanings. Assume suitable data if required

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1. Distinguish between monostable and astable operations of an IC 555 timer circuit. Design an IC555 timer circuit such that a control door is set to open for a duration of 15 secs after a trigger signal is received. The dc voltage available for the IC is 15 volts. Assume a charging capacitor of 10 μF. Draw the complete circuit diagram and determine all external component values used. Modify the above circuit such that the 15-sec opening of the door is repeated after every 5 secs. Determine the values of any additional components used.

(10 marks)

2. An op-amp based voltage regulator is shown in Figure 1. The zener diode is designed to operate at 10 V, 0.5 A. In the circuit, R_1 = 20 kΩ, R_2 = 10 kΩ. Assuming that the op amp is ideal, determine the following:
   (i) output voltage, V_o,
   (ii) minimum input voltage V_{in}
   (iii) the value of R_3 based on minimum V_{in}.

   If the op-amp is not ideal with an open loop gain of 1000, will the output voltage V_o change? If so, by how much?

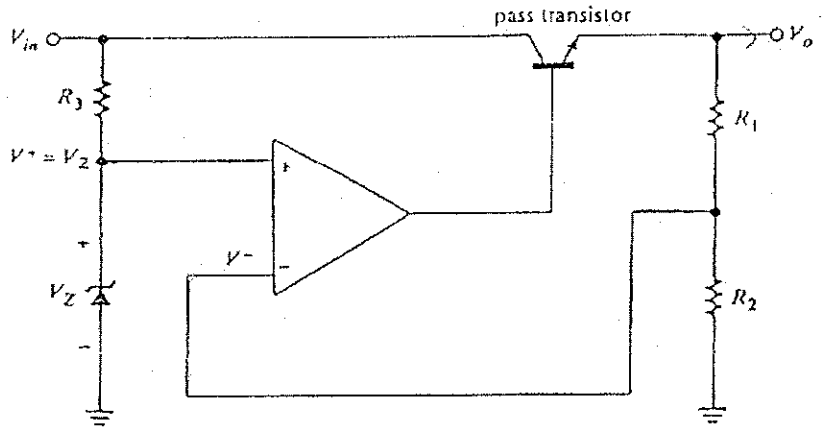


Figure 1

(8 marks)

3. In a Class A power amplifier, the total collector current is given by

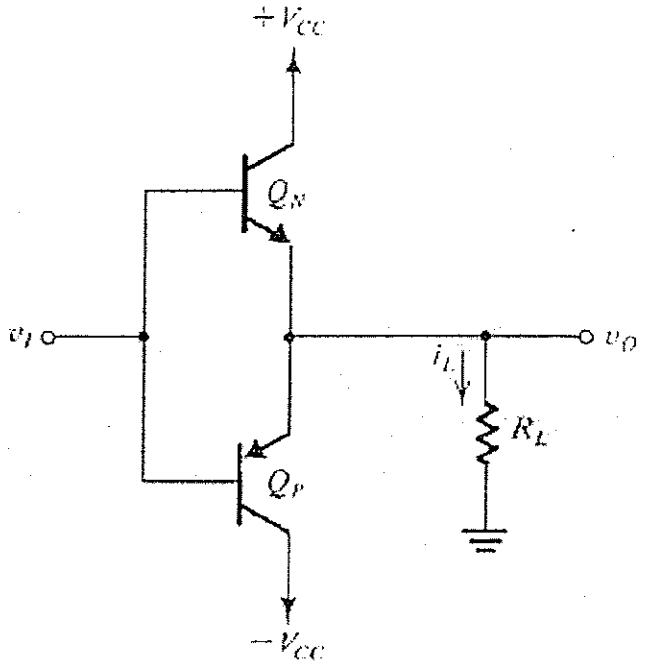
$$i_C = (2.5)(2 + v_{in})^3 \text{ mA}$$

where the input v_{in} (in mV) = 10sinωt. Determine the quiescent collector current, average collector current and the total harmonic distortion for the power amplifier.
Given: $\sin 3\theta = 3\sin\theta - 4\sin^3\theta$

(6 marks)

4. In the circuit below, 20 W average power is delivered to the load with R_L = 10 ohms, when a sinusoidal input is applied. Assuming V_{CE}(sat) for all transistors is zero, determine the power supply voltages used. What is the total average power drawn from power supplies? What is the main drawback of this power amplifier?

(6 marks)



The End

BITS PILANI DUBAI CAMPUS
ECE / INSTR C364 ANALOG ELECTRONICS - Test 1

Sem2, 2010 - 11 CLOSED BOOK Time Allowed: 50 mins
Total Marks : 30 Weightage: 15%

INSTRUCTIONS

1. This paper contains **Five (5)** questions and has TWO (2) pages. Answer **ALL** questions. Unless specifically stated, all symbols have their usual meanings. Assume suitable data if required

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1. A 2 V peak to peak sinusoidal signal source is applied to the input of an inverting op-amp circuit that has R_1 = 5 kΩ and R_f = 47 kΩ. Assume that the opamp is ideal. An a.c voltmeter is connected to the opamp circuit between the output terminal and ground to measure the output voltage. Assume supply voltages to be ± 10 V. Draw the opamp circuit, showing all relevant op-amp pin numbers. Calculate the reading on the voltmeter. If there is a 10% increase in the input signal source, sketch the resulting output waveform.

(5 marks)

2. Find output voltage V_o in terms of V_1 and V_2 for the op-amp circuit shown in the Figure 1. Assume ideal op-amp. What function does the circuit perform? Under what condition is the output independent of the input voltages V_1 and V_2 ?

(8 marks)

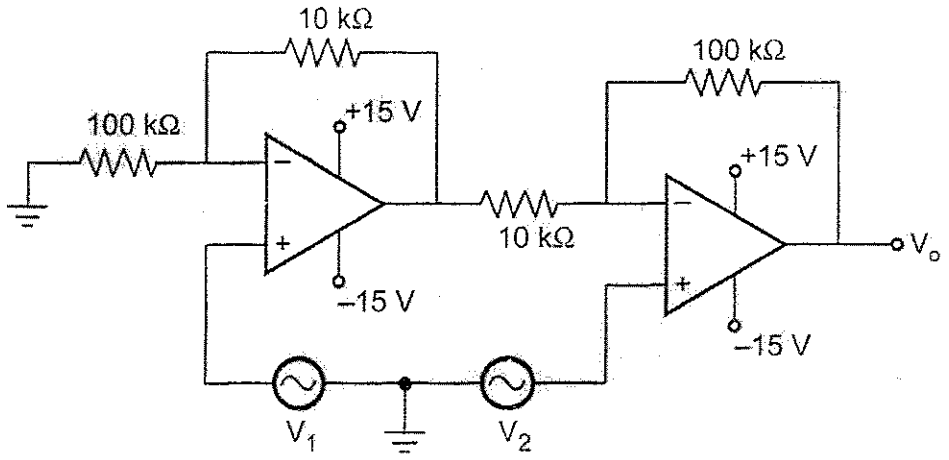


Figure 1

P.T.O

3. What application does the circuit shown in Figure 2 have? Determine the range over which the differential gain can be varied if the potentiometer is varied over its entire range.

(7 marks)

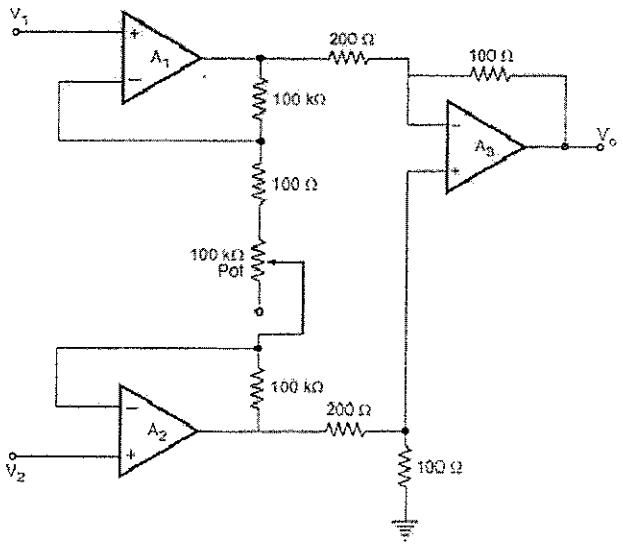


Figure 2

4. The cutoff frequency of a certain second-order Butterworth low-pass filter is 2 KHz. Assume all capacitor values to be 0.01μF. Draw a schematic of the circuit and determine suitable values of all resistors used in the filter design. It is desired to convert this low-pass filter to have a cutoff frequency of 3KHz by using the frequency scaling technique. Which circuit elements would you change and to what value?

(7 marks)

5. Redraw the circuit of Figure 3 to indicate the output sampling, input mixing and the feedback network. Hence determine the feedback topology. Consider $R_1 = 104.26$ KΩ and $R_2 = 1$ KΩ. Calculate the feedback factor β. If $V_s = 100$mV and $V_o = 10$ V, how much is the open loop gain A of the amplifier? Indicate correct units for all quantities calculated.

(3 marks)

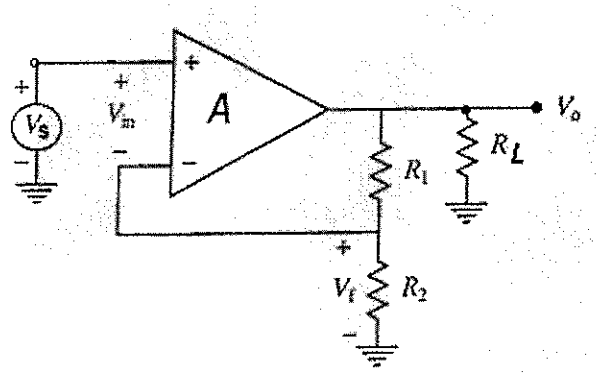


Figure 3

The End

quiz-2

BITS PILANI, DUBAI CAMPUS **(PART-A)**

ECE/INSTR C364 ANALOG ELECTRONICS QUIZ-2(CLOSED BOOK)

WEIGHTAGE: 5% DATE: 20.04.2011 DURATION: 20 MINUTES MAX MARKS: 10 MARKS

Answer all questions

Name: _____ **ID:** _____

1. For the Schmitt trigger circuit shown in Fig.1 calculate the upper and lower threshold voltage levels. Assume V_{sat} = 0.9 Vcc , Vcc = 12 V, and V_{in} = 10Vp-p sinusoid waveform. Also sketch the input and output waveforms. What is the purpose of the 0.8 kΩ resistor. Why the value is chosen as 0.8 kΩ? **[4 Marks]**

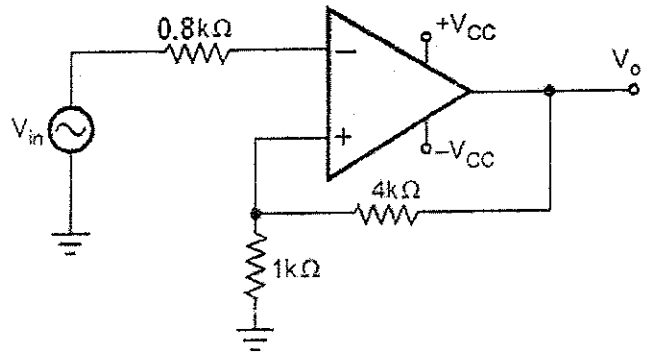


Figure.1

2. Identify the type of circuit in Fig 2 and analyze its output voltage as the input voltage smoothly increases from -5 volts to +5 volts. Assume that both diodes in this circuit are silicon switching diodes, with a nominal forward voltage drop of 0.7 volts. [2 Marks]

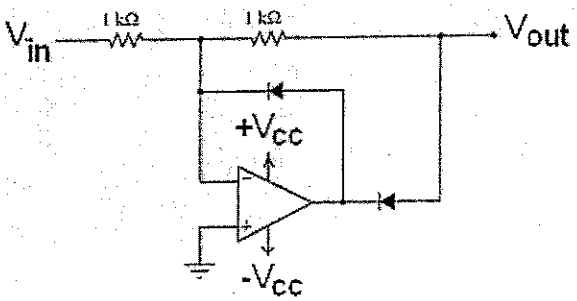


Fig.2

3. If Vi = 5sinωt is applied to the input of a squarer circuit and the output passed through a DC blocking capacitor. Draw the output. Waveform. [2 Marks]

4. Determine the output voltage of this circuit shown in Fig 3 for two different input voltage values: +4 volts, and -4 volts. [2 Marks]

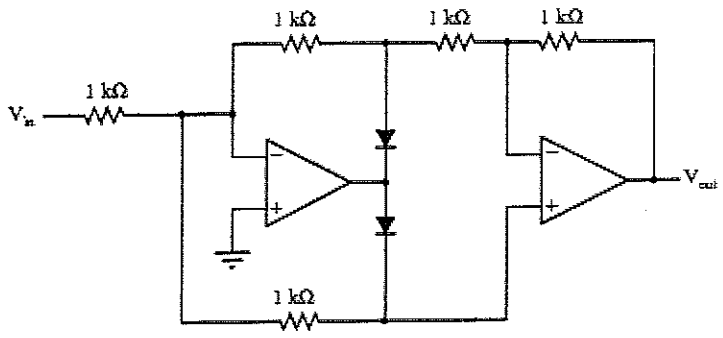


Figure 3

SET A

BITS PILANI, DUBAI CAMPUS

ECE/INSTR C364 ANALOG ELECTRONICS QUIZ-1(CLOSED BOOK)

WEIGHTAGE: 5% DATE: 2.03.2011 DURATION: 20 MINUTES MAX MARKS: 10 MARKS

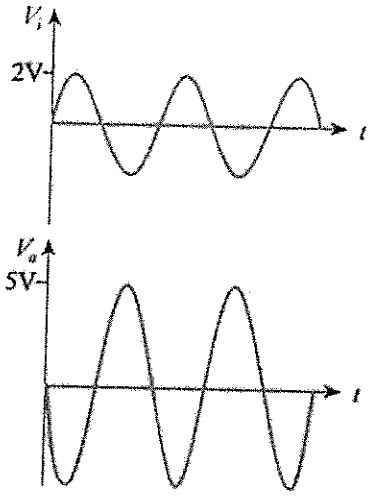
Name: _____ **ID:** _____

This question paper has 9 questions and comprises of 4 pages. Answer all questions

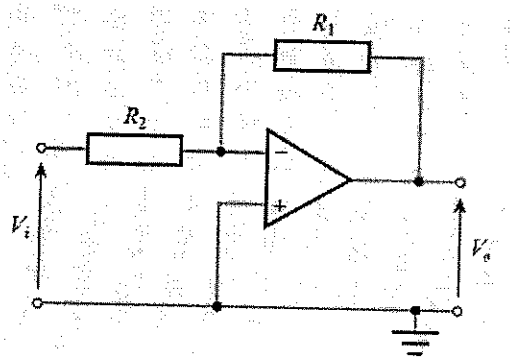
1. Which of the following characteristics would apply to an ideal operational amplifier? **[1M]**

   (A) An infinite voltage gain, an infinite input resistance and zero output resistance
   (B) An infinite voltage gain, an infinite input resistance and an infinite output resistance.
   (C) An infinite voltage gain, zero input resistance and zero output resistance.
   (D) An infinite voltage gain, zero input resistance and an infinite output resistance

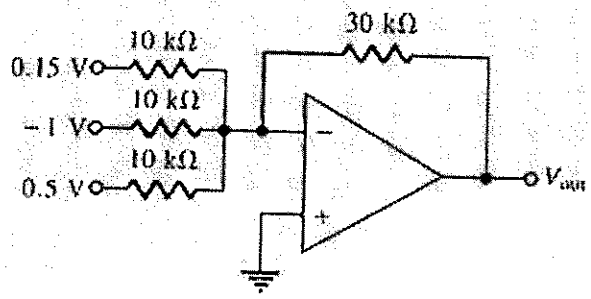
2. The graphs below show the input and output waveforms of an amplifier. Design a suitable closed loop op amp circuit that will provide the necessary output for the given input. **[1M]**



3. In the following circuit, it is required to have a voltage gain of -50 and an input resistance of 1 kΩ. Determine the values of R_1 and R_2. **[1M]**

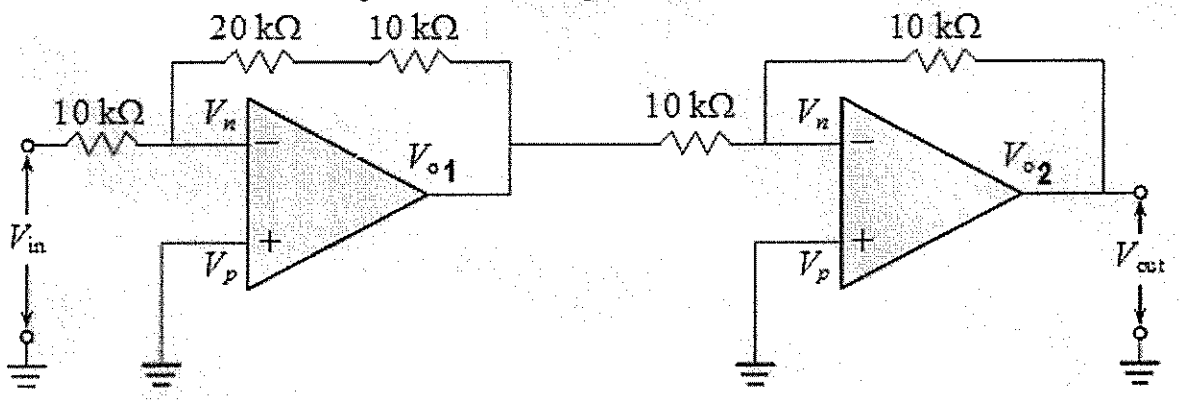


4. Refer to the figure below. Determine the output voltage, V_{OUT}. **[1M]**



5. Design a suitable op amp circuit that would take a DC input voltage V_{in} = 1 V and produce an output voltage V_{out} = 2 V. **[1M]**

6. Consider the following schematic diagram: **[2M]**

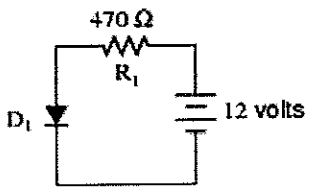


If V_{in} = 1.5 V, what is V_{out} (in volts)?

If V_{in} = 5 V, what is V_{out} (in volts)?

7. When "P" and "N" type semiconductor pieces are brought into close contact, free electrons from the "N" piece will rush over to fill holes in the "P" piece, creating a zone on both sides of the contact region devoid of charge carriers. What is this zone called, and what are its electrical characteristics? Write only key points in your answer. **[1M]**

8. Complete the following table of values for this diode circuit, assuming a typical forward voltage drop of 0.65 volts for the diode: **[1M]**



	R_1	D_1	Total
V			12 V
I			
R	470 Ω		
P			

9. A common emitter npn transistor amplifier has $\beta = 100$. The collector terminal is connected to a 15 V power supply through a resistance $R_c = 5$ K. A dc bias of 1 V is applied to the base terminal and the emitter terminal is connected to ground through an emitter resistor 1 K. The transistor is in the active mode of operation. Assume $V_{BE} = 0.7V$. Determine V_{CE} , I_C , I_B and I_E. **[1M]**