BITS PILANI, DUBAI CAMPUS
International Academic City, Dubai
Second Semester 2010 – 2011
Advanced Computer Organization CS C342 (III year CS)
Comprehensive Examination

Duration: 3 Hrs **Weightage: 40%**
Date: 02.06.2011 **MAX Marks: 80 Marks**
No. of pages: 03

PART A AND PART B SHOULD BE ANSWERED IN SEPARATE ANSWER BOOKLETS

PART A

1. What is the difference between application software and system software? Name each one of the following as one of them.
   a) HD sector boot software
   b) Web browser
   c) Device driver software
   d) Database software **4 Marks**

2. What are the series of abstraction layers present in a typical vision of computer architecture? **4 Marks**

3. Write the shortest sequence of MIPS code for each of the following C code. Assume that the value of a, b, i, j are on registers $s0, $s1, $t0, $t1, respectively. Also, assume that register $s2 holds the base address of the array D.

a)
```
for(i=0; i<10; i++)
  a+=b;
```

b)
```
while (a<10)
{
  D[a] = b+a;
  a+=1;
}
```
3 + 5 = 8 Marks

4. Write the MIPS assembly code to load the 32-bit constant equivalent to decimal 75000 into $s0. **3 Marks**

5. What are the various addressing modes in MIPS. Name the addressing modes used in each of the following instruction
   a) addi b) add c) lw d) beq e) j **3 Marks**

6. Show the IEEE 754 binary representation of the floating-point number **1.375** in single and double precision. Give your results in hexadecimal format. **6 Marks**

7. Multiply $\mathbf{2.25_{ten}}$ and $\mathbf{1.5_{ten}}$, using the floating point multiplication algorithm. Express the resultant product with 5 bits in floating point. Also, convert the answer to decimal and check the results. **6 Marks**

8. The various types of instructions, their respective frequencies and CPI executed on a certain machine are given in the table below.

Instruction type	*Frequency*	*CPI*
ALU	50%	1
Load	20%	5
Store	10%	3
Branch	20%	2

Answer the following

a) How much faster would the machine be if a better data cache reduced the average load time to 2 cycles?

b) How much faster would the machine be if two ALU instructions are executed at once?

3 x 2 = 6 Marks

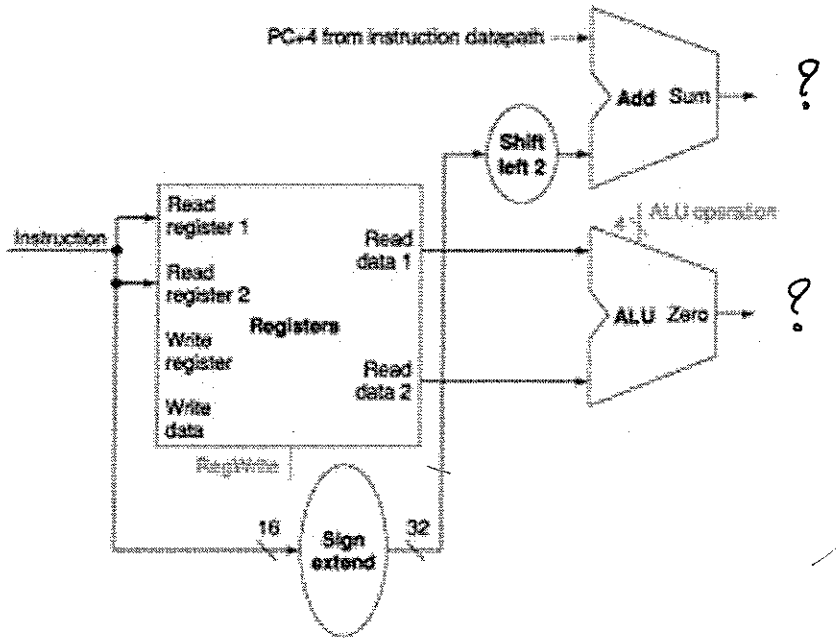
PART B

9. What are the key differences of the arithmetic-logic instructions and the memory instructions data path operations? **5 Marks**

10. What you mean by pipeline hazards? Mention and explain in two lines the different types of pipeline hazards? **5 Marks**

11. What do you mean by division of instructions into n stages? How stages are there in a pipeline data path and how instruction can be executed during a single clock cycle? **5 Marks**

12. What is the function of the data path diagram shown below? Give short descriptions of it and also what will be output signal of the Add Sum and ALU Zero? **7 Marks**



13. Give the traditional single-clock-cycle pipeline diagram for the following instructions:

6 Marks

lw \$10, 100(\$0)
lw \$13, 200(\$0)
lw \$14, 300(\$0)

14. What do you mean by Principles of locality? What are the different types of locality available?

4 Marks

15. Assume an instruction cache miss rate for a program is 2% and a data cache miss rate is 4%. If a processor has CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Use the attached instruction frequencies for SPECint 2000 chart for the above problem calculation.

8 Marks

Core MIPS	Name	Integer	Fl. pt.	Arithmetic core + MIPS-32	Name	Integer	Fl. pt.
add	add	0%	0%	FP add double	add.d	0%	8%
add immediate	addi	0%	0%	FP subtract double	sub.d	0%	3%
add unsigned	addu	7%	21%	FP multiply double	mul.d	0%	8%
add immediate unsigned	addiu	12%	2%	FP divide double	div.d	0%	0%
subtract unsigned	subu	3%	2%	load word to FP double	l.d	0%	15%
and	and	1%	0%	store word to FP double	s.d	0%	7%
and immediate	andi	3%	0%	shift right arithmetic	sra	1%	0%
or	or	7%	2%	load half	lhu	1%	0%
or immediate	ori	2%	0%	branch less than zero	bltz	1%	0%
nor	nor	3%	1%	branch greater or equal zero	bgez	1%	0%
shift left logical	sll	1%	1%	branch less or equal zero	blez	0%	1%
shift right logical	srl	0%	0%	multiply	mul	0%	1%
load upper immediate	lui	2%	5%				
load word	lw	24%	15%				
store word	sw	9%	2%				
load byte	lbu	1%	0%				
store byte	sb	1%	0%				
branch on equal (zero)	beq	6%	2%				
branch on not equal (zero)	bne	5%	1%				
jump and link	jal	1%	0%				
jump register	jr	1%	0%				
set less than	slt	2%	0%				
set less than immediate	slti	1%	0%				
set less than unsigned	sltu	1%	0%				
set less than imm. uns.	sltiu	1%	0%				

FIGURE 3.26 The frequency of the MIPS instructions for SPEC2000 integer and floating point. All instructions that accounted for at least 1% of the instructions are included in the table. Pseudoinstructions are converted into MIPS-32 before execution, and hence do not appear here. This data is from Chapter 2 of *Computer Architecture: A Quantitative Approach*, third edition.

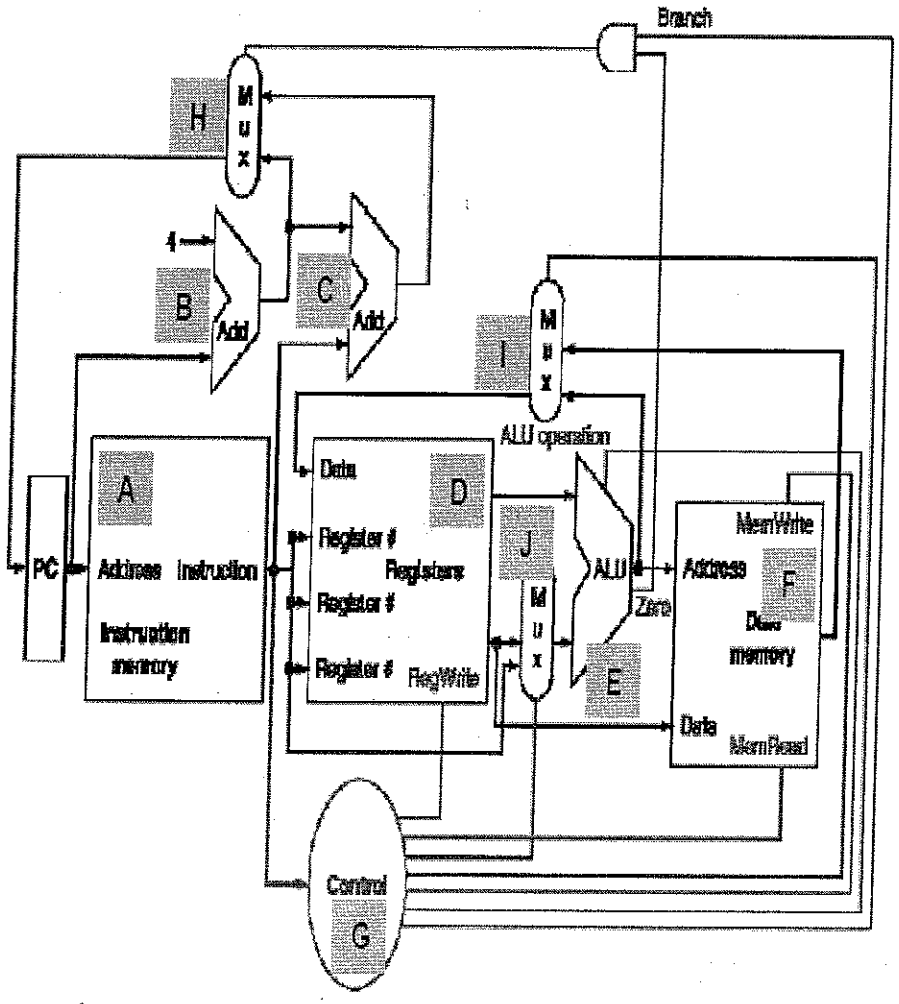
**********BEST OF LUCK**********

BITS PILANI, DUBAI CAMPUS
International Academic City, Dubai
Second Semester 2010 – 2011
Advanced Computer Organization CS C342 (III year CS)
Test – 2 (Open Book)

Duration: 50 minutes **Weightage: 20%**
Date: 17.04.2011 **MAX Marks: 40 Marks**
No. of pages: 03

ANSWER ALL QUESTIONS

1. For questions (a), (b) and (c), consider the following simplified MIPS datapath **3 x 5 = 15 M**



The datapath supports the following instructions: add, sub, and, or, slt, beq, lw and sw.

a) Referring to the labels **A** through **J** in the datapath diagram above, which components are required during the execution of a **lw** instruction? (Ignore the PC for this question.)
b) What is the critical path for the lw instruction? Mention them in terms of the labels as per the above diagram.
c) Referring to the labels **A** through **J** in the datapath diagram above, which components are required during the execution of a beq instruction? And also mention what are the components not required for this instruction?

2. What do mean by state elements and combinational elements? List two components for state and combinational elements. Which element in the data path diagram is called data selector? **5 M**

3.
   a. Write the format, description and the sequence of steps involved in the execution of the **jal** instruction. **3 M**
   b. Draw the single cycle data path of the **jal** instruction. Add necessary data paths and control signals to the single cycle data path of MIPS and justify the need for the modifications, if any. **7M**

4. For each of the **pipelined code sequence** given in (a) and (b) below identify whether a data dependence exists or not. If there exists a data dependence which leads to a data hazard mention the type of action required to overcome it. **2 x 2 = 4 M**

   a)
   ```
   lw  R1, 45(R2)
   add R5, R1, R7
   sub R8, R6, R7
   or  R9, R6, R7
   ```

   b)
   ```
   lw  R1, 45(R2)
   add R5, R6, R7
   sub R8, R6, R7
   or  R9, R1, R7
   ```

c) Consider the following MIPS assembly code:

```
add $s3, $s2, $s3
lw $s4, 100($s3)
sub $s7, $s6, $s2
xor $s6, $s4, $s3
```

Assume there is no forwarding or stalling circuitry in a pipelined processor that uses the standard 5-stages (IF, ID, EX, Mem, WB). Instead, we will require the compiler to add no-ops (no –operations) to the code to ensure correct execution. (Assume that if the processor reads and writes to the same register in a given cycle, the value read out will be the new value that is written in.) Rewrite the code to include the no- ops (no – operations) that are needed. Do not change the order of the four statements. Use as few no- ops as possible. **6 M**

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BITS PILANI, DUBAI CAMPUS
International Academic City, Dubai
Second Semester 2010 – 2011
Advanced Computer Organization CS C342 (III year CS)
Test – 1 (Closed Book)

Duration: 50 minutes **Weightage: 25%**
Date: 27.02.2011 **MAX Marks: 50 Marks**
No. of pages: 2

PART – A

1. Mention any two hardware/software components that affect the program performance. 2 M

2. Assume $s0 has the binary number
   1111 1111 1111 1111 1111 1111 1111 1111

   $s1 has the binary number
   0000 0000 0000 0000 0000 0000 0000 0001

   What are the contents of the registers $t0 and $t1 after the following instructions?

   slt $t0, $s1, $s0
   sltu $t1, $s1, $s0 3 M

3. Convert 16 bit versions of 11_{ten} and -11_{ten} to 32 bit binary numbers. 5 M

4. With a neat table illustrate the overflow conditions for addition and subtraction. 5 M

5. Write whether overflow occurs or not in each of the following 4 – bit signed arithmetic. 2 x 5 = 10M

   a) -2 + 3 b) -5 + 3 c) -4 – 3 d) -7 – 3 e) 6 + 3

PART – B

1. Convert the following into MIPS instructions and give its meaning.
   a) $s1 = ~ ($s2 | $s3) 6 M
   b) If (a<b) small=a else small = b; assume suitable registers for the variables.
   c) go to 10000

2. Write the MIPS instruction for "compare less than constant for natural numbers". 3 M

3. Write the C code segment for the following: 5 M

```
Sum: slti  $a0, 1
       beq $a0, $zero, sum_end
       add  $a1,  $a1, $a0
       addi $a0, $a0, -1
        j  Sum
 sum_end :
          add $v0, $a1, $zero
           jr  $ra
```

4. Give the 32 bit instruction format for the I-type MIPS instruction. 3 M
5. What do you mean by PC-relative addressing? Explain it with a flow diagram. 4 M
6. What are the different types of registers available, mention them with their use. 4 M

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BITS PILANI, DUBAI CAMPUS
International Academic City, Dubai
Second Semester 2010 – 2011
Advanced Computer Organization CS C342 (III year CS)
Quiz 2 (Closed Book)

Duration : 20 minutes **Weightage : 7%**
03.05.2011 **MAX : 14 Marks**
No. of pages : 02

VERSION A

ID No: **Name :**
Sec:

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1. What are the control lines used in each of the following stages in a pipelined control and data path of MIPS?
   a) Ex/ Address Calculation stage
   b) Memory access stage
   c) WB stage. (3 Marks)

2. Complete the following table with the control lines used in each stage of the pipelined data path for each of the instruction types R-format, lw, sw and beq. Mention all control lines used in each stage and mark them as set(1), reset (0) or don't care(x) depending on the instruction type .

Instruction type	*Ex/address calculation stage*	*Mem access stage*	*WB stage*
R format			
lw			
sw			
beq			

(4 Marks)

3. A 4-kilobyte cache with a line size of 32 bytes direct mapped on virtual addresses. Thus each load/store to cache moves 32 bytes. If one variable of type float takes 4 bytes on our system, what will be the number variables each cache line will hold?

(3 Marks)

4. Consider a cache with 64 blocks and a block size of 16 bytes, what block number does bytes address 1200 map to?

(2 Marks)

5. Give the formula to find the total number of bits in a direct-mapped cache? (2 marks)

Ans

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BITS PILANI, DUBAI CAMPUS
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Second Semester 2010 – 2011
Advanced Computer Organization CS C342 (III year CS)
Quiz 1 (Closed Book)

Duration : 20 minutes **Weightage : 8%**
23.03.2011 **MAX : 16 Marks**
No. of pages : 04

VERSION A

ID No: **Name :**
Sec:

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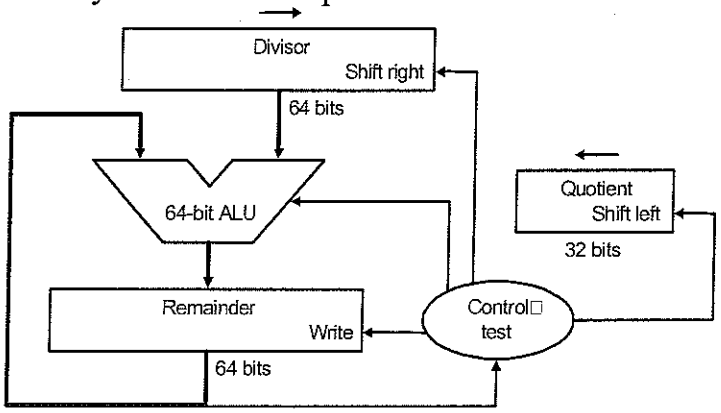
1. Give improved version of the following hardware block diagram and mention why it is called improved version? 3 M



Ans:

2. Give the floating point number for the following inputs:
   Let S=0, E=3, significand = 01000101 3M
   Ans:

3. Instruction execution rate of a machine is defined as number of instructions executed per second. Write an equation to express CPI of a machine in terms of its instruction execution rate.

   Ans:

   CPI =

   2 M

4. A program P1 is run on two machines M1, M2 and the following measurements were made:

Program	**Time on M1**	**Time on M2**
P1	10 secs	5 secs

Program	**Instructions executed on M1**	**Instructions executed on M2**
P1	200×10^6	160×10^6

If the clock rates of the machines M1 and M2 are 200MHz and 160 MHz respectively, answer the following 4 x 1 = 4 M

a) What is the instruction execution rate of M1 ?
Ans:

b) What is the instruction execution rate of M2?
Ans:

c) What is the CPI of M1 in terms of its instruction execution rate?
Ans:

d) What is the CPI of M2 in terms of its instruction execution rate?
Ans:

5. Find the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200MHz. 2 M

Instruction Category	**Percentage of occurrence**	**No. of cycles per instruction**
ALU	38	1
Load and Store	15	3
Branch	42	4
Others	5	5

Ans:

6. What is the MIPS rating of the machine A, which is described in the **previous question number 5.** 2 M

Ans:

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