BITS – PILANI DUBAI

Dubai International Academic City, Dubai

II semester III Year 2009-2010

Digital Electronics & Computer Organisation / EEE C 391

Comprehensive examination

23 – 05 – 10 **Time : 3Hrs.** Max. Marks : 80 **Weightage : 40 %**

(Answer all questions. All parts of a question have to be answered together and continuously)

1.a) Add the following signed 2's complement binary numbers and verify the answers in decimal.

(i) 011 + 1101 (ii) 0101 + 1110

b) Represent the following Gray code in its equivalent Binary code 100101

c) Clearly define the Noise margin and Propagation delay of a digital IC which characterize the logic family. (4 + 2 + 3)

2.a) Consider the Boolean function $F = \overline{X}Y + X\overline{Y}$. Draw the logic circuit using AND, OR and NOT gates. At time t = 0, all the variables are set to zero. At t = 20 msec, X toggles and again toggles at t = 45 msec. Y toggles at t = 30 msec, and again toggles at t = 55 msec. Sketch the timing diagram for the logic circuit inputs and the circuit output (Note : Toggle means that the variable switches to other value)

b) For the logic circuit described in the above question, write the verilog HDL codes for the circuit description and a stimulus for the inputs. (5 + 5)

3.a) What is a full adder? Write the truth table of a full adder. Draw the block diagram level representation of a full adder circuit **using two half adders and basic logic gates**.

b) Design and explain **a 10's complimenter circuit** of a BCD number (circuit takes BCD as input and gives ten's complimented output in binary) using four bit binary adder and external logic gates (Use Block diagram representation of four bit binary adder eg: 7483). (5 + 5)

4.a) Design a decimal to BCD encoder using only four OR gates. Switches S0 to S9 indicate the 9 decimal numbers at the input, when an operator closes a switch the circuit will produce a BCD number at the output which is the binary equivalent of the decimal number pressed. Draw the logic circuit.

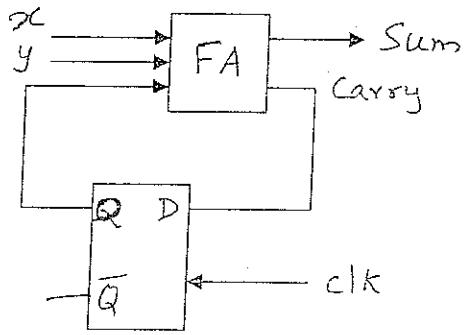
b) List the PLA programming table for the BCD to excess-3 code converter. Optimize the no. of product terms for true outputs. (4 + 6)

5.a) Draw and explain the **logic diagram** of a multiplier to explain the working of the 3bit x 2 bit word multiplication. Show the working of the circuit using the data 7 x 3

b) Explain clearly the Booth's algorithm of computer multiplication using the data -13 x 3. Give comments on each steps and verify your answer (5 + 5)

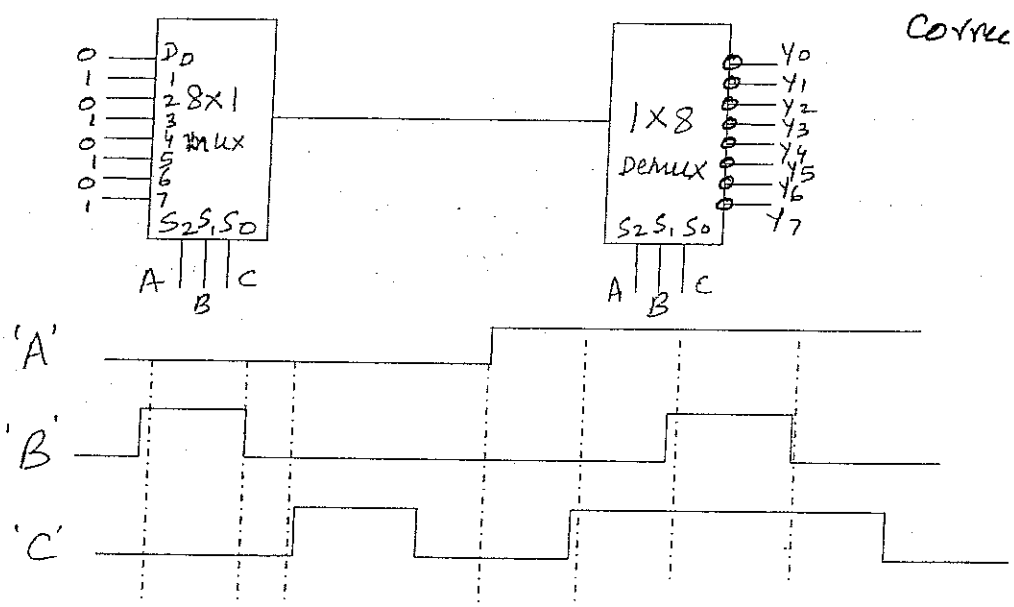
6.a) Draw a four bit MOD – 16 binary ripple up counter using JK flip flops, explain its working. Show the timing diagram of this counter. Assume the flip flops are initially in state 0.

6. b) A sequential circuit has one D flip flop and two inputs x and y and one output S. The circuit consists of a full adder connected to the D flip flop as shown in the figure. Derive the state table and state diagram of the sequential circuit.
Assuming the initial state of D flip-flop as zero, what will be the output sequence if the following input sequences are applied to the circuit . x = 01101 and y = 11101



(5 + 6)

7.a) A combinational circuit using an 8 x 1 multiplexer is given in figure below. Sketch the outputs Y0 – Y7 for the given conditions of A,B,C. (Note: output of the Demultiplexer is 1 when not selected



b) Design a four bit universal shift register using D flip flops and multiplexers which will perform the following operations based on the function table given below. (6+4)

No.	S_1 S_0	Function
1	0 0	Clear the register
2	0 1	Shift right
3	1 0	Shift left
4	1 1	Load new data

8.a) With a neat circuit diagram, explain the operation of an inverter circuit using Schotky transistors. What are the advantages of schotky gates over other TTL logic gates?

b) Write short notes on commonly used bus arbitration schemes . (5 + 5)

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BITS, PILANI – DUBAI

International Academic City, Dubai

Year III – Semester II 2009– 2010

Course No.: EEE C 391 **Course Title: DECO**

TEST – II (Open Book)

Date: April 18, 2010 **Time: 50 Minutes** **Max. Marks = 25**

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1. Design a PROM programming table which will implement the function $F(x) = 5x^2 + 2$, where x is a three bit binary number. What would be the minimum size of the ROM required for implementing this function? (5)

2. A sequential circuit has two JK flip flops A and B and one input x. The circuit is described by the following input equations.
   $J_A = A' + x$; $K_A = B'$; $J_B = Bx'$; $K_B = A$
   i) draw the sequential circuit
   ii) Derive the state equations $A(t + 1)$ and $B(t+ 1)$
   iii) Write the state table of the circuit
   iv) Draw the state diagram of the circuit (8)

3. Design a four-bit shift register with a parallel load, using D flip-flops. There are two control inputs : shift and load. When shift is '1' the contents of the register are shifted right by one position. New data are loaded into the register when load is '1' and shift is '0'. If both control inputs are equal to '0', the content of the register do not change. Draw the logic diagram of the shift register. (6)

4. Draw the flow chart to represent the division algorithm using NON-RESTORATION method for unsigned integer numbers. Illustrate the steps with the sample data 1110÷0100 (6)

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BITS – PILANI DUBAI

Dubai International Academic City

II semester III Year 2009-2010

Digital Electronics & Computer Organisation

EEE C 391

Test -1 **(Closed Book)**

07 – 03 – 10 **Time : 50min.** Max. Marks : 25 **Weightage : 12.5 %**

(Answer all questions. **Calculators are not allowed. Assume positive logic**)

1. Implement a NOT, a two-input AND and a two-input OR logic gate using only two-input NORs and hence show that the NOR is an Universal logic gate (1+2+1)

2. Draw a logic diagram which represents the function F(A,B,C,D) = (A'B + AD')'C. Assume only true inputs are available. Redraw the circuit using NAND gates alone. Represent the function as product of max terms (2+2+2)

3. Its desired to design a combinational logic circuit that will cause a light to go ***ON*** each time the decimal equivalent of 4-bit binary input is divisible by 3. It is known that the numbers 0,1,7, 11 and 14 will never occur as inputs. Map the function and simplify using K-Map. (3+2)

4. Explain the construction of a 4 x 1 Mux with three-state buffers and a 2 – 4 decoder. Also show how this circuit can be used as a Half adder. (2+3)

5. How many 32 x 8 RAM chips are needed to provide a memory capacity of 256 bytes? How many address lines will be needed to address this memory bank? Show the decoding of address lines to generate the chip select signals of the memory units using a decoder. (1+1+3)

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Name : Id no :

BITS, PILANI – DUBAI

SET A

International Academic City, Dubai

Year III – Semester I 2009– 2010

Course No.: **EEE C 391** Quiz II Course Title: **DECO**

Date: May 10, 2010 Time: 20 Minutes Max. Marks = 10

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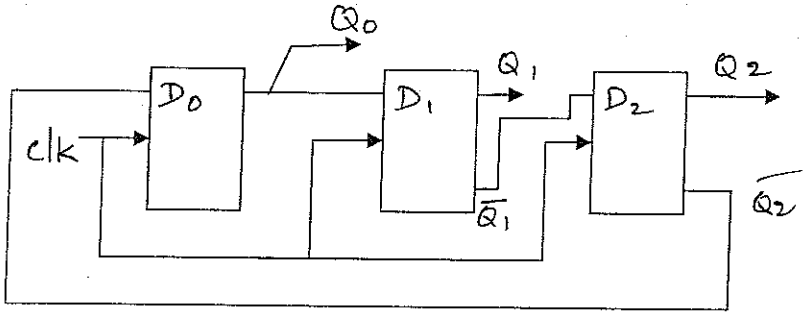
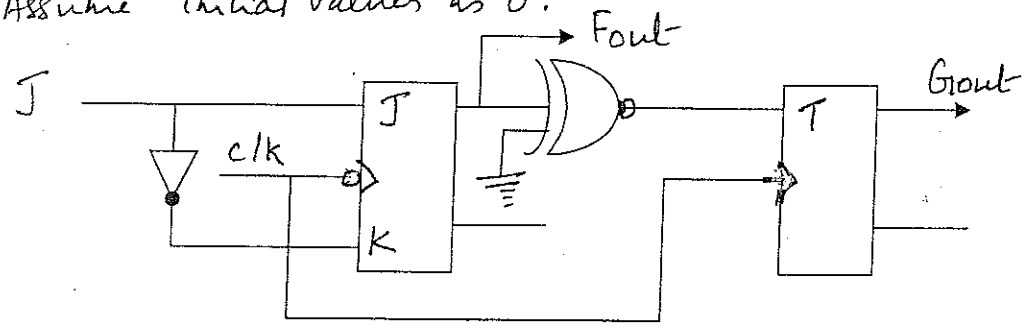
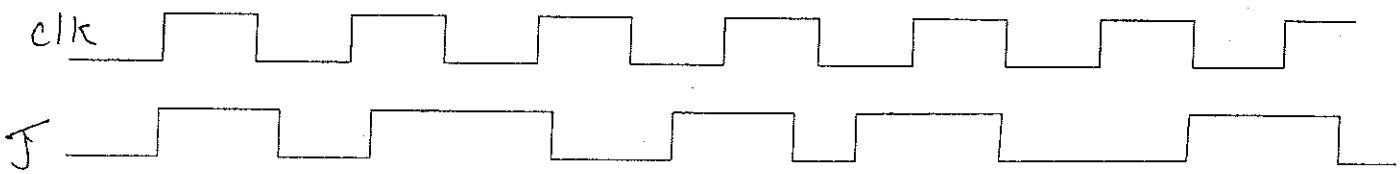
1. Tabulate the out puts Q_0 Q_1 Q_2 of the shift register shown below for six clock pulses assuming the initial state was 000.



2. Given below is a sequential circuit. Draw the out put waveforms for both the flip flops F_{out} and G_{out} for the input waveform shown in the figure with respect to the clock signal.

Assume initial values as '0'.





3. Given the following state table of a Mealy model sequential circuit with one input **x**, one output **z** and four states **A,B,C & D**, draw the state diagram

S(t)	S(t+1),z	
	x = 0	x = 1
A	B,0	A,1
B	B,1	C,0
C	D,0	A,0
D	B,0	C,1

4. What will be the output sequence if the following input sequence (01101001011) is applied to the circuit in question. No.3 starting from the state 'A'.

Name :

Id NO :

BITS, PILANI – DUBAI

SET B

International Academic City, Dubai

Year III – Semester I 2009– 2010

Course No.: **EEE C 391** Quiz II Course Title: **DECO**

Date: May 10, 2010 Time: 20 Minutes Max. Marks = 10

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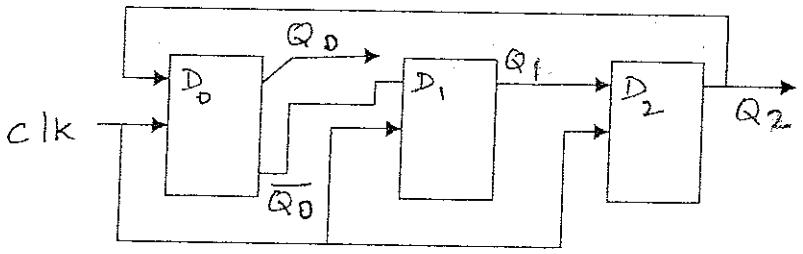
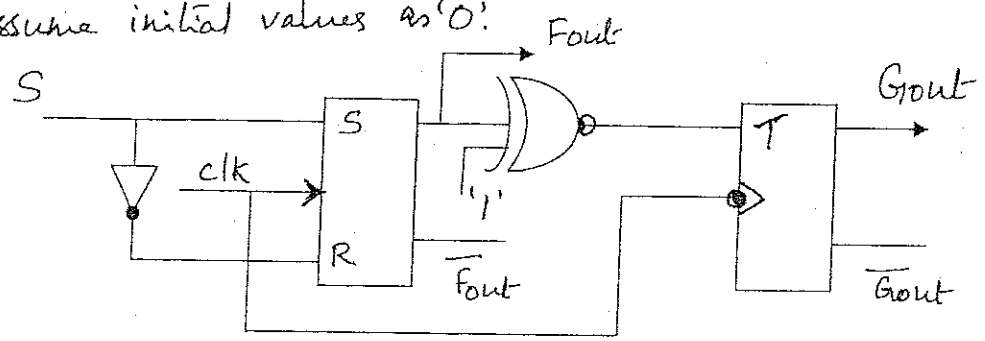
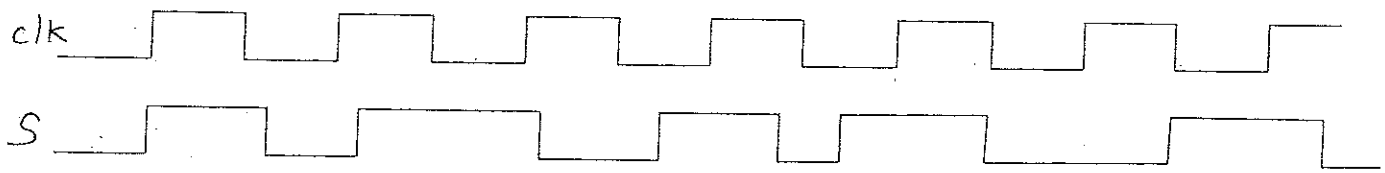
1. Tabulate the out puts Q_0 Q_1 Q_2 of the shift register shown below for six clock pulses assuming the initial state was 000.



2. Given below is a sequential circuit. Draw the out put waveforms for both the flip flops F_{out} and G_{out} for the input waveform shown in the figure with respect to the clock signal.

Assume initial values as '0'.





3. Given the following state table of a Mealy model sequential circuit with one input **x**, one output **z** and four states **A, B, C & D**, draw the state diagram

S(t)	S(t+1),z	
	x = 0	x = 1
A	B,1	A,0
B	A,0	D,0
C	D,0	A,1
D	C,1	B,1

4. What will be the output sequence if the following input sequence (**01101001011**) is applied to the circuit in question. No.3 starting from the state '**A**'.

BITS, PILANI – DUBAI

International Academic City, Dubai
Year III – Semester II 2009 – 2010
Quiz I (Closed Book)

SET A

Course No.: **EEE C 391** Course Title: **DECO**

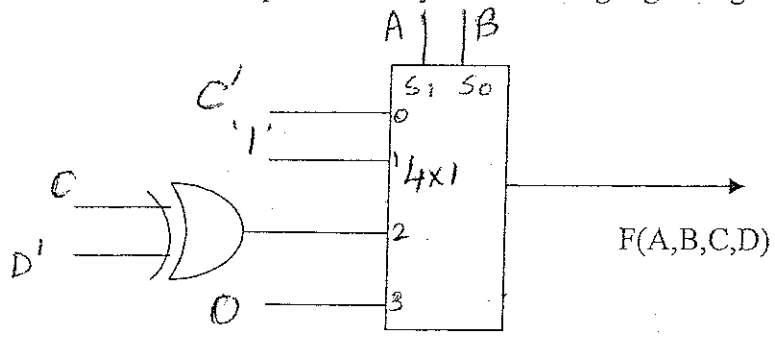
Date: March 29, 2010 Time: 20minutes. Max. Marks = 10

(Calculators not allowed)

1. Convert the following (1·5 + 1 + 1)

   $(1BCD)_H$ = (----------) $_{10}$ = (----------)$_8$ = (----------)$_2$

2. Find the function implemented by the following logic diagram. (2M)



3. Implement the Boolean function $S(x,y,z) = x'z + yz'$ using a 3 x 8 active low decoder and external two input AND gates. (2 M)

4. Match the following according to the functions. (0·5 × 5 = 2·5 M)

i) PROM	a) 2^n inputs one output , n select lines
ii) DECODER	b) Programmable AND arrays fixed OR arrays
iii) DEMULTIPLEXER	c) n inputs and 2^n outputs
iv) PLA	d) Fixed AND arrays Programmable OR arrays
v) PAL	e) one input, 2^n outputs and n select lines
	f) Programmable AND arrays and OR arrays

********** GOOD LUCK **********

Answers:

BITS, PILANI – DUBAI

International Academic City, Dubai
Year III – Semester II 2009 – 2010
Quiz I (Closed Book)

SET B

Course No.: **EEE C 391** Course Title: **DECO**

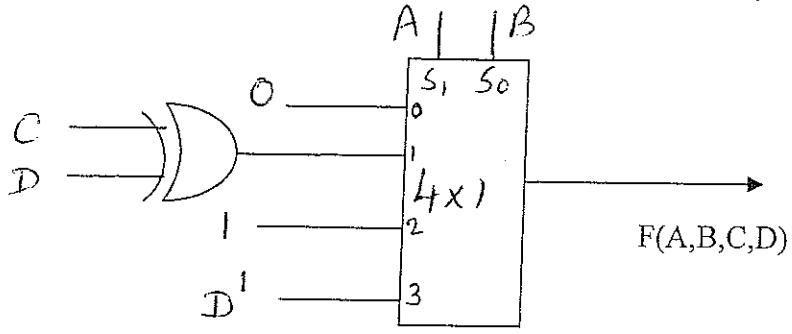
Date: March 29, 2010 Time: 20minutes. Max. Marks = 10

(calculators not allowed)

1. Convert the following (1·5 + 1 + 1)

   $(1B.0D)_H$ = (----------) $_{10}$ = (----------)$_8$ = (----------)$_2$

2. Find the function implemented by the following logic diagram. (2 M)



3. Implement the Boolean function S(x,y,z) = x'z' + y'z using a 3 x 8 active low decoder and external two input AND gates. (2 M)

4. Match the following according to the functions. (0·5 × 5 = 2·5 M)

i) PAL	a) 2^n inputs one output , n select lines
ii)DEMULTIPLEXER	b) Programmable AND arrays fixed OR arrays
iii) DECODER	c) n inputs and 2^n outputs
iv) PLA	d) Fixed AND arrays Programmable OR arrays
v) PROM	e) one input, 2^n outputs and n select lines
	f) Programmable AND arrays and OR arrays

********** GOOD LUCK **********

Answers :