BITS PILANI – DUBAI
International Academic City, Dubai
Second Semester 2008 – 2009
Advanced Computer Organization CS C 342 (III year CS)
Comprehensive Examination (Closed Book)

Duration : 3 hours **Weightage : 40%**
25.05.09 **MAX : 40 marks**

Question Paper contains 9 questions.

1. a. What are the hardware and software components that affects performance ? (1 mark)
   b. What are the addressing modes possible on the MIPS for loads / stores? (1 mark)

2. a. Decode the following MIPS machine code and give its instruction format in assembly language. (1 mark)
   00af8022hex
   b. What hexadecimal number does this binary number represent:
   10111010110100001100101011111110 (1 mark)
   c. Assume variable h is associated with register $s2 and variable g is associated with register $s4 and the base address of the array BLOCK is in $s3. What is the MIPS assembly code for the C assignment statement below?
   BLOCK[40] = g – h + BLOCK[20]
   Use only two temporary registers t0 and t1. (2 marks)
   d. If $3 = 20 , $4 = 35, what will be the contents of $5 after the following code is executed. (1 mark)
   addi $6, $3, 15
   slt $5, $6, $4

3. a. What is -31 in 8 bit two's complement form? (1 mark)
   b. Write 23.3125 in single precision floating point representation. Give the answer in hexadecimal. (1 mark)
   c. Use 4-bit numbers to multiply 0101 and 1001. (3 marks)
   d. Add 3.25 x 10 ** 3 and 2.63 x 10 ** -1 (2 marks)

4.a Calculate the % of elapsed time in Unix time command. (1 mark)
   65.2u 16.5s 3:57 _____%
   b. If Computer A runs a program in 25 seconds and computer B in 40 seconds, then Which computer is faster by how many times? (1 mark)
   c. Define workload. (1 mark)

5.a. How many select lines does 32:1 MUX has? (1 mark)

b. What is the term used to define the process of increasing the number of bits used to represent a number by replicating the MSB to the left? (1 mark)

c. Why instruction memory need only provide read access? (1 mark)

d. What are the units needed to implement loads and stores ? (1 mark)

6. a. Consider the following code segment

```
    lw r1, 0(r4)
    lw r2, 0(r5)
    add r3,r1, r2
    bnz r3,1
    lw r4, 100(r6)
    lw r5, 200(r6)
    sub r3,r4,r5
1:  sw r3,50(r1)
```

Rewrite the code (without changing the meaning of the program) as to minimize data hazards as far as possible. Assume that no other general purpose registers other than those used in the code, are available. (2 marks)

b. Assume that the individual stages of a MIPS datapath implementation have the following latencies (ps represents picoseconds);

Instruction Fetch	Instruction Decode	Execute (ALU)	Memory Access	Register Write Back
200ps	120ps	190ps	400ps	100ps

What is the clock cycle time in a pipelined and non-pipelined implementation version of this MIPS processor? (2 marks)

c. What is the total latency of the lw instruction in a pipelined processor? (Use the data given in b) (1 mark)

7.a. Consider the following piece of code

```
for(i=0;i<100000;i++)
    Data[i]++;
```

What kind of locality is exhibited by access to "Data" ? (1 mark)

b. Consider a 4-way set associative cache with a total size of 64KB. The block size is 32 bytes and the addresses are 32-bit long. Then how the 32-bit address is divided into the tag, index and block offset? (1 mark)

c. Least Recently Used Replacement Policy. Consider a tiny fully associative cache that can hold 4 blocks and is initially empty. A program accesses 8 blocks: b0, b1, ..., b7 during its execution in the following sequence:
b0, b1, b2, b3, b4, b5, b2, b3, b2, b4, b2, b7, b2, b3, b2, b3, b6, b3, b6, b3
Calculate the hit ratio. (2 marks)

d. Match the memory hierarchy element on the left with the closest phrase on the right: (1 mark)

1. L1 cache	a. A cache for a cache
2. L2 cache	b. A cache for disks
3. Main memory	c. A cache for a main memory
4. TLB	d. A cache for page table entries

8.a. If a disk spins at 7200RPM, what is its rotational latency ? (1 mark)
b. What is the average time to read or write a 512-byte sector for a typical disk rotating at 12,000 RPM? The advertised average seek time is 7ms, the transfer time is 6ms and the controller overhead is 0.4 ms. Assume that the disk is idle so that there is no waiting time. (1 mark)
c. Expand RAID. (1 mark)
d. What is Cache Flushing? (1 mark)
e. What is polling? (1 mark)

9.a. Explain the different types of snooping protocols . Give an example of a Cache Coherency Protocol with diagram. (3 marks)
b. What is false sharing? (1 mark)

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Second Semester 2008 – 2009
Advanced Computer Organization CS C 342 (III year CS)
Test – 2 (Open Book)

Duration : 50 minutes **Weightage : 20%**
26.04.09 **MAX : 20 Marks**

Question Paper contains 5 questions.
Note : Only Prescribed Text Book and Handwritten class notes are allowed.

1. If page access pattern is 0,1,2,3,0,1,2,4,0,1,2,3,0,1,2,4
   a. Find the hit ratio. (1 mark)
   b. Assume that the first four pages are filled up. Illustrate with diagram each step. (2 marks)
   c. Specify whether each access is hit or miss. (2 marks)
   d. Find the total number of misses. (1 mark)

2. The logical address space in a computer system consists of 128 segments of capacity 32 pages of 4K words. The physical memory consists of 4K page frames, each of 4K word capacity. Formulate the logical and physical address format. (4 marks)

3. Memory subsystem designers of a computer system decided to employ two levels of cache memory: L1 and L2. For the purpose of simulation study the hit time and miss penalty are expressed in terms of number of CPU clock cycles. Simulation study with two options – (I) direct mapped, and (II) two way set associatively mapped L2 cache - resulted in following figures:
   a. Out of 1000 memory references no. of misses in L1 : 80
   b. For option I, no. of misses in L2 : 20
   c. For option II, no. of misses in L2 : 12
   d. For option I, hit time on L2 : 4 cycles
   e. For option II, hit time on L2 increases by : 20% of clock
   f. Miss penalty for L2 : 40 clock cycles.

   Compare the average memory access time for either of the two options. (5 marks)
   Note:
   - Average memory access time = Hit time L1 + Miss rate L1 * Miss penalty L1
   - Miss penalty L1 = Hit time L2 + Miss rate L2 * Miss penalty L2
   - L2 cache is always synchronized with L1 cache and CPU
   - L1 has same cycle time as that of CPU and usually direct mapped.

4. Draw the timing diagram for asynchronous data transfer for write operation. (2 marks)

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5. Consider executing the following code on the pipelined datapath of MIPS.

```
sub $12,$2,$5
or  $13,$6,$2
and $14,$2,$2
lw $6,200($3)
add $7,$3,$6
sub $4,$2,$5
```

a. Identify all of the data dependencies in the above code. (1 mark)

b. Identify the registers involved in hazards. (1 mark)

c. Identify the techniques used to resolve the hazards. (1 mark)

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Second Semester 2008 – 2009
Advanced Computer Organization CS C 342 (III year CS)
Test – 1 (Closed Book)

Duration : 50 minutes **Weightage : 25%**
15.03.09 **MAX : 25 Marks**

1. Define Abstraction. (1 mark)
2. Calculate the % of elapsed time in Unix time command
   65.2u 13.5s 4:28 _____ % (1 mark)
3. Consider the assignment statement
   a = (b+c) + (d-e) – (f+g);
   variables a,b,c,d,e,f,g are assigned to the registers $s0,$s1,$s2,$s3,$s4,$s5 and $s6 respectively. What is the compiled MIPS code. Use minimum temporary registers. (2 marks)
4. Assume variable x is associated with register $s4 and the base address of the array LIST is in $s5. What is the MIPS assembly code for the C assignment statement below? LIST[24] = x + LIST[16];
   What is the MIPS machine language code for these instructions? Represent your answer in decimal. (2 marks)
5. What is the assembly language statement corresponding to the machine instruction 00B04812. (2 marks) 00B04822
6. What is the decimal representation of the instruction srl $s1,$a2,15. (1 mark)
7. For the MIPS assembler code

```
Loop : srl  $a1,$t2,5
       sub  $s1,$s2,$s3
       lw   $t0,48($1)  $s1
       beq  $t0,$s6,Again
       addi $s3,$t5,12
       andi $s1,$s2,400
       j  Loop
Again:
```

   Assume, loop starts at location 64000 in memory. What is the MIPS machine code for this loop? (3 marks)
8. What is the meaning of the instruction j 2500? (1 mark)
9. Multiply 7 * 2 in binary. Show all the steps in detail. (4 marks)
10. If CPI = 7 and there are 15 clock cycles, find the total number of instruction in that program. (1 mark) 14
11. Computer P has a clock cycle time of 800ns and a CPI of 4.6 for some program and computer Q has a clock cycle time of 1120ns and a CPI of 3.6 for the same program. Which computer is faster and by how much. (2 marks)
12. What are the basic components of performance and how each is measured? (2 marks)
13. Show the IEEE 754 binary representation of the number -0.5_{ten} in single precision. (1 mark)
14. Represent -7 as single precision number. (2 marks)

BITS, Pilani - Dubai
International Academic City, Dubai
II– Semester 2008-2009

Course Number	:	**CS C342**
Course Name	:	**Advanced Computer Organisation**
Nature of Component	:	**Quiz 3 – Closed book (Version - A)**
Weightage	:	5 %
Max. Marks	:	10 Marks
Duration	:	15 minutes.
Date of Examination	:	23.04.2009

Name : _____ **ID No.** _____

1. State true or false.
   If TLB is a hit and page table and cache are miss then the combination is possible.

2. _____ bit is used to set whenever a page is accessed and that is used to implement LRU.

3. Suppose the page references (in order) are 15,22,19,17,21,15 and the referenced page is 8, then _____ page will be replaced for the first page fault and if page 12 is referenced next time _____ page will be replaced for the next page fault.

4. The space on the disk reserved for the full virtual memory space of a process is called _____.

5. What should be the status of TLB where page table is a miss and cache is a hit and the _____ combination should be impossible.
   a. Hit and miss
   b. Hit or miss
   c. None of the above

6. Consider executing the following code on the pipelined datapath of MIPS.

```
add $1,$2,$3
sub $4,$5,$6
sub $7,$8,$9
add $10,$11,$12
sub $13,$14,$15
```

   How many clock cycles are required to execute all the instructions?
7. State Amdahl's law for performance improvement.
8. What will be the page size in terms of KB when 14 bits are assigned to page offset in virtual address?
9. When block size is increased, cache miss penalty _____.
10. If cache has 2^{12} words and a block size of one word, then _____ bits are used to index the cache and _____ bits are used for tag.

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II– Semester 2008-2009

Course Number	:	**CS C342**
Course Name	:	**Advanced Computer Organisation**
Nature of Component	:	**Quiz 3 – Closed book (Version - B)**
Weightage	:	5 %
Max. Marks	:	10 Marks
Duration	:	15 minutes.
Date of Examination	:	23.04.2009

Name : _____ **ID No.** _____

1. A _____ occurs if the page table entry does not have a valid physical address.

2. List the various components of memory hierarchy.

3. Suppose the page references (in order) are 15,22,19,17,21,15 and the referenced page is 8, then _____ page will be replaced for the first page fault and if page 12 is referenced next time _____ page will be replaced for the next page fault.

4. _____ is a method of resolving a branch hazard that assumes a given outcome for the branch and proceeds from that assumption rather than waiting to ascertain the actual outcome.

5. What should be the status of TLB where page table is a miss and cache is a hit and the _____ combination should be impossible.
   a. Hit and miss
   b. Hit or miss
   c. None of the above

6. Consider executing the following code on the pipelined datapath of MIPS.

```
add $1,$2,$3
sub $4,$5,$6
sub $7,$8,$9
add $10,$11,$12
sub $13,$14,$15
```

   How many clock cycles are required to execute all the instructions?

7. State Amdahl's law for performance improvement.
8. What will be the page size in terms of KB when 14 bits are assigned to page offset in virtual address?
9. _____ contains the address information required to identify whether a word in the cach corresponds to the requested word.
10. If cache has 2^{12} words and a block size of one word, then _____ bits are used to index the cache and _____ bits are used for tag.

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Course Number	:	**CS C342**
Course Name	:	**Advanced Computer Organisation**
Nature of Component	:	**Quiz 2 – Closed book (Version - A)**
Weightage	:	5 %
Max. Marks	:	10 Marks
Duration	:	15 minutes.
Date of Examination	:	30.03.2009

Name : _____ **ID No.** _____

1. The operation time for memory access is 100ps, and for ALU operation is 175ps and for register file read or write is 50ps. 425 ps is the total time taken for _____ instruction. Assume the instruction takes one clock cycle.

2. _____ is the type of hazard in the code segment and _____register is involved in the hazard.

```
sub $s1,$s2,$t3
add $t2,$s1,$t3
```

3. _____ is the type of hazard in the code segment and _____ technique is used to resolve the hazard.

```
lw $s0,12($t5)
add $t3,$s0,$s1
```

4. IF/ID register must be _____ bits wide.

5. Register file contains all the registers and has _____ read ports and _____ write port.

6. _____ is used to decide whether the incremented PC or branch target should replace the PC, based on the zero output of the ALU.

7. With an edge triggered timing methodology there is no _____ within a single clock cycle.

8. _____ and _____ are the operations of branch datapath.

9. Pipelining is a technique that exploits _____ among the instructions in a sequential instruction stream.

10. The signal ALUOp is _____ bit control signal while all the other control lines are _____ bit signals.

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Course Number	:	**CS C342**
Course Name	:	**Advanced Computer Organisation**
Nature of Component	:	**Quiz 2 – Closed book (Version - B)**
Weightage	:	5 %
Max. Marks	:	10 Marks
Duration	:	15 minutes.
Date of Examination	:	30.03.2009

Name : _____ **ID No.** _____

1. The operation time for memory access is 100ps, and for ALU operation is 175ps and for register file read or write is 50ps. _____ is the total time taken for store instruction. Assume the instruction takes one clock cycle.

2. Data hazard is the type of hazard in the code segment and ____ register will be involved in the hazard.

```
sub $s1,$s2,$t3
add $t2, ___,$t3
```

3. _____ is the type of hazard in the code segment and _____ technique is used to resolve the hazard.

```
lw $s0,12($t5)
add $t3,$s0,$s1
```

4. Every instruction begins execution on _____ and completes execution on the _____.

5. Register file contains all the registers and has _____ read ports and _____ write port.

6. _____ is used to decide whether the incremented PC or branch target should replace the PC, based on the zero output of the ALU.

7. With an edge triggered timing methodology there is no _____ within a single clock cycle.

8. _____ and _____ are the operations of branch datapath.

9. _____ takes place in the third pipe stage of a load instruction.

10. The signal ALUOp is _____ bit control signal while all the other control lines are _____ bit signals.

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II– Semester 2008-2009

Course Number	:	**CS C342**
Course Name	:	**Advanced Computer Organisation**
Nature of Component	:	**Quiz 1 – Closed book** (Version - A)
Weightage	:	5 %
Max. Marks	:	10 Marks
Duration	:	15 minutes.
Date of Examination	:	23.02.2009

Name : _____ **ID No.** _____

1. _____ is the formula for Arithmetic Mean.

2. Calculate the % of elapsed time in Unix time command
   65.2u 16.5s 3:57 _____ %

3. If a computer X is n times faster than computer Y, then the execution time of Y is n times longer than it is on X is measured by the formula.
   a. Performance $_x$ / Performance $_y$ = Execution time $_y$ / Execution time $_x$ = n
   b. Performance $_y$ / Performance $_x$ = Execution time $_y$ / Execution time $_x$ = n
   c. n * (Performance $_x$ / Performance $_y$)

4. sw instruction copies the data from _____ to _____.

5. _____is the instruction format in decimal for the instruction andi $s1,$s2,100.

6. $t1 = 0000 0000 0000 0000 0000 1101 0000 0000
   $t2 = 0000 0000 0000 0000 0000 0000 0000 0000
   Value of $to is _____ after nor $to,$t1,$t2.

7. Give the MIPS machine language for the instruction
   bne $s1,$s2,800

8. Compile the statement in MIPS where variable x is associated with register $s2 and the base address of the array B is $s3.
   B[16] = x + B[4]

9. If computer A runs a program in 25 seconds and computer B in 40 seconds, then A is _____ times faster than B.

10. _____ is the number of instructions for the program where 26 is the number of CPU clock cycles and average clock cycles per instruction is 2.