BITS,Pilani-Dubai
International Academic City
Dubai
IInd Semester,2007-08
Subject: Power Electronics (EEE UC461/INSTR UC461)
COMPREHENSIVE EXAMINATION
3rd year(EEE/EIE)----F.M=80(40%)---Duration= 3 hours- -Date -28/05/2008

(1) The reverse recovery time of a p-i-n diode is $t_{rr}$ =1.5 microseconds. The forward current of this diode is 22 amps for a considerable span of time.Calculate the peak reverse current($I_{rr}$) at a temperatute of 22 degree-centigrade, if the breakdown voltage($V_{BR}$) is 840 volts. The other given data are:
k=$(1.4)(10)^{-23}$ Joules/Degree Kelvin ; q=charge of an electron=$(1.6)(10)^{-19}$ Coulomb ;$\mu_n$ =1300 $cm^2$/V-sec. ; $\mu_p$ =470 $cm^2$/V-sec.; $E_{BR}$ =200 KV/cm. [4 Marks]

(2)(a) Explain the turn-off transients of Power Diode with necessary equations and diagrams. [6 Marks]

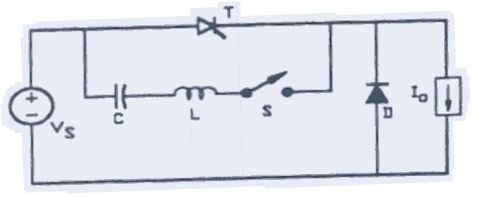
(b) Draw equivalent circuits and concerned waveforms for each of four modes, in context to Turn- off transients of MOSFET. Write the concerned equations also. [5 Marks]

(3) (a)A voltage pulse of $V_{DD}$ volts and pulse width= "a" seconds , is injected to the gate of MOSFET, in context to the Turn-on phenomenon . Derive, starting from fundamentals, the expression for gate to source voltage ($v_{gs}(t)$) as a function of time using the method of Laplace Transform or any other method. Use the equivalent circuit of Mode-1 of "Turn-on phenomenon" for the above said analysis, with following assumptions(changes) to be incorporated:
Gate to drain capacitance is realistic and it is a parallel combination of ideal capacitor($C_{gd}$ ) and a resistor($R_{gd}$ ) and
Gate to source capacitance is realistic and it is a parallel combination of ideal capacitor($C_{gs}$ ) and a resistor($R_{gs}$ ) [7 Marks]

(b) Write the concerned equations in connection with the operation of IGBT, with necessary diagrams , plots(if any) ,with a brief explanation . [5 Marks]

(4)(a) Consider the circuit diagram shown below in connection with Resonant Commutation of Thyristor. Given that, the initial voltage across the capacitor is, $v_c(0)= V_s$ volts and initial current through inductor ,is $i_L(0)= I_1$ amps. Applying the method of Laplace Transform, or otherwise, prove that :
(i) $i_L(t) = -C V_s \omega_o Sin(\omega_o t)+ I_1 Cos(\omega_o t)$ and (ii) $v_c(t) = V_s Cos(\omega_o t)+ [I_1/(\omega_o C)]Sin(\omega_o t)$ . It is given that $\omega_o$ is the resonant frequency in radians/second . Also it is given that t=0 is considered when the switch , "S" is made closed.

(b) In connection with 4(a) question, calculate the value of inductor(L) if the thyristor has a turn-off time of 20 micro-seconds. Given data are: $I_o$ =41 amps. , $V_s$ =215 volts , resonant frequency ($f_o$ )= 18 KHz and $I_1$ =0 . [6+3 Marks]




(5) (a)Explain the operation of " Isolated Buck- Boost(Flyback) Converter" or " Isolated Buck Converter"—(any one), with basic circuit diagram and individual circuit diagrams of each mode , and design aspects(if any) and necessary waveforms and necessary equations. [6 Marks]

(b) Explain the operation of a D.C-D.C boost converter with necessary equations, circuit diagrams and waveforms in continuous conduction mode. [6 Marks ]

(6) Third Harmonic component of voltage output of a single phase PWM Inverter has to be eliminated by the method of "NOTCHING". Develop the final algorithm, with $\alpha_k = \pi/2$. Start the analysis from fundamentals. Draw necessary waveforms, clearly. [8 Marks]

(7) Explain different control techniques for A.C to D.C conversion with necessary circuit diagrams and waveforms. [10 Marks]

(8) Consider a resonant tank loaded with a current sink in voltage source excitation:
(a) Develop the STATE PLANE TRAJECTORY starting from fundamentals ,using normalized state variables.
(b) "If the input voltage source terminals are short circuited within themselves, then also the State Plane Trajectory can be developed"----- Justify this statement ,with proper reasoning (mathematical or physical) , in context to the analysis of part (a) question. [10+4 Marks]

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**3rd year(EEE/EIE)--Test II(OPEN BOOK) --F.M=20(20%)---Duration=50 min.- -**
**Date -20/04/2008**

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**Instructions: Text Book and Ref. Book 1(as per handout) (photocopies also) and classnotes( handwritten and photocopies) are allowed.**

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**(1)A Boost converter operating in CCM has following parameters: Input voltage,$V_s$=10 volts, L=225 µH, Load resistance=20.0 ohm,C=470 µF, ON time($T_{ON}$) =.03milliseconds , OFF time($T_{OFF}$) =.02milliseconds . Calculate:**
**(a) Average output voltage (b) Peak to peak ripple in voltage output (c) Value of Duty Ratio (D) for which output current for boundary case( $I_{OB}$) will be minimum (d) Minimum value(magnitude) of $I_{OB}$ [6 Marks]**

**(2) With a neat ciruit diagram, explain the operation of a Tansformer-coupled gate drive circuit (triggering circuit) of Thyristor. Function of each circuit component must be explained. Also,explain in detail, why the PULSE TRANSFORMER is used in this circuit. [7 Marks]**

**(3)(a)In connection with the circuit of "IMPULSE COMMUTATION" of Thyristor, shown in Fig. 1, $C_1$ and $C_2$ are series connected. $C_1 = C_2$=3.0 µF and thyristor turn – off time is 20 µs. Each capacitor is pre-charged to "-80" volts. Calculate the value of constant load current ($I_O$) with switch closed.**

**(b) With reference to part (a) question, a resistor of 100 ohm is connected in parallel with the capacitors combination. Calculate, after how much time gap with effect from the closing of the switch, the total capacitor combination will be charged to "zero" voltage. Load current ($I_O$) value remains same as obtained in part(a) question. [2+5 Marks]**

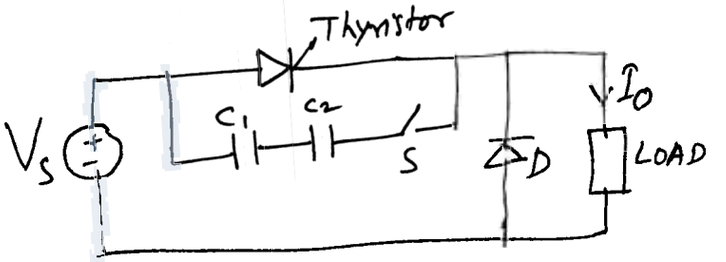


Fig. 1

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**3rd year(EEE/EIE)--Test I--F.M=25(25%)---Duration=50 min.- -Date -09/03/2008**

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**(1)(a)Explain only the design aspects (or, trade off aspects) of "Schottky Barrier Diode(SBD)", writing the concerned equations.**
**(b) "The Ohmic junction undermines the Schottky barrier properties"—Explain this statement , with necessary equations . [4+2 Marks]**

**(2) Explain the turn-on and turn-off transients of Power Diode with necessary equations and diagrams. [6+5 Marks]**

**(3) A voltage pulse of $V_{DD}$ volts and pulse width= "a" seconds , is injected to the gate of MOSFET, in context to the Turn-on phenomenon . Derive, starting from fundamentals, the expression for gate to source voltage ($v_{gs}(t)$) as a function of time using the method of Laplace Transform or any other method. Use the equivalent circuit of Mode-1 of "Turn-on phenomenon" for the above said analysis,after suitable modifications. [8 Marks]**