BITS, PILANI – DUBAI
International Academic City, Dubai
BE (Hons) CS III Year – 2nd Sem

ADVANCED COMPUTER ORGANISATION – CS UC 342
COMPREHENSIVE EXAM (Closed book)

Date: 01 June 2008
Time: 3 hrs **Max Marks: 80**

Note: Answer all questions

1. a. CellMorph is a photo-editor for your cellphone. Morphing an image requires floating-point operations. High-end cellphones come equipped with a floating-point coprocessor that CellMorph uses. For low-end cellphones (without the coprocessor), the program uses integer-based software routines to perform the floating-point operations. Both types of cellphones use a 20MHz processor. The high-end cellphone has a CPI of 10 and takes 1 second to morph an image, whereas the lowend cellphone has a CPI of 6 and takes 10 seconds for the same task.
i) What is the total number of instructions executed for both runs? 3 mks
ii) On the average, how many integer instructions does it take to perform a floating point operation in software? 2 mks

b. A RISC assembler is especially written to process the output of a CISC compiler for running the code on a RISC machine. This assembler treats CISC instructions as RISC pseudoinstructions. It is found that on an average one CISC instruction produces four RISC instructions. The code from the CISC compiler, when run on a CISC computer, takes 8 cycles per instruction (CPI). The RISC computer for the modified code takes 1.5 CPI and this RISC computer has a 1.5 times faster clock. Show how fast or slow is the RISC computer when compared to the CISC computer for executing the program 5 mks

2. a. Compute the value of R1 at the end of each of the following instructions. The last two operands are added and the result is placed in the first operand (R1) 3 mks

S.No	Instruction	Addressing mode for the last operand	Result in R1
1	Add R1, R2, 40	Memory indirect	
2	Add R1, R2, 40	Immediate	
3	Add R1,R2, 40	Memory direct	

Memory

10	20
20	10
30	50
40	30
50	60
60	70
70	50

Registers

R1	20
R2	2
R3	60
R4	30
R5	40
R6	50
R7	70

b. For each of the instructions specified in 2 (a), give the corresponding instruction(s) in MIPS and specify addressing modes used. 7 mks

3. a. Consider the following IEEE 754 single precision floating point format number, represented in hexadecimal. What is the equivalent value as a decimal number: 43E30000 5 mks

b. What are the different floating point instructions available in MIPS. Indicate the function of each instruction. 5 mks

4. a. Which MIPS instruction(s) determines the cycle time of a single-cycle datapath? 2 mks

b. If memory access takes 200 ps, instruction decode and register operation takes 100 ps, and ALU operation requires 200 ps, then find the upper bound on the clock rate of a single-cycle datapath. 4 mks

c. Does the execution of the following sequence of instructions generate a hazard? If yes, can the hazard be handled without a pipeline stall? Illustrate the handling of hazard by a sketch of pipeline stages using a multi cycle MIPS data path. 4 mks

```
add   $s0, $t0, $t1
add   $t2, $s0, $t3
```

5. a. A disk drive spins at 7200 RPM. On a typical disk access, the heads must move 213 tracks at a rate of 5 microseconds/track plus 250 microseconds for settling. What is the average latency for an access in milliseconds? 3 mks

b. Assume 512 bytes/sector; 270 sectors/track; 4500 tracks/surface; 16 surfaces are available in a disk drive. What is the minimum number of disk drives required to store a 3 dimensional array of size 16K X 16K X16K X 8 bytes. 2 mks

c. What is RAID. Discuss the different levels of RAID 5 mks

6. a. How does a data cache take advantage of spatial locality? 2 mks

b. Imagine a 4 word cache with an access pattern of 0, 1, 2, 3, 4, 0, 1, 2, 3, 4. Calculate the hit rate for a direct mapped cache and for a fully associative cache with an LRU replacement policy. Show the complete set of steps 4 mks

c. Let's say we have a 20-bit virtual address, with a 4 KB page size. Let's assume that the system we're running upon has a maximum of 1 GB of physical memory. How big is each page table? (assume 2 extra bits of information are needed beyond the usual stuff). Give the answer in terms of total number of bits in the page map table. 4 mks

7. a. Given the code fragment below, how many processes will be created by executing this code and how will they be related to one another? Explain your answer. (Be sure to

cover the cases where some or all of the system calls fail, as well as the case where all of them succeed.) 5 mks

```
void main (){
int . childpid;

for (i = 0; i < 10; i++
    childpid = fork();

    if (childpid > 0){

        exit(2);
    }
    else if (childpid < 0){
        fprintf(stderr, "Error with fork.\n");
        exit(1);
    }
  }
```

b. What are the dependencies in the loop below? Is this loop parallel (i.e. can the loop iterations be executed in parallel? Explain why. 5 mks

```
for (I = 1; I <= 100; I++) {
A[I] = A[I] + B[I]; /* S1 */
D[I+1] = D[I] + E[I]; /* S2 */
B[I+1] = C[I] + D[I+1]; /* S3 */
}
```

8. Write short notes on any two: 10 mks

a. Microprogrammed Control Unit

b. Digital Signal Processing

c. Modes of data transfer

BITS, PILANI – DUBAI
International Academic City, Dubai
BE (Hons) CS III Year – 2nd Sem

Advanced Computer Organisation CS UC342
Test 2 (Open Book)

Date: 11 May 2008 **Time: 50 min** **Max Marks: 20**

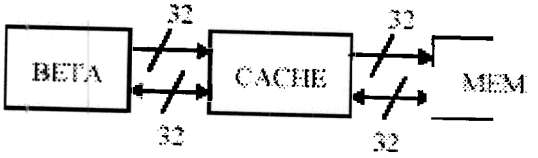
Note: Answer all questions.

1. For the following MIPS code sequence, state if the memory accesses show: temporal locality, spatial locality, both or neither, based on justification. 3 mks

```
        addi $t0, t0, 100
LOOP:   lw $t1, 19196($s0)
        lw $t2, 0($s0)
        addi $t0, $t0, -1
        bne $t0, $zero, LOOP
```

2. Consider the following diagram showing a Beta CPU and its memory system. Useful facts:

. Beta has 32-bit byte addresses
. Beta has 32-bit data and instructions
. main memory reads/writes 1 word (32-bits) in a single cycle
. Cache is **direct-mapped** with 4 entries
. each cache entry has a 1-word (32-bit) data block
. each cache entry has a 1-bit "dirty" flag
. each cache entry has a 1-bit "valid" flag
. cache implements a **write-back** strategy



a. How many total bits of tag are there in the cache? 5 mks

b. Assume the access time of the cache is 5 ns and the access time of the memory is 50ns. Accesses to main memory are initiated only after the cache misses. If we want the Beta to see an average access time of 8ns, what does the average cache hit rate have to be? 5 mks

3. Assume a 1GHz computer, which averages 3 cycles per instruction, is connected to the Internet via a 10,000,000 bits/sec connection (i.e., the line speed allows 10 million bits to pass every second). From the time the computer receives the first bit, how many instructions can the computer execute while waiting for a single 8-bit character to arrive? 2 mks

4. What complexity does DMA present to the management of cache memory? 5 mks

BITS, PILANI – DUBAI
International Academic City, Dubai
BE (Hons) CS III Year – 2nd Sem

Advanced Computer Organisation – CS UC342
Test 1 (Closed Book)

Date: 30 March 2008 **Time: 50 min** **Max Marks: 25**

Note: Answer all questions.

1. a. Using MIPS conventions, perform a move operation of register 7 to register 5 (in other words, after the end of this instruction, register 5 should contain the value that was stored in register 7) using a single instruction. 2 mks

b. For the instruction defined above give the instruction format that is to be used. Explain each field in the format. 3 mks

2. a. The following information is given about a processor. The instruction mix is relative to a particular benchmark program. What is the average CPI of the processor? 2 mks

	Instruction Class			
	A	B	C	D
CPI	2	3	4	5
Instruction mix	45%	25%	15%	15%

b. Consider a program P, which runs on a 1 GHz machine M in 10 seconds. An optimization is made to P, replacing all instances of multiplying a value by 4 (mult x,x,4) with two instructions that set x to x+x twice (add x,x; add x,x). call this new optimized program P'. The CPI of a multiply instruction is 4, and the CPI of an add is 1. After recompiling, the program now runs in 9 seconds on machine M. How many multiplies were replaced by the new compiler? 3 mks

3. Consider the following value, using the IEEE 754 single precision format. What is the equivalent value as a decimal number? 3 mks

0100 0010 1010 1100 0000 0000 0000 0000

4. a. What are the different ways in which a new value can be loaded into the program counter of MIPS. Draw the data path to illustrate the same. 3 mks

b. In the multicycle machine discussed in the class five stages (IF, ID, ALU, MEM, WB) were used. Assume the clock cycle to be 200 psec. 4 mks

i. If the time for the ALU operation can be shortened by 25%, what will be the clock cycle? Will it effect the speed obtained by pipelining? If yes, why and if not why not?
ii. If the ALU operation now takes 25% more time, what will be the clock cycle? Will it effect the speed obtained by pipelining? If yes, why and if not why not? 3 mks

5 Write short notes on the following 5 mks
a Addressing modes in MIPS
b Floating point addition