BITS,Pilani-DUBAI CAMPUS
Knowledge Village,Dubai
Semester II, 2006-2007
COMPREHENSIVE EXAMINATION (Closed Book)
B.E(Hons.) III rd year(EEE/EIE) (Course Title—POWER ELECTRONICS)
Course No. EEE UC461/INSTR UC461 M.M=80 (Weightage 40%)
Date-- 28-05-2007 Time—3 hours

(1) (a) Explain "TURN-ON TRANSIENT" of p-i-n diode with suitable diagram. (6 M)

1(b) The reverse recovery time of a p-i-n diode is t_{rr}=1.2μs .The forward current (I_f)of this diode is 25 amps for a considerable span of time. Calculate the peak reverse current (I_{rr}) at a temperature of 22 degree-centigrade , if the breakdown voltage is , V_{BR} =810 Volts . The other given data are :
k=(1.4) $(10)^{-23}$ Joules/Degree Kelvin ; q=charge of an electron =(1.6) $(10)^{-19}$ Coulomb ; E_{BR} =200 KV/cm. ; μ_n =1300 cm^2/V-sec. ; μ_p=470 cm^2/V-sec.
(4Marks)

(2) (a) What do you mean by "INVERSION LAYER" in MOSFET? ---- Explain with necessary diagrams(with labeling).
(2+1 Marks)

(2) (b) Explain the TURN-ON Transients of a MOSFET, with necessary circuit diagrams/plots and equations, in different modes. (7 Marks)

(3)(a) Explain the Impulse Commutation of Thyristor with necessary equations and circuit diagrams.
(7 Marks)

(3) (b) Explain any one Gate Drive Circuit for triggering of Thyristor. (3 Marks)

(4) (a) Explain the operation of a " Full Bridge D.C-D.C Converter with bi-polar switching" with basic circuit diagram and individual circuit diagrams for each mode and the necessary waveforms and necessary equations.
(7 Marks)

(4)(b)In connection with question 4(a),derive the equation of Linear Switch-Mode Amplifier.(3 M)

(5) (a) Explain the operation of a Full –bridge Inverter(VSI) with square-wave switching and with A.C. Voltage Sink load .Draw circuit diagrams and waveforms.

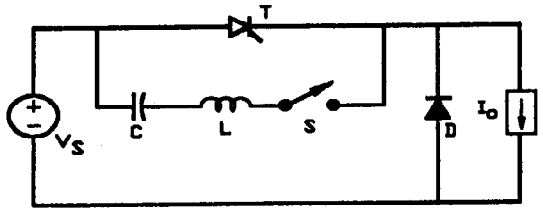
P. T. O.

Also derive the necessary equations.
(6 Marks)

(5) (b) A 240 Volts(r.m.s),400 Hz utility grid is connected to the output of a 1-phase VSI through a 5.0 mH inductor. The inverter is excited from 320 volts D.C source and it delivers 1.1 KW power to the utility grid (a.c BUS). Calculate the phase angle φ_1 in the inverter operation for $v_{a.c} = 240\sqrt{2}\,\mathrm{Sin}(\theta - \varphi_1)$.
(4 Marks)

(6) Consider the discontinuous conduction mode topology of a Series Resonant D.C-D.C Converter with Voltage Sink. Draw the circuit diagrams for mode-1 and mode-2 and develop the "STATE PLANE TRAJECTORY" in each mode, deriving the necessary equations and solutions for state variables, ,in details, starting from fundamentals(using normalized quantities).
(1+1+6+6 Marks).

(7) (a) Consider the circuit diagram shown below in connection with Resonant Commutation of Thyristor. The initial voltage across the capacitor is $v_c(0) = V_S$ Volts. Applying the method of Laplace Transform for solution , or otherwise , prove that : (i) $v_c(t) = V_S \cos \omega_o t$ and (ii) current through the inductor , $i_L(t) = -(V_S/\omega_o L)\sin \omega_o t$. ω_o is the resonant frequency in radians/sec.
t=0 is considered as the instant when the switch ,"S" is closed. Also , $i_L(0) = 0$.
(3+2 Marks)



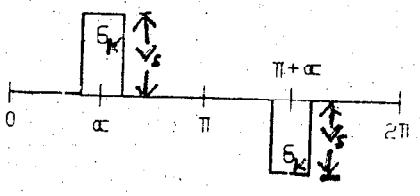
(7)(b) In connection with 7(a) question, calculate the value of inductance(L) if the Thyristor has a turn off time of 25 micro –seconds. $I_o = 45.0$ amps., $V_S = 200.0$ Volts and resonant frequency (f_o) =15.0 KHz.
(3 Marks)

(8)(a) Explain the operation (Converter Operation) of a 1-phase,2-pulse full bridge A.C-D.C Converter with constant output current with "PHASE ANGLE DELAY CONTROL". Draw basic circuit diagram and topologies of each mode.
(4 Marks)

8((b) Consider the "THIN PULSE"(of width equals to δ_k) as shown below, in connection with Harmonic Elimination by Notching. With reference to harmonic analysis of this pulse, prove that

$$b_n = (4V_S/n\pi)\mathrm{Sin}(n\alpha)\,\mathrm{Sin}(n\delta_k/2) \text{ --- for } n = 1,3,5,7 \ldots\ldots$$
$$= 0 \text{ ---------- for } n = 2,4,6,8 \ldots\ldots$$

(4 Marks)



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Semester-I I 2006-2007

Test II (OPEN BOOK)

BE(Hons.) III year (EEE/EIE) (Course-Power Electronics)

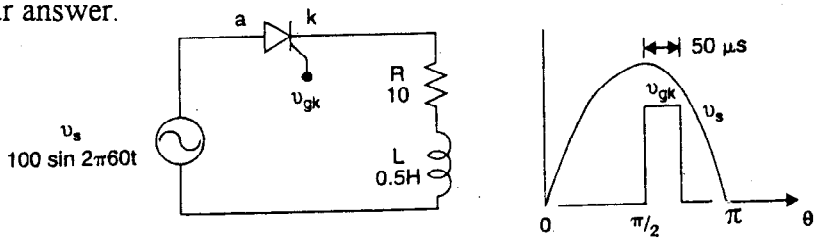
Course No. EEE UC461/INSTR UC461 M.M=20 (Weightage 20%)

Date 08-04-2007 Time: 50 Minutes

Note:

1. Answer all the questions.
2. All the symbols carry their usual meanings unless otherwise stated.
3. Text Books (and Photocopies),Class-notes (and Photocopies) are allowed.

(1) (a)The thyristor in the circuit below has a holding current of 20 mA . A 50 μs wide gate trigger pulse is applied at the delay angle of $\pi/2$. Will the thyristor turn on? Explain your answer.



(b) In connection with part-(a) question, if the thyristor does not turn on, it is suggested to add a resistor in parallel with the R-L load. Determine the value of additional resistance that would just enable the thyristor to turn on . (2M + 3M)

(2) (a) In connection with the circuit of "IMPULSE COMMUTATION " of thyristor , the capacitor is pre-charged to -160 volts. C=6.0 μF and thyristor turn off time is 20 μs. Calculate the value of constant load current(I_o),with switch closed.

(b)In context to part (a) question, if a resistor of 5.0 ohms is connected in parallel with the capacitor, calculate, after how much time gap, with effect from the closing of the switch, the capacitor will charge up to +160 volts. The load current remains same. (2M+4 M)

(3) A Boost converter operating in CCM has following parameters:

V_S =5.0 volts, L=250 μH, Load resistance(R_L)= 20.0 ohm, C= 470 μF, Switching frequency(f_s) =20.0 kHz ,Duty ratio(D) =0.4. Calculate:

(a) Average output voltage ; (b) Peak to peak voltage ripple in the output ; (c) Value of I_{OB} (1M+2M+1M)

(4) (a)Prove that, from fundamentals, duty ratio(D) for which the Voltage Transfer Ratio (T_w) of a BUCK-BOOST Converter(operating in CCM) will be maximum, will have a very large value(infinite).

(b) Why is the polarity of "DIODE" made reversed in BUCK-BOOST Converter as compared to that in the BOOST Converter ?----Explain

(c) Under what condition the assumption of inductor current (in any D.C-D.C Converter) to be linear with respect to time is valid ?—Explain (3M+1M+1M)

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Semester-I I 2006-2007
Quiz I (CLOSED BOOK)
BE(Hons.) III year (EEE/EIE)
Course Title-Power Electronics **(SET-A)**
Course No. EEE UC461/INSTR UC461 M.M=20 (Weightage 10%)
Date 22-03-2007 Time: 30 Minutes

Name:
ID NO.

Marks Distribution Q.(1) to Q.(12)—1*12 AND rest questions-----2*4

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(1) In a n-channel MOSFET, thickness of the inversion layer becomes minimum :
(a)at the gate end (b) at the drain end (c) at the source end (d) none of the above

(2)In a MOSFET, the gate to drain capacitance(C_{gd}),the capacitance across the insulator layer (C_{ox}) and the capacitance across depletion region (C_s) are related by :
(a) $C_{gd} = C_{ox} + C_s$
(b) $C_{gd} = (C_{ox} + C_s)/2$
(c) $C_{gd} = (C_{ox} C_s)/ (C_{ox} + C_s)$
(d)) $C_{gd} = (C_{ox} + C_s) /4$

(3)With reference to TURN-ON TRANSIENTS of a MOSFET : (where τ is the time constant)
(a) $v_{gs}(t) = V_{DD} (1-e^{-t/\tau})$
(b) $v_{gs}(t) = V_{DD} (1-e^{-t/\tau})^2$
(c) $v_{gs}(t) = (V_{DD} /2) (1-e^{-t/\tau})$

(4) IGBT can be considered as a combination of :
(a) Two transistors (b) One MOSFET and one transistor (c) One MOSFET and two transistors (d) One MOSFET,two transistors and one power diode

(5)Transconductance(g_m) of MOSFET is :
(a)proportional to (LZ) (b) proportional to (L^2/Z) (c)proportional to (1/LZ) (d) proportional to (Z/L)

(6)With reference to "Turn On Transients of MOSFET", during the time span, when V_{ds} is decreasing from peak value to almost zero value(linearly) ,then :
(a)I_d decreases linearly (b) I_d decreases but in a non-linear manner (c) I_d increases linearly (d) I_d becomes constant

(7) An IGBT cell is very much similar to the MOSFET cell except that:
(a)the n^+ layer in SOURCE region is replaced by p^+ layer (b) the n^+ layer in SOURCE region is replaced by n^- layer (c)the n^+ layer in DRAIN region is replaced by p^+ layer

(8) A thyristor is remaining in "FORWARD BLOCKING STATE". Then the junctions of the device will behave as:
(a) J_1 and J_3 ---Forward biased ; J_2—Reverse biased (b) J_1 ---Forward biased ; J_3, J_2—Reverse biased (c) J_1 and J_2 ---Forward biased ; J_3—Reverse biased (d) J_1 and J_3 ---Reverse biased ; J_2—Forward biased

(9) In the expression for I_A of Thyristor ,value of$(\alpha_1 + \alpha_2)$ approaches unity(1.0). It will indicate:
(a) Negative feedback (b) Positive(regenerative) feedback (c) No feedback (d) Open-circuit
(10) Two transistors analogy relates to : (a)MOSFET (b)IGBT (c)Thyristor (d)Power diode
(11)The turning off problem of Thyristors is taken care of by another device called ---------- and in that modified device the value of $(\alpha_1 + \alpha_2)$ is maintained ---------- than unity.
(12) Draw the low-frequency equivalent circuit of MOSFET.

(13) Write the expression for I_A of Thyristor in terms of current gains of resolved transistors (α_1 and α_2) and gate current(I_G) and reverse saturation currents(I_{co1} and I_{co2}) of the resolved transistors.

(14) A particular MOSFET has: R_g = 0.8 ohm; C_{gs} =2500 pico farads ; C_{gd} =350 pico farads ; V_{DD} =15.0 Volts ;Threshold Voltage, V_T =4.0 volts. With reference to "TURN ON Transients of MOSFET", write the expression for time required(t_1) by the "gate to source voltage" to reach the value of V_T. Also calculate the numerical value of time(t_1).

(15) Why is a Thyristor to be protected against high values of "dV/dt" and "dI_F/dt" ?

(16) Draw the circuit diagram for Impulse Commutation of Thyristor and write the expression for its "Turn-off time (t_{off})".

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Semester-I I 2006-2007
Test I (CLOSED BOOK)
BE(Hons.) III year (EEE/EIE)
Subject-Power Electronics
Course No. EEE UC461/INSTR UC461 M.M=20 (Weightage 20%)
Date 25-02-2007 Time: 50 Minutes

Note:

1. Answer all the questions
2. All the symbols carry their usual meanings unless otherwise stated
3. All questions carry equal marks

(1)Why is a Power Diode referred as **p-i-n** diode?----Explain from the view point of construction along with necessary diagrams. Also explain the phenomenon of "Conductivity Modulation" in the **p-i-n** diode.

(2)With reference to the switching characteristics of **p-i-n** diode , explain "Turn-Off-Transient" and prove that $t_{rr} = AV_{BR}\sqrt{\frac{I_f}{di_r/dt}}$;

$$where\ A = \frac{1}{E_{BR}}\sqrt{\frac{q}{kT}\frac{2}{\mu_p + \mu_n}}$$

(3)State or Explain the salient points of "SCHOTTKY BARRIER DIODE",with necessary equations. Also explain any one design aspect of that device.

(4) Draw the diagram of a basic enhancement mode n-channel MOS cell. Starting from fundamentals, prove that the channel resistance can be expressed as given by:

$$R_{ch} = \frac{v_{ds}}{i_D} = \frac{L}{Z\mu_n C_{ox}(v_{gs} - V_T)}$$