BITS, PILANI – DUBAI CAMPUS
Knowledge Village, Dubai
BE (Hons) CS III Year – 2nd Sem

ADVANCED COMPUTER ORGANISATION – CS UC 342
COMPREHENSIVE EXAM (Closed book)

Date: 29 May 2007
Time: 3 hrs **Max Marks: 80**

Note: Answer all questions

Part A (20 mks)

All questions carry equal marks

1. For the following IEEE single precision values below, explain what they represent. If the quantity has a numeric value give it.
   a) 0111 1111 1000 1111 0000 1111 0000 0000
   b) 0100 0010 0100 0000 0000 0000 0000 0000

2. The 32-bit value 0x30A79847 is stored to the location 0x1000 in MIPS. What is the value of the byte in address 0x1002 if the MIPS is
   a) Big endian?
   b) Little endian?

3. Every subprogram must have the instruction:
   jr $ra
   Is it true or false? Justify your answer.

4. Two processor designs M1 and M2 implement the same architecture but with different performance characteristics, as shown below:

Machine	CPI	Clock Frequency
M1	3.2	1 GHz
M2	4	2 GHz

   When we run benchmark program P it executes 20 Million instructions.
   (a) What will be the execution time of program P on machine M1?
   (b) What will the execution time of program P on machine M2?

5. What are the steps required to add two floating point numbers?

6. The MIPS branch instructions are beq and bne can only change the current program counter by a limited amount. How many instructions (or words) can be reached relative to the program counter?

7. A cache has 1024 blocks and each block can hold 128 bytes of data. Assuming a 32-bit main memory address, give the address corresponding to the first byte in the data block of the cache containing data from the following addresses:
   a) 0xA23847EF
   b) 0x7245E824

8. A parent and a child process are communicating using pipes. A two way flow of data is required.
   a) Give commands needed to create the pipe.
   b) Show which ends of the pipe are needed to be closed in the parent and the child processes to establish the bidirectional communication

9. What is DMA? How is it different from interrupts?

10. Why do RISC architectures use fixed-width instructions?

Part B (60 mks)

11. a) Explain the addressing modes available in MIPS. 5 mks

    b) Translate the following code into MIPS assembly: 5 mks

    $$A = B - C - 30 + D - E + F$$

    Assume that variables A, B, C, D, E, F are in registers $s1, $s2, $s3, $s4, $s5, $s6. Also, assume that you cannot overwrite variable, A, B, C, D, E, F; since they will all be used later in the program. Write the code such that it uses the minimal number of registers. How many additional registers (other than $s1 to $s6) does your code require? Indicate against each MIPS instruction, the type of the instruction format (Give the field breakup)

12. A virtual address space is specified by 16 bits and the corresponding physical memory space by 12 bits. 10 mks
    a. How many words are there in the virtual address space
    b. How many words are there in the physical memory space
    c. If a page consists of 256 words, how many pages and frames are there in the system?
    d. Show with the help of a diagram how a virtual address is mapped to a physical address.

13. With the help of a diagram, explain the data path and list all the micro operations required to execute the following instruction: 10 mks
    lw $t1, 2000($t2)

14. List and explain the main kinds of hazards that can arise when using a pipelined implementation. Propose a solution for each of them. 10 mks

15. a) Explain the Flynn's taxonomy for multiprocessors. Give an example for each class. 5 mks

b) Suppose we want to sum 100,000 numbers on a single-bus multiprocessor computer. Let's assume we have 100 processors. Explain how this job can split between the 100 processors and how they would synchronize with each other in order to get the result. 5 mks

16. Write short notes on the following: 10 mks
(a) Digital Signal Processors
(b) Microprogramming

BITS, PILANI – DUBAI CAMPUS
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Test 2 (Open Book Exam)

Date: 29 April 2007
Time: 50 min

Max Marks: 20

Note: Answer all questions

1. Differentiate between loosely coupled and tightly coupled parallel computers. (2 mks)

2. What is cache coherence. Explain with the help of a diagram of a parallel computer that is being used. Show a case wherein a read request could cause a problem and another wherein a write request could cause a problem. (4 mks)

3. A parent process spawns off a child process and passes two data values to the child process. The child process receives the two numbers from the parent process, computes their sum and sends the result back to the parent process. The parent process prints the result. The data exchanges between the parent and the child processes uses the unix pipe mechanism. Write a C program using fork(), pipe(), dup2, waitpid() system calls which were discussed in the class. (6 mks)

4. Consider the following sequence of instructions to be executed in a 5 stage pipelined processor discussed in the class. R1, R2, ...R9 are general purpose registers. The explanation of each instruction is given as comments (starting with //)

```
LOAD  R2, 2000(R3)     // R2 = M(2000+R3)
ADD   R1, R2, R3       // R3 = R1 + R2
MUL   R4, R3, R1       // R1 = R4 * R3
SUB   R7, R8, R9       // R9 = R7 – R8
```

   a. Identify data dependencies which exist between the instructions. (1 mk)

   b. Give two different solutions to the data hazards arising in the above code. Draw pipeline execution diagrams for each solution. (6 mks)

   c. Based on the pipeline execution diagrams, which of the two solutions suggested by you is a better solution in terms of overall execution time.(1 mk)

BITS, PILANI – DUBAI CAMPUS
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Advanced Computer Organisation – CS UC 391
Test 1

Date: 18 March 2007
Time: 50 min **Max Marks: 20**

Note: Answer all questions

1. Conversion from decimal to IEEE floating point (in Binary form) 4 mks
   0.015625

2. Give the flowchart for multiplication of two unsigned 32 bit binary numbers using a standard "shift and add" sequential multiplier with a 32 bit register for multiplier and 64 bit register for multiplicand and product. 2 mks

3. Processor X has a clock speed of 1 GHz, and takes 1 cycle for integer operations, 5 cycles for memory operations, and 6 cycles for floating point operations. Empirical data shows that programs run on Processor X typically are composed of 35% floating point operations, 30% memory operations, and 35% integer operations. You are designing Processor Y, an improvement on Processor X which will run the same programs and you have an option to set the clock speed to 500 Mhz, and with memory operations handled by a cache memory with a miss penalty of 20 clock cycles for 5% of the memory operations, and a cache access takes 1 clock cycle. Number of cycles for integer and floating point operations remains the same. Is this going to improve the performance. If so by how much and if not by how much? 8 mks

4. Trace the following code: 6 mks

```
add $t0, $t1, $t2
nor $t3, $t1, $ zero
sltu $t3, $t3, $t2
bne $t3, $zero, address
```

Show the contents of the registers before and after the execution of each line

BITS, PILANI – DUBAI CAMPUS
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Advanced Computer Organisation – CS UC391
Quiz (B)

Date: 01 March 2007
Time: 30 min

Max Marks: 20

ROLL NO:_____ **NAME:**_____

Note: Answer all questions

I. State whether true or false (5 mks)

1. A stack machine can have zero operands
2. If the clock speed is 200 MHz, then the cycle time is 50 picoseconds.
3. In IA-32 there is an instruction to move data from register to memory
4. In MIPS register $zero can contain any constant.
5. In the branch instruction format, the branch address is interpreted as number of bytes after branch instruction
6. In the stored program concept the high level language program along with the data is stored in the main memory
7. Stack grows from higher address to lower address in MIPS
8. The frequency of usage of arithmetic operations is generally greater than the frequency of usage of load/store operations
9. The inputs to a compiler and an assembler are one and the same
10. The MIPS architecture allows for retrieval of operands from memory in arithmetic instructions.

II. Multiple Choice (5 mks)

1. For a given instruction set architecture, performance increase can come from?
   a) increases in clock rate
   b) improvements in processor organization that lower CPI
   c) optimisations in compiler which decrease the number of instructions to be executed
   d) all of the above
2. Using MIPS convention, which of the following instruction can be used to move data from register $t7 to register $t5?
   a) add $t7, $t5, $zero
   b) add $t5, $t7, $zero
   c) add $zero, $t5, $t7
   d) add $zero, $t7,$t5
3. The execution time which is used to measure performance includes
   a) elapsed time for system
   b) CPU time taken by system programs only

c) CPU time taken by user programs only
d) All of the above

4. In the procedure calling conventions of the MIPS architecture which of the following are required to be saved to the stack on a procedure call.
   a) The arguments to the procedure
   b) The values returned by the procedure
   c) The return address for use at the completion of this procedure
   d) All of the above
5. The statement A[12] = h + A[8] has to be converted to MIPS assembly code. Assume A is an array of 100 words. The compiler associated variable h with register $s2. The base address of array is in $s3. Which of the following is the correct MIPS code.

   a)
   ```
   lw $t0, 8($s3)
   add $t0, $s2, $t0
   sw $t0,12($s3)
   ```
   b)
   ```
   lw $t0, 16($s3)
   add $t0, $s2, $t0
   sw $t0,24($s3)
   ```
   c)
   ```
   lw $t0, 32($s3)
   add $t0, $s2, $t0
   sw $t0,48($s3)
   ```
   d)
   ```
   lw $t0, 0($s3)
   add $t0, $s2, $t0
   sw $t0,0($s3)
   ```

III. Short Answers (10 mks)

1. Consider the sequence of four instructions shown below.

```
loop: lw $6, 0($5)
      add $7, $7, $6
      addi $5, $5, -4
      bne $5, $8, loop
```

In the space provided below, show the decimal representation of each of the four instructions in this sequence. Clearly show the values filled in each field. Fields which are not relevant to a particular format should be marked as n.a. (not applicable) 7 mks

Instruction	Format	rs1 (source 1)	rs2 (source 2)	rd (destination)	Immediate
lw $6, 0($5)					
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2. Assume that you have the option of implementing an enhancement to a processor that reduces the number of instructions in an average program by 5%. In addition assume that due to this enhancement the clock cycle is increased by 10%. The CPI remains the same. What is the overall improvement in performance? (3 mks)

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Quiz (B)

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Time: 30 min **Max Marks: 20**

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Advanced Computer Organisation – CS UC 391
Quiz (A)

Date: 01 March 20007
Time: 30 min **Max Marks: 20**

ROLL NO:_____ **NAME:**_____

Note: Answer all questions

I. State whether true or false (5 mks)

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3. A stack machine can have zero operands
4. In IA-32 there is an instruction to move data from register to memory
5. The MIPS architecture allows for retrieval of operands from memory in arithmetic instructions.
6. If the clock speed is 200 MHz, then the cycle time is 0.5 picoseconds.
7. In MIPS register $zero can contain any constant.
8. In the branch instruction format, the branch address is interpreted as number of bytes after branch instruction
9. Stack grows from higher address to lower address in MIPS
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B) The values returned by the procedure
C) The return address for use at the completion of this procedure
D) All of the above
E) None of the above

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