BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
SECOND SEMESTER 2005 – 2006
EEE UC 371 ELECTROMECHANICAL ENERGY CONVERSION
Comprehensive Examination (CLOSED BOOK)

MAXIMUM MARKS: 60 **WEIGHTAGE: 30%**
DATE: 16.05.06 DURATION: 3 Hours

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1. Explain the external characteristics of a dc shunt generator. Also explain how the external characteristic of a dc shunt generator is different from that of a separately excited generator. **[3+3 Marks]**

2. A dc motor takes an armature current of 110 A at 480 V. The resistance of the armature circuit is 0.2 Ω. The machine has 6 poles and the armature is lap connected with 864 conductors. The flux per pole is 0.05 Wb and iron and friction losses are 2 kW. Calculate **[6 Marks]**
   i) speed
   ii) torque developed by the armature.
   iii) Mechanical power developed by the armature.
   iv) Motor Output

3. Estimate the percentage reduction in speed of a separately excited dc generator working with constant excitation on 400 V constant voltage bus bars to reduce its load from 600 kW to 400 kW. The machine resistance is 0.02 Ω. Neglect armature reaction. **[6 Marks]**

4A) What are the constants or parameters of the equivalent circuit that are determined from OC and SC tests of a transformer and how these are calculated? **[4 Marks]**
4B) From which side (LV or HV) OC test is conducted and why? Why is the copper loss almost negligible in this test? **[2 Marks]**

5. A 5000 kVA, 3 phase Δ/ Y connected 6.6kV/33 kV transformer has a full load copper loss of 35 kW. The impedance drop (per phase) at full load is 7%. Calculate the percentage regulation when a load of 3200 kW at 0.8 pf lagging is delivered at 33 kV. **[6 Marks]**

6. Explain what is meant by fractional slot winding and discuss its advantages and limitations. **[3+3 Marks]**

7. Explain why induction motors can not operate at synchronous speeds. Also explain what is meant by slip speed and breakdown torque. **[4+2 Marks]**

8. A 4 pole, 50 Hz three phase induction motor has, at rated voltage and frequency, a starting torque of 160 percent and a maximum torque of 200 percent of full load torque. Determine **[4+2 Marks]**
i) full load speed ii) speed at maximum torque

9. What do you mean by phase splitting? Explain with a neat schematic diagram, the operation and torque-speed characteristics of a two-value capacitor motor. **[6 Marks]**

10. A 500 V, single phase synchronous motor gives a net output mechanical power of 7.46 kW and operates at 0.9 pf lagging. Its effective resistance is 0.8 Ω. If the iron and friction losses are 500 W, calculate the efficiency. **[6 Marks]**

BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
SECOND SEMESTER 2005 – 2006
EEE UC 371 ELECTROMECHANICAL ENERGY CONVERSION
TEST II (OPEN BOOK)

MAXIMUM MARKS: 20

DATE: 16.04.06 DURATION: 50 MINUTES

1. A 4-pole series motor has 944 wave-connected armature conductors. At a certain load the flux per pole is 34.6 mWb and the total mechanical power developed is 4kW. Calculate the armature current and the speed at which the motor will run with an applied voltage of 500 V. The total motor resistance is 3 Ω. **[7 Marks]**

2. Design a suitable double layer lap winding for a 6-pole dc armature with 18 slots and two coil-sides per slot. Give the values of front pitch, back pitch and commutator pitch. **[3 Marks]**

3. A 200 V shunt motor has $R_a = 0.1\Omega$ and $R_f = 240\ \Omega$. On full load, the line current is 9.8 A with the motor running at 1450 rpm. Determine **[5 Marks]**
   i) the mechanical power developed
   ii) torque developed by the armature
   iii) full load efficiency if rotational losses are 236 W.

4. Describe **any two** speed control schemes which provide a constant-torque drive for a dc shunt motor. **[5 marks]**

BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
SECOND SEMESTER 2005 – 2006
EEE UC 371 ELECTROMECHANICAL ENERGY CONVERSION
QUIZ II (CLOSED BOOK)

MAXIMUM MARKS: 10 (B) **WEIGHTAGE: 10 MARKS**
DATE: 06.04.06 **DURATION: 30 MINUTES**

NAME:					ID NO.					
QUESTION	1	2	3	4	5	6	7	8	9	10
ANSWER										

1. In an unsaturated dc machine the armature reaction effect is
A) cross-magnetizing
B) de-magnetizing
C) magnetizing
D) dependent on whether the machine is generating or motoring

2. Which of the following statement is true with respect to compensating windings in a dc a machine
A) produce mmf in such a direction to aid armature mmf
B) series connected with armature
C) reduce main field ampere turns
D) All the above

3. The armature reaction in a dc machine
A) are in the same direction as the main poles
B) are in direct opposition to the main poles
C) make an angle with the main pole axis other than 90°
D) make an angle of 90° with the main pole axis

4. For the voltage build up of a self excited dc generator, which of the following is not an essential condition?
A) There must be some residual flux
B) Field winding mmf must aid the residual flux
C) Armature speed must be very high
D) Total field circuit resistance must be less than the critical value

5. A dc motor can be looked upon as a dc generator with the power flow
A) increased
B) reduced
C) reversed
D) modified

6. The critical resistance in a dc shunt generator is
A) the resistance of the field circuit
B) the value of the field circuit resistance above which the generator would fail to excite
C) the value of the field circuit resistance below which the generator would fail to excite
D) the value of the field circuit resistance for which the flux/pole is not reliable

7. The motor best suited for hoist, crane and traction type load is
A) dc series motor
B) induction motor
C) dc shunt motor
D) synchronous motor

8. Which is the completely correct statement in a dc shunt motor
A) No load speed is directly proportional to flux/pole and inversely proportional to armature voltage
B) No load speed is directly proportional to flux/pole and directly proportional to armature voltage
C) No load speed is inversely proportional to flux/pole and inversely proportional to armature voltage
D) No load speed is inversely proportional to flux/pole and directly proportional to armature voltage

9. A series motor should not be run on no load because
A) it will draw dangerously high current
B) it will not run
C) it will run dangerously at high speed
D) None of the above

10. Interpoles help commutation in a dc machine by
A) aiding the main poles
B) neutralizing reactance voltage
C) increasing brush resistance
D) increasing armature reaction

BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
SECOND SEMESTER 2005 – 2006
EEE UC 371 ELECTROMECHANICAL ENERGY CONVERSION
QUIZ 1(CLOSED BOOK)

MAXIMUM MARKS: 10 (A) **WEIGHTAGE: 10 MARKS**
DATE: 23.03.06 **DURATION: 30 MINUTES**

NAME:						ID NO.				
QUESTION	1	2	3	4	5	6	7	8	9	10
ANSWER										

1. A Δ / Y transformer has a phase-to-phase voltage transformation ratio of k (Δ phase): 1 (Y phase). The line-to-line voltage ratio for Y/ Δ is given by:
a) k / √3 b) k√3/1 c) √3 / k d) k /1

2. On the two sides of a Y/ Δ transformer:
a) the line voltages and currents are both in phase
b) the line voltages and currents both differ in phase by 30°
c) the line voltages and currents differ in phase by 30° but currents are in phase
d) the line currents differ in phase by 30° but voltages are in phase

3. In a Scott-connected transformer the number of main primary and teaser primary turns respectively is:
a) N, 2/√3 N b) N/2, N c) √3 N/2, N d) N, √3 N/2

4. In a Scott-connected transformer the neutral point divides the teaser primary winding in the ratio
a) 2:1 b)√3:1 c) 1:√3 d) √3:2

5. Which of the following statements are true with respect to a Scott-connected transformer?
a) Under balanced load conditions, main transformer rating is 15% lower than that of teaser.
b) Under balanced load conditions, main transformer rating is 15% greater than that of teaser
c) Under balanced load conditions, main transformer rating is equal to that of teaser
d) None of the above

6. The number of parallel paths in the two types of dc armature winding namely, lap winding and wave winding respectively are:
a) 2, P/2 b) 2, P c) P, 2 d) P/2 ,2

7. If S= number of slots and P=number of poles then in a symmetrical three phase fractional slot winding

a) S/3P=fraction, S/3= fraction
b) S/3P=fraction, S/3= integer
c) S/3P=integer, S/3= fraction
d) S/3P=integer, S/3= integer

8. The fractional slot windings are used because

a) it results in saving in machine tools
b) it reduces the high frequency harmonics caused by slotting
c) All the above
d) None of the above

9. If U= number of coil-sides /slot and Y_{cs}=coil span in slots then the back-pitch of a dc winding is given by:

a) $UY_{cs}-1$ b) UY_{cs} c) Y_{cs} d)$UY_{cs}+1$

10. The chording means

a) coil span made less than one pole pitch
b) coil span made more than one pole pitch
c) coil span made equal to one pole pitch
d) fractional slot winding

BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
SECOND SEMESTER 2005 – 2006
EEE UC 371 ELECTROMECHANICAL ENERGY CONVERSION
TEST 1(CLOSED BOOK)

MAXIMUM MARKS: 20 **WEIGHTAGE: 20%**
DATE: 05.03.06 DURATION: 50 MINUTES

1. i) Derive the expression for total approximate voltage drop in transformer secondary from a neatly drawn primary phasor diagram. Neglect exciting current I_0 and assume primary and secondary power factor angles to be equal.

   ii) Assuming a leading power factor, derive the condition for zero voltage regulation. **[4+1Mark]**

2. Explain, with a neat diagram, a testing procedure for a single phase transformer where the input to the transformer consists of both iron loss and full load copper loss.
   Also state the limitations of this testing method. **[5 Mark]**

3. The efficiency of a 400-kVA, single phase transformer is 98% when delivering full load at 0.8 p.f. and 99% at half load and unity p.f.
   Calculate
   i) the iron loss
   ii) copper loss at quarter load
   iii) Load at which maximum efficiency occurs. **[5 Mark]**

4. A 5-kVA, 250/500-V, 50 Hz, 1-phase transformer gave the following test results:

   No-load : 250 V, 0.75 A, 60 W (L.V. side)
   Short circuit : 9 V, 6 A, 22 W (H. V. side)

   Calculate
   i) the magnetizing current and the iron loss component current at normal voltage and frequency.
   ii) the efficiency at full-load at unity power factor.
   iii) the corresponding terminal voltage on full load at unity power factor.
   [5 marks]

BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester II 2005 – 2006
Comprehensive Examination (Closed Book)

Course No.: **EEE UC 391** Course Title: **DECO**

Date: May 17, 2006 Time: 3 Hours Max. Marks = 75

(Answer questions from Part A and Part B on separate answer sheets .
Calculators are not allowed. State any assumptions made clearly.
Unless stated otherwise, assume all logic gates are using positive logic.)

PART A

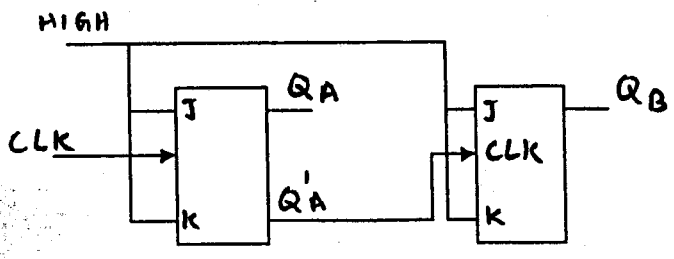
1. a) Given the following equation, determine the base x that permits the equation to be true. $(24)_x + (17)_x = (40)_x$
   b) Assuming the two input AND gate delay is T seconds, write a formula for the gate delay of an N input AND gate implemented using 2-input AND gates.
   c) What range of decimal values can be represented by a four-digit hex number?
   (3+2+2)

2. a) Prove that $XZ + Y'Z + Z' = X + Y' + Z'$ using Boolean laws.
   b) Draw the Multi level NOR realization for the expression $F = W (X + Y + Z) + XYZ$
   c) Design a combinational circuit which will convert a 3-bit number into its 2's complement. In your design use only the following components.
   Four 2- input XOR gates and one 2- input AND gate. (1.5 + 2.5 + 4)

3. a) Explain the construction of a 4 x 1 Mux with three-state buffers and a 2 – 4 decoder. Also show how this circuit can be used as a Half adder.

   b) A BCD code is being transmitted to a remote receiver. The bits are $A_3A_2A_1A_0$ with A_3 being the MSB. The receiver circuit includes a BCD error detector circuit that examines the received code to see if it is a legal BCD code. Design this circuit to produce a HIGH for any error condition.
   (4 + 4)

4. For the ripple counter shown in figure, draw the complete timing diagram for eight clock pulses showing the clock, Q_A and Q_B waveforms.



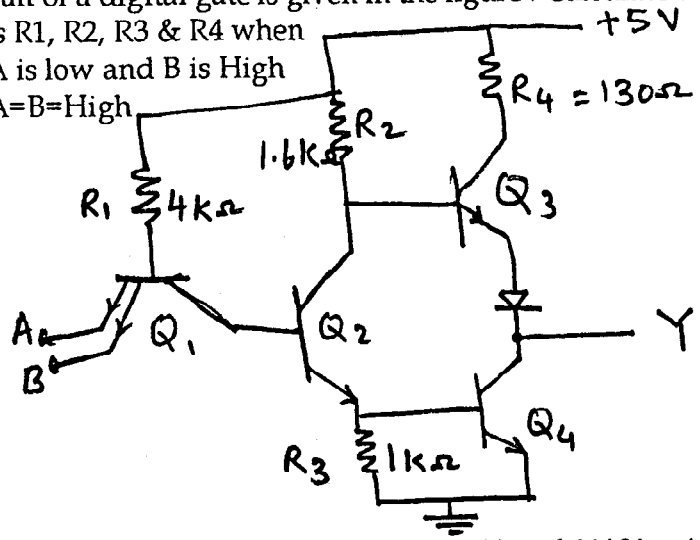
(7)

5. Design a sequential circuit to generate the sequence 111101 . (7)

PART B

6. a) Draw the logic programming fuse map for a four bit binary to gray code converter PROM. Also tabulate the PROM.
   b) Given a 32 x 8 ROM chip with enable input, show the external connections necessary to construct a 128 x 8 ROM with four chips and a decoder. (4+3)

7. The circuit of a digital gate is given in the figure . Calculate the voltage drop across the resistors R1, R2, R3 & R4 when
   a) A is low and B is High
   b) A=B=High



(4+4)

8. Multiply the two given binary numbers 11000 and 11101 using
   a) shift and add method b) Booth's algorithm
   Compare the processes and their results. (3+3+2)

9. The gate -level description of a circuit using Verilog HDL and its stimulus to analyse the circuit are given below.
   a. Draw the corresponding logic circuit marking the input and output signals
   b. Write the results printed on the monitor for the given stimulus . (4+4)

```
//Gate-level description of circuit
module analysis (A,B,C,F1,F2);
   input   A,B,C;
   output  F1,F2;
   wire    T1,T2,T3,F2not,E1,E2,E3;
   or  g1 (T1,A,B,C);
   and g2 (T2,A,B,C);
   and g3 (E1,A,B);
   and g4 (E2,A,C);
   and g5 (E3,B,C);
   or  g6 (F2,E1,E2,E3);
   not g7 (F2not,F2);
   and g8 (T3,T1,F2not);
   or  g9 (F1,T2,T3);
endmodule
```

```
//Stimulus to analyze the circuit
module test_circuit;
  reg [2:0]D;
  wire F1,F2;
  analysis fig42(D[2],D[1],D[0],F1,F2);
  initial
    begin
     D = 3'b000;
     repeat(7)
      #10 D = D + 1'b1;
    end
  initial
     $monitor ("ABC = %b F1 = %b F2 =%b ",D, F1, F2
endmodule
```

10. A sequential circuit has two JK flip flops A and B and one input x. The circuit is described by the following flip flop input equations.
    $J_A = x$; $K_A = B'$; $J_B = x$; $K_B = A$; Derive the state equations A(t+1) and B(t+1) and draw the state diagram of the circuit. (7)

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BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester II 2005 – 2006
Test II Mk-up (closed Book)

Course No.: **EEE UC 391** Course Title: **DECO**

Date: April 25, 2006 Time: 50 Minutes Max. Marks = 30

1. Using a positive edge triggered AB flip-flop whose characteristic table is given below, design a synchronous mod-6 counter whose counting sequence is as given below.
   000 – 110 – 101 – 011 – 010 – 001 – 000 …., etc.
   (force the unused states to 000 as next state)

A	B	Q(t+1)
0	0	0
0	1	Q'
1	0	Q
1	1	1

2. Using a PAL device with 3 inputs, 3 outputs and 3wide AND-OR structure realize the following set of Boolean functions. List the PAL program table and sketch the fuse map.
   $F1(x,y,z) = \Sigma (1,2,4,6,7)$
   $F2(x,y,z) = \Sigma (2,4,5,6)$
   $F3(x,y,z) = \Sigma (1,4,6)$

3. Draw the state diagram for the state table given below

Pr. St.	Next state				outputs			
	X_1X_2=00	01	10	11	X_1X_2=00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

Also draw the corresponding logic circuit using T-flip flops and basic logic gates.

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BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester II 2005 – 2006
Test II (closed Book)

Course No.: **EEE UC 391** Course Title: **DECO**

Date: April 23, 2006 Time: 50 Minutes Max. Marks = 30

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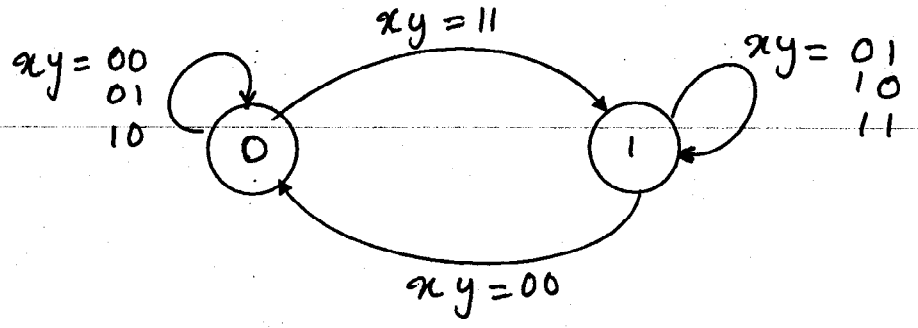
1. The pair of Boolean functions F_1 (A, B, C, D) = Σ (2,4,5,10,12,13,14) and F_2 = Σ (2,9,10,11,13,14,15) are to be realized with a minimum size PLA having true outputs. Draw the PLA programming table and the logic diagram in PLD notation.

(10 M)

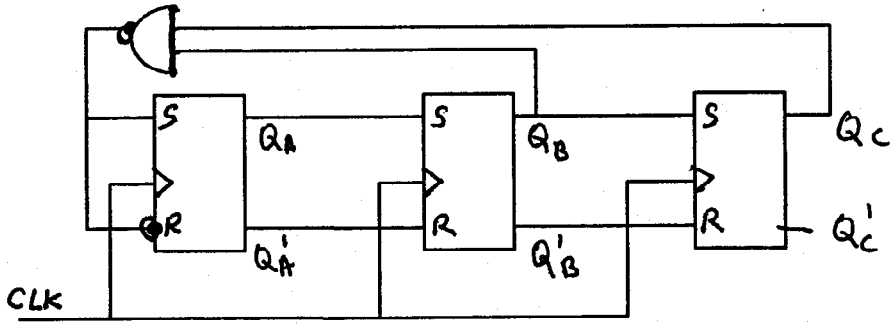
2. For the sequential circuit whose state diagram is given below, do the circuit realization using T-Flip Flops and basic two input logic gates.



(10 M)

3. Analyse the counter given below and draw the complete state diagram. Also find the invalid state or states. An invalid state is one that is not in the counter's normal sequence.

Assume that initially all stale (FF) is cleared.



(10 M)

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BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester II 2005 – 2006
Quiz (closed Book) Mk -Up

Course No.: **EEE UC 391** Course Title: **DECO**

Date: April 6, 2006 Time: 30 Minutes Max. Marks = 20

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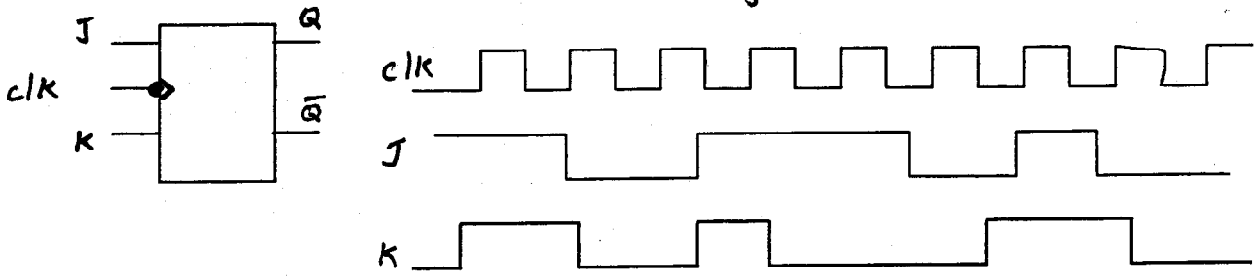
1. Use 10's complement arithmetic to compute $(53 - 87)_2$. Comment on your result.

2. The Binary equivalent of the gray code 1101100 is _____

3. (a) In a J-K flip Flop, the inputs are supplied as shown in the figure. Draw the out put Q of the flip flop. Assume $Q = 0$ initially.



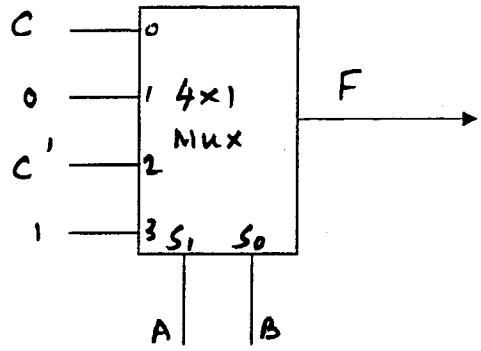
4. The complement of $\overline{A}B + \overline{C}D$ is _____.

5. Write a Boolean expression which will produce a high output when A < B where A & B are 4-bit binary words.

6. Find the Prime Implicants and Essential Prime Implicants of the Boolean function $Y(A,B,C,D) = \Pi\,(2,3,4,5,10,11,12,13)$

7. Implement the reduced function of the Boolean expression given in Q6. using single logic gate.

8. The function implemented by the circuit shown in figure below is _____



9. Implement the X-OR function using 2-input NAND gates.

10. Implement a half adder using an active low 2 x 4 decoder and minimum no. of logic gates.

BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester I 2005 – 2006
Test I (Closed Book)

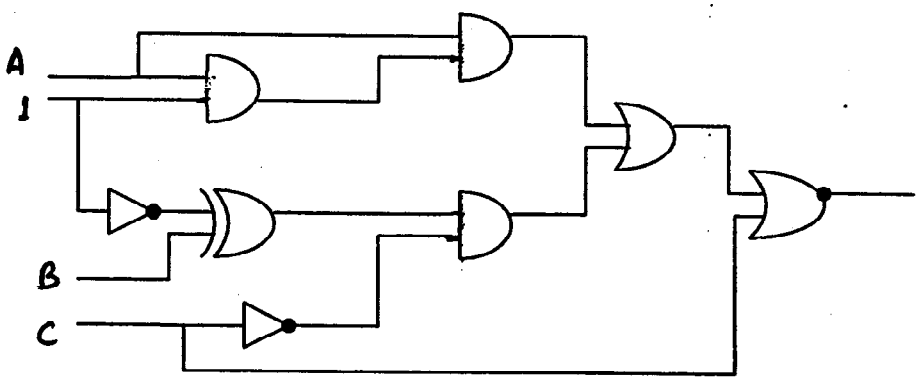
Course No.: **EEE UC 391** Course Title: **DECO**

Date: March 12, 2006 Time: 50 Minutes Max. Marks = 30

(Answer all questions. Calculators are not allowed)

1. a) Convert the following
   i) 110101 in Binary is equivalent to _____ in Gray code
   ii) $(783.375)_{10}$ = (_____)$_8$ = (_____)$_{16}$ = (_____)$_2$
   iii) Using 2's complement arithmetic to compute $(10 - 21)_{10}$ and analyse the result.
   (2+3+2)

2. Write the logic expression of the function implemented by the circuit shown below. Simplify the function and implement it using a single logic gate



(4)

3. Simplify the SOP function below and draw the circuit using K-Map. Also find the prime Implicants and essential prime Implicants of the function. (5)
   $P(w, x, y, z) = \Sigma(0,1,4,5,6,7,8,9,14,15)$

4. Design a combinational logic circuit using three half adders which will implement the following four Boolean functions

   a) $F_1(A, B, C) = A \oplus B \oplus C$ *b)* $F_2(A, B, C) = A'BC + AB'C$

   c) $F_3(A, B, C) = ABC' + (A' + B')C$ *d)* $F_4(A, B, C) = ABC$ (5)

5. Draw a BCD adder circuit using two 4 -bit binary parallel adders. Explain its operation in steps with the inputs *A = 1001 and B = 0011* (4)

6. Implement the following Boolean function using a 2 to 4 decoder and a 4 to 1 Multiplexer
   $F(A, B, C, D,) = \Pi(0, 1, 3, 4, 5, 7, 8, 9, 10)$ (5)

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