BITS, PILANI – DUBAI CAMPUS
KNOWLEDGE VILLAGE, DUBAI
III Year Second Semester 2005 – 2006
ADVANCED COMPUTER ORGANISATION CS UC 342
Comprehensive Examination (Closed Book)

Time : 3 hours **Weightage : 40%**
29.05.06 **MAX : 40 MARKS**
Answer all the questions.

1. a. What is datapath? (1 mark)
   b. Define Abstraction. (1 mark)

2. a. Explain the instruction slt $s5,$s3,$125. (1 mark)
   b. For the given values, identify the instruction and the format. 43,20,17,300. (2 marks)
   c. With diagram, explain base addressing. (1 mark)
   d. For the instruction sub $t4,$s1,$s4 find the corresponding hexadecimal code. (2 marks)

3. a. Add $2.36 * 10^2$ to $7.46 * 10^3$ assuming that there are only three significant digits, first with guard and round digits and then without them. (2 marks)
   b. Represent -5.0 in single precision float by converting to binary. (1 mark)
   c. Represent -0.4375_{ten} in binary normalized notation. (1 mark)

4. a. Generate MIPS code for the segment in C, assume all variables are in memory and are addressable as offsets from $t0. Find the hazards in the code segment and reorder the instructions to avoid any pipeline stalls. (3 marks)

```
A = B + E;
C = D + F;
```

   b. The operation time for memory access is 100ps and for ALU operation is 150ps and for register file read or write is 50ps. Find the total time taken for store word instruction. Assume the instruction takes one clock cycle. (1 mark)

5. a. Calculate the % of elapsed time in Unix time command (1 mark)
   65.2u 16.5s 3:57 _____ %
   b. Define workload. (1mark)
   c. Computer X has a clock cycle time of 400ns and a CPI of 2.3 for some program and computer Y has a clock cycle time of 560ns. If computer X is faster by 1.095 times, find the CPI? (1 mark)

6. What are the three different types of instruction classes? Explain the steps in detail to execute the instructions with examples. (3 marks)

7. a. Why it is difficult to write parallel processing programs ? (1 mark)
   b. Define snooping. Explain the different types of snooping protocols with diagram. (1 mark)
   c. Discuss about MESI protocol. (1 mark)

8. a. Define microprogramming. (1 mark)
   b. What are the various DSP applications? (1 mark)
   c. Distinguish between DSP and general purpose processor. (2 marks)

9. a. Briefly explain about direct mapped cache with diagram. Also represent in a diagram for a direct mapped cache with 16 entries, the addresses of memory words in binary 2,3,11,16,21,13,64,48,19,11,3,22,4,27,6. Specify whether it is a hit or miss. (3 marks)
   b. Distinguish between temporal and spatial locality. (1 mark)
   c. What are the various techniques to maintain consistency of data between memory and cache during writes. Discuss them in detail. (2 marks)

10. a. With example, illustrate how asynchronous buses work for reading a word from memory. Explain all the steps in detail with diagram. (3 marks)
    b. What are the different techniques of communicating I/O device with the processor. Explain them in detail. (2 marks)

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TEST – II (Open Book)
Makeup

Time : 50 minutes **Weightage : 20%**
MAX : 20 MARKS

Answer all the questions. Only Text Book is allowed. Class Notes will not be allowed.

1. Explain cache coherency steps and bus traffic for four processors P0,P1,P2 and P3. Consider what happens when one processor releases the lock and the remaining processors attempt to read the lock simultaneously. (5 marks)

2. Consider executing the following code on the pipelined datapath of MIPS.

```
lw $3, 40($4)
sub $5,$3,$2
add $8,$7,$9
or  $11,$12,$13
add $1,$11,$5
```

   a. How many clock cycles are required to execute all the instructions? (1 mark)
   b. Identify all of the data dependencies in the. Which dependencies are data hazards that will be resolved via forwarding? Which dependencies are data hazards that will cause a stall? Explain in detail. (3 marks)
   c. Show the steps in detail needed to execute the above instructions with diagram. (2 marks)

3. Outline clearly the need for different units and multiplexors in single cycle data path of MIPS and the purpose of every control signal needed for executing all the basic instructions (5 marks)

4. If the maximum I/O rate of CPU is 20,000 I/Os/second and CPU can sustain 4. billions of instructions per second and it needs 200,000 instructions per I/O operation. Find the instructions in the Operating System per I/O. (4 marks)

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TEST – II (Open Book)

Time : 50 minutes **Weightage : 20%**
30.04.06 **MAX : 20 MARKS**

Answer all the questions. Only Text Book is allowed. Class Notes will not be allowed.

1. A memory backplane bus is capable of sustaining a transfer rate of 1500 MB/sec and the maximum I/O rate of bus is 11,719 I/O's/second. Find I/O transfer. (2 marks)
2. Explain in detail, with diagram all the steps needed to execute the following instructions (3 marks)

```
add $3,$4,$6
sub $5,$3,$2
lw $7,100($5)
add $8,$7,$2
```

3. Consider executing the following code on the pipelined datapath of MIPS.

```
add $1,$2,$3
sub $4,$5,$6
sub $7,$8,$9
add $10,$11,$12
sub $13,$14,$15
```

How many clock cycles are required to execute all the instructions? Explain with diagram. (2 marks)

4. Identify all of the data dependencies in the following code. Which dependencies are data hazards that will be resolved via forwarding? Which dependencies are data hazards that will cause a stall? Explain in detail. (3 marks)

```
add $3,$4,$2
sub $5,$3,$1
lw $6,200($3)
add $7,$3,$6
```

5. State Amdahl's law for performance improvement. (1 mark)
6. What will be the page size in terms of KB when 14 bits are assigned to page offset in virtual address. (1mark)
7. A benchmark executes in 200 seconds of elapsed time and it takes 10% of elapsed time for I/O. If CPU time improves by 25% for the first year, 35% for the second year, 50% for the third year and improves by 60% for the remaining years . If I/O time improves by 10% for the first year, 15% for the second year and then it does not improve. How much faster will the program run at the end of five years.
   a. Find the improvement in CPU performance over 5 years . (2 marks)
   b. Find the improvement in elapsed time. (2 marks)
   c. Find the improvement in I/O time. (2 marks)
   d. Find the improvement in %I/O time. (2 marks)

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QUIZ – II (Closed Book)
Make up

Time : 30 minutes **Weightage : 10%**
MAX : 10 MARKS

1. The operation time for memory access is 100ps, and for ALU operation is 150ps and for register file read or write is 50ps. _____ is the total time taken for store word instruction. Assume the instruction takes one clock cycle.

2. The following code segment has data hazard . _____ will be the register involved in the hazard.
   Sub $t1,$s2,$t3
   Add $t2,$s5,____

3. A _____ branch is one that causes transfer to the branch target.

4. In _____ transaction memory will assert DataRdy signal since it is providing the data.

5. To increase the effective bus bandwidth _____ the bus when it is not being used for transmitting information.

6. State true or false.
   It is advantageous in synchronous buses, where every device on the bus run at the same clock rate.

7. Fully associative TLB has a lower _____ rate.

8. Pipelining improves performance by increasing _____ and decreasing _____.

9. Store word is an example of _____ type of instruction class.

10. Performance of a machine is determined by _____ key factors.

11. Program counter is used to hold the address of _____instruction.

12. When the instruction immediately following branch is always executed independent of branch condition, then it is called as _____.

13. Page table register points to _____.

14. If the OS chooses to replace the page, _____ bit indicates whether the page needs to be written out.

15. Translation Look aside buffer is a _____ that keeps track of recently used address mappings to avoid an access to the page table.

16. _____ , _____ are the different types of misses.

17. Suppose the page references (in order) are 25,12,19,7,11,25,16,12 and the referenced page is 10, then _____ page will be replaced for the first page fault .

18. What should be the status of TLB where page table is a hit and cache is a miss and the combination should be possible.
    a. Hit
    b. Miss
    c. None of the above

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QUIZ – II (Closed Book)
Version - A

Time : 30 minutes
13.04.06

Weightage : 10%
MAX : 10 MARKS

Each blank carries half mark.

1. The operation time for memory access is 100ps, and for ALU operation is 175ps and for register file read or write is 50ps. _____ is the total time taken for store word instruction. Assume the instruction takes one clock cycle.

2. _____ is the type of hazard in the code segment and _____ register is involved in the hazard.
   Sub $s1,$s2,$t3
   Add $t2,$s1,$t3

3. _____ is the type of hazard in the code segment and _____ technique is used to resolve the hazard
   Lw $s0,12($t5)
   Add $t3,$s0,$s1

4. State true or false.
   If TLB is a hit and page table and cache are miss then the combination is possible.

5. _____ bit is used to set whenever a page is accessed and that is used to implement LRU.

6. Suppose the page references (in order) are 15,22,19,17,21,15 and the referenced page is 8, then _____ page will be replaced for the first page fault and if page 12 is referenced next time _____ page will be replaced for the next page fault.

7. _____ is an example of I/O bus standard.

8. Memory reference instructions use _____ register for address calculation.

9. In MIPS, Program Counter increments each instruction by the value _____.

10. The operation time for memory access is 150ps, and for ALU operation is 250ps and for register file read or write is 75ps. _____ is the total time taken for set less than instruction. Assume the instruction takes one clock cycle.

11. The space on the disk reserved for the full virtual memory space of a process is called _____.

12. _____ is used to select from among several inputs based on control lines.

13. To compute memory address load instruction adds _____and _____.

14. In sequential elements output depends on input and _____.

15. _____ is used to connect I/O bus to memory.

16. What should be the status of TLB where page table is a miss and cache is a hit and the combination should be impossible.
    a. Hit and miss
    b. Hit or miss
    c. None of the above

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TEST – I (Closed Book)
Makeup

Time : 50 minutes

Weightage : 20%
MAX : 20 MARKS

1. Define Instruction Set Architecture. (1 mark)
2. What is displacement addressing? (1 mark)
3. For the instruction add $s0,$a1,$s7 find the corresponding hexadecimal code. (2 marks)
4. Draw the instruction format for MOV EBX,[EDI +45] (1 mark)
5. Given a branch on register $s6 being equal to register $s7

   beq $s6,$s7,L5

   replace it by a pair of instructions that offers a much greater branching distance. (1 mark)
6. Using 4 bit numbers, divide 9_{ten} by 2_{ten}. Show the different iterations and values of registers at each step. (2 marks)
7. Add $2.36 * 10^2$ to $7.46 * 10^3$ assuming that you have only three significant digits, first with guard and round digits and then without them. (2 marks)
8. The miss rate for cache is 23%. Find the hit rate. (1 mark)
9. Distinguish between temporal and spatial locality. (1 mark)
10. What are the various techniques to maintain consistency of data between memory and cache during writes(1 mark)
11. Computer X has a clock cycle time of 400ns and a CPI of 2.3 for some program and computer Y has a clock cycle time of 560ns and a CPI of 1.8 for the same program. Which computer is faster and by how much? (2 marks)
12. Define response time. (1 mark)
13. In the table execution time of 2 programs on 2 different computers is given in the table. Find which computer is faster and by how much? (2 marks)

	Computer X	Computer Y
Program 1(seconds)	5	12
Program 2(seconds)	875	200

14. For the given MIPS assembler code, what is the MIPS machine code if loop is starting at lo 40000 in memory. (2 marks)

```
Loop :   sll  $t1,$s3,4
         Add $t1,$t1,$s6
         lw $t0,400($t1)
         bne $t0,$s5,Exit
         addi $s3,$s3,1
         j Loop
Exit
```

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Time : 50 minutes **Weightage : 20%**
19.03.06 **MAX : 20 MARKS**
Answer all the questions

1. State the principle of stored program concept. (1 mark)
2. If $t3 has the base of the array B and $s4 corresponds to x, the assignment statement B[400] = x + B[250]
   a. Give the equivalent MIPS instruction. (Use only one temporary register) (1 mark)
   b. Give the equivalent MIPS code in decimal with all the fields and the formats. (1 mark)
3. What is the MIPS assembly code to load the 32 bit constant into register $s0? (1 mark)
4. What is immediate addressing? (1 mark)
5. What is the assembly language statement corresponding to the machine instruction?
   026F8812 hex (2 marks)
6. Give an example for string instruction. (1 mark)
7. Using 4 bit numbers multiply $4_{ten} * 3_{ten}$. Show the different iterations and the values of registers at each step. (2 marks)
8. Compile the C program into MIPS assembly code

```
float sample( float x)
{
        return ((22.0/7.0) * (x + 5.0));
}
```

   Assume that the floating point argument x is passed in $f14 and the result should go in $f5. What is the MIPS assembly code? (2 marks)
9. Consider a cache with 128 blocks and a block size of 8 bytes. What block number does byte address 1600 map to? (1 mark)
10. How many total bits are required for a direct mapped cache with 16KB of data and one word block? (1 mark)
11. Represent in a diagram for a direct mapped cache with 8 entries, the addresses of memory words in binary 26,3,26,18. Specify whether it is a hit or miss. (2 marks)
12. What are the basic components of performance? (1mark)
13. A program runs 20 seconds on computer, which has a 8 GHz clock. Find the number of clock cycles. (1mark)
14. For the table given below, which code sequence executes the most instructions? Which will be faster and what is the CPI for each sequence. (2 marks). CPI for Program A is 1 and for B it is2

Code Sequence	Instruction counts for instruction class	
	A	B
1	3	2
2	2	4

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QUIZ – I (Closed Book)
Version - A

Time : 30 minutes
02.03.06

Weightage : 10%
MAX : 10 MARKS

1. To maximize performance _____ response time.

2. _____ time is the time spent in the operating system performing tasks on behalf of the program.

3. _____ is the formula for Arithmetic Mean.

4. Calculate the % of elapsed time in Unix time command
   65.2u 16.5s 3:57 _____ %

5. _____ is the number of instructions for the program where 26 is the number of CPU clock cycles and average clock cycles per instruction is 2.

6. If computer A runs a program in 25 seconds and computer B in 40 seconds, then A is _____ times faster than B.

7. If a computer X is n times faster than computer Y, then the execution time of Y is n times longer than it is on X is measured by the formula.
   a. Performance $_x$ / Performance $_y$ = Execution time $_y$ / Execution time $_x$ = n
   b. Performance $_y$ / Performance $_x$ = Execution time $_y$ / Execution time $_x$ = n
   c. n * (Performance $_x$ / Performance $_y$)

8. _____ instruction copies the data from register to memory.

9. Give the sequence of instructions that adds 4 variables w,x,y,z and store the final result in a.

10. $s0 = 0000 0000 0000 0000 0000 0000 0000 1000
$s1 = 0000 0000 0000 0000 0000 0000 0000 0110
Value of $to is _____ after sltu $to,$s0,$s1

11. Convert 11100101 to decimal.

12. Convert A84E to binary.

13.Convert 0111 1101 1111 1001 to hexa.

14. _____ instruction is used to set upper 16 bits of a constant in a register.

15. The mnemonic **beq** stands for _____.

16. Define Instruction Set Architecture.

17. _____ is the instruction format in decimal for the instruction sub $t0,$s1,$s2.

18. Compile the statement in MIPS where variable x is associated with register $s2 and the base address of the array B is $s3.

B[16] = x + B[4]

19. Given
bne $s5,$s7,L1
replace it by a pair of instructions that offers a much greater branching distance.

20. Give the MIPS machine language for the instruction
beq $s1,$s2,100