BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai

Year III – Semester I 2013– 2014

Comprehensive Examination

Course No.: **CS F342** Course Title: **Computer Architecture**

Date: **29.12.13 (AN)** Time: **3 hours** Max. Marks = **80** Weightage **(40%)**

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1. Show in the table format, the overflow conditions for the addition and subtraction. [4 M]

2. Briefly explain with neat diagram, the data path in operation for an R- type instruction. [8 M]

3. Three copies of data may exist in: cache, memory, and disk which leads to the Stale Data Problem, write few possible solutions to avoid them. [4 M]

4. RAID 4 and RAID 5 use roughly the same mechanism to calculate and store parity for data blocks. How does RAID 4 differ from RAID 5 and for what applications would RAID 5 be more efficient [6 M]

5. What is the average time to read or write a 1024 byte sector for a typical disk rotating at 7,200 RPM? The advertised average seek time is 11 ms, the transfer rate is 34 MB/sec, and the controller transfer rate is 480 Mbits/sec. Assume that the disk is idle so that there is no waiting time. [6 M]

6. Expand the acronyms [4 M]
   SISD, MIMD, SIMD SPMD

7. A computer system uses 16 GB virtual memory and 4 GB physical memory. The physical memory is byte addressable and the page size is 4 K bytes. [6 M]

   i) What is the size of the page offset in the virtual and physical address?

   ii) What is the number of page table entries?

   iii) Give a diagram showing how a virtual address would be translated to a physical address.

8. What is the difference between the jal and jr instructions? [4 M]

9. Provide the hexadecimal encodings of the following instructions? [6 M]

```
sll  $t2 , $s0,  4
sub  $s2, $s0, $s1
```

10. Convert the following C code to MIPS assembly code. [6 M]

```
void  swap( int v[], int k)
{
int temp;
temp= v[k];
v[k]= v[k+1];
v[k+1]= temp;
}
```

11. We are considering an enhancement to the processor of a web server. The new CPU is 20 times faster on search queries than the old processor. The old processor is busy with search queries 70% of the time, what is the speedup gained by integrating the enhanced CPU? [6 M]

12. How many total bits are required for a 4-way set-associative cache with 256KB of data and 16B blocks, that is, uses write-back (including the dirty bit), assuming a 32 bit address space? [6 M]

13. Explain the terms weak scaling and strong scaling. [4 M]

14. How is the number $-6\ ^{5}/_{8}$ represented in the IEEE 754 **single precision** encoding of floating point number. [6 M]

15. Write the decimal value of this 32 bit two's complement number.
11111111 11111111 11111111 11111000. [4 M]

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Year II – Semester I 2013– 2014

TEST II (Open Book)

Course No.: **CS F342** Course Title: **Computer Architecture**

Date: **08.12.13** Time: **50 Minutes** Max. Marks = **30** Weightage **(15%)**

Each question carries 5 marks.

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1. We want to compare the performance of a **single-cycle CPU design** with a **multi-cycle CPU**. Suppose we add the multiply and divide instructions. The operation times are as follows:

Instruction memory access time = 190 ps,
Register file read access time = 150 ps,
ALU delay for basic instructions = 190 ps,
Data memory access time = 190 ps
Register file write access = 150 ps
ALU delay for multiply or divide = 550 ps

Ignore the other delays in the multiplexers, control unit, sign-extension, etc. Assume the following instruction mix: 30% ALU, 15% multiply & divide, 20% load, 10% store, 15% branch, and 10% jump.

a) What is the total delay for each instruction class and the clock cycle for the single-cycle CPU design.

b) Assume we fix the clock cycle to 200 ps for a multi-cycle CPU, what is the CPI for each instruction class and the speedup over a fixed-length clock cycle?

2. Show the timing of the instruction sequence given below, for the pipeline without any forwarding but assuming a register Read and Write in the same clock cycle. Assume MIPS code is executed with predict- Not taken branch predictor.

```
        add  $1, $5, $3
label L1:  sw  $1, 0($2)
        add  $2, $2, $3
        beq  $2, $4, label L1  ;  Not taken
        add  $5, $5, $1
        sw  $1, 0($2)
```

3. For a direct – mapped cache design with 32- bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-4	3-0

a) What is the size of the cache (in words)?
b) How many entries (blocks) does the cache have?
c) What is the ratio between total bits required for such a cache implementation over the data storage bits?

Starting from power on, the following byte-addressed cache references are recorded,

Address	0	4	16	132	232	160	1024	30	140	3100	180	2180

d) How many blocks are replaced?
e) What is the hit ratio?

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TEST I

Course No.: **CS F342** Course Title: **Computer Architecture**

Date: **20.10.13** Time: **50 Minutes** Max. Marks = **30** Weightage (15%)

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1. Suppose the register $t0 contains 0x 20001400, what is the value of $t2 after the following instructions. **[4 M]**

```
        slt $t2, $t0, $t0
        bne $t2, $zero, ELSE
        j DONE
ELSE :  addi $t2, $t2, 2
DONE:   addi $t2, $t2, 4
```

2. Write the decimal representation of the following MIPS instruction and also label the individual fields of the decimal representation. **[6 M]**

```
add $t0 , $t0, $zero
lw $t1, 4 ($s3)
```

3. Using a 4-bit version divide 6 by 4, show the following details of all the steps in the form of a table. **[6 M]**

Iteration	Step	Quotient	Divisor	Remainder

4. Write any 4 differences between ARM ISA and MIPS ISA? **[2 M]**

5. Which are the registers involved in calling a procedure for holding input parameters, return values, and return address in MIPS software. **[6 M]**

6. Suppose $t0 holds i, $t1 holds a, and $t2 holds b then convert the following C code statements to MIPS assembly code. **[6 M]**

```
for ( i=0; i< 10; i++)
a += b;
```

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QUIZ II

SET A

Course No: **CS F342** Course Title **Computer Architecture**

Date: 20.10.13 Time: 20 Minutes Max. Marks = 10 Weightage(5%) **2 X 5 = 10 Marks**

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1. What are the values of all inputs for the "Registers" unit for the instruction, add $s1, $s2,$ s3

2. What decimal number does the bit pattern represent if it is a single precision floating-point number? **Use the 754 standard.**
   0X24A60004

3. A four segment pipeline implements a function and has the following delays for each segment

segment	Maximum delay
1	17 ns
2	15 ns
3	21 ns
4	14 ns

a. What is the clock cycle time that maximizes performance without allocating multiple cycles to a segment?

b. What is the total time to execute the function through all stages?

4. Name any four control signal names produced by the multiplexer in the data path of the processor.

5. Name any two schemes for resolving control hazard and two schemes for resolving data hazard.

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QUIZ I

SET A

Course No: **CS F342** Course Title **Computer Architecture**

Date: 02.10.13 Time: 20 Minutes Max. Marks = 10 Weightage (5%)

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1. What is the relationship between execution time and CPU performance? [1M]

2. ---------- of machine is an abstraction interface between the hardware and lowest level software. [1M]

3. Assume variable h is associated with register $s1 and base address of the array START is in $s2. What is the MIPS assembly code for the C assignment statement given below? [2M]

   START [5] = h + START [4]

4. Number of registers that are available in MIPS processor is ---------- and they are of size---------- bits. [1M]

5. Represent the number — 4 in two's complement form using 32 bit pattern. [1M]

6. A computer's memory is composed of 16K words of 32 bits each. How many bits are required for memory address if the smallest addressable memory unit is a word? [1M]

7. Expand the Acronyms. [1M]

   RISC

   CPI

   MIPS

   ISA

8. Consider the two processors P1 and P2 executing the same instruction set with the clock rates and CPIs as given in the following table, which processor has the higher performance. [1M]

Processor	Clock rate	CPI
P1	2 GHz	2
P2	4 GHz	2.5

9. Suppose a program spends 80% of its time in a square root routine. The new processor which has incorporated square root routine is 5 times faster on computation than the original processor. What will be the Fraction $_{\text{Enhancement}}$ and Speedup $_{\text{Enhancement}}$ for that processor? [1M]