BITS PILANI DUBAI CAMPUS
DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI
I SEMESTER 2012-2013
COMPREHENSIVE EXAMINATION

COURSE	: **CS C391**	**Digital Electronics and Computer Organization**
DURATION	: 3 HOURS	**III YEAR**
WEIGHTAGE	: 40% (80 Marks)	
Date	: 08-01-2013 FN	

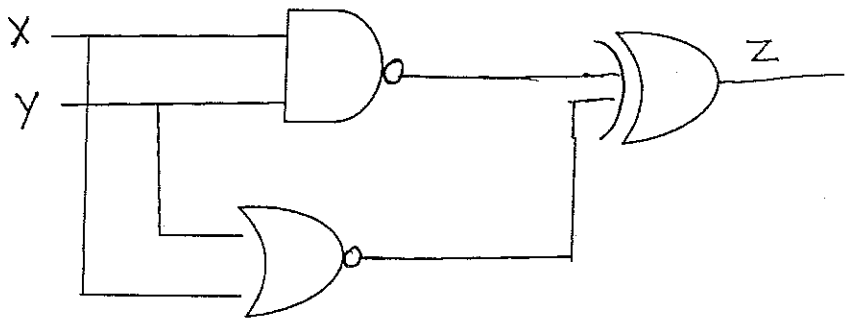
Calculators are not allowed

1a) Subtract 176 from 204. Do the work in binary using 2's complement notation.

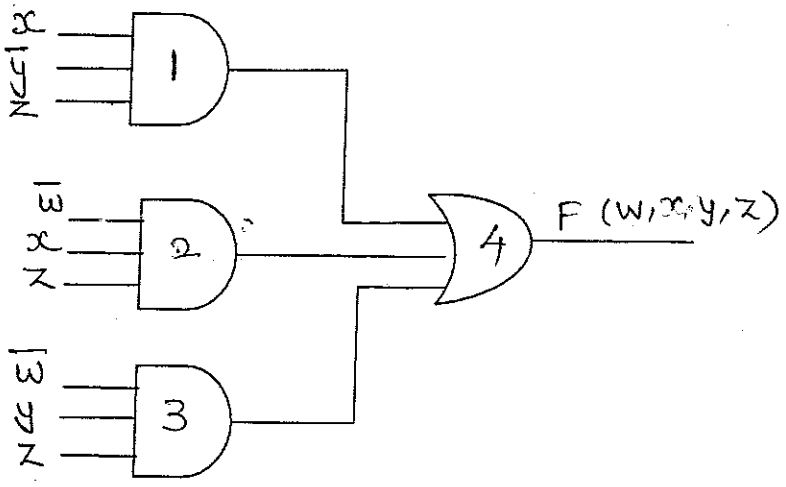
1b) Express the hexadecimal number B73D as an equivalent octal number.

1c) Give the Gray-coded equivalent of the hex number 3A7. [3+3+3] M

2a) Draw the truth table for the following logic diagram. [2+4]M



2b) In the logic circuit given below, find the redundant gate, by using K'MAP



3a) Show the circuit of a 5 X 32 decoder constructed with four 3 X 8 decoders and one 2 X 4 decoder. [4 M]

3b) Design a logic circuit for "sum" output of a full adder using only inverters and **2 X 1** MUX [5 M]

4a) A sequential circuit with two D flip-flops A and B, two inputs x and y, and one output z is specified by the following next-state and output equations. [9 M]

$A(t+1) = x'y + xB$

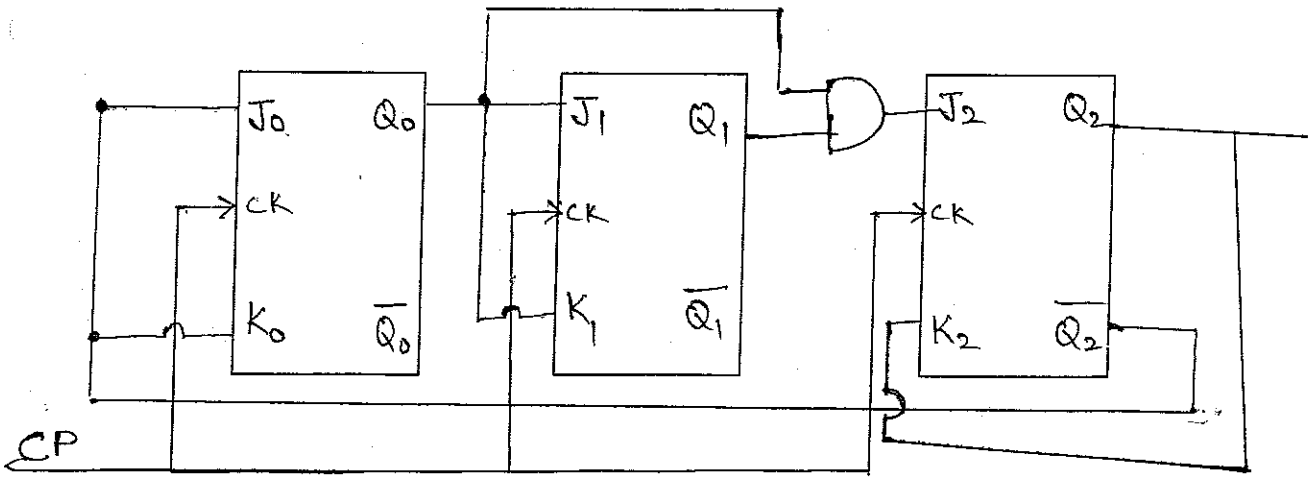
$B(t+1) = x'A + xB$

$Z = A$

a) Draw the logic diagram of the circuit.
b) List the state table for the sequential circuit.
c) Draw the corresponding state diagram.

4b) For the divide by 'n' counter circuit shown below, $J_0=K_0=\overline{Q_2}$; $J_1=K_1=Q_0$; $J_2=Q_0Q_1$; $K_2=Q_2$ write the truth table of the Q_0, Q_1 and Q_2 after each pulse and find the value of 'n'. (Assume the initial state of the counter as 000)

[5 M]



5a) Draw and explain the design of a 4 bit serial adder. And compare serial adder and parallel adder. [6 + 2 M]

5b) Assuming unused states are driven to don't care states, design a counter with D flip-flops that goes through the following binary repeated sequence: 0, 1, 3,4,6,7. what are self correcting circuits? And how will you make sure the circuit you have designed as self correcting circuit. [6 M]

6a) specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for the following combinational circuit components: [4 M]

1) A binary multiplier that multiplies two four-bit words
2) A 4 bit adder-subtractor.
3) A quadruple two to-one-line multiplexer with common select and enable inputs, and
4) A BCD-to-seven-segment decoder with an enable input.

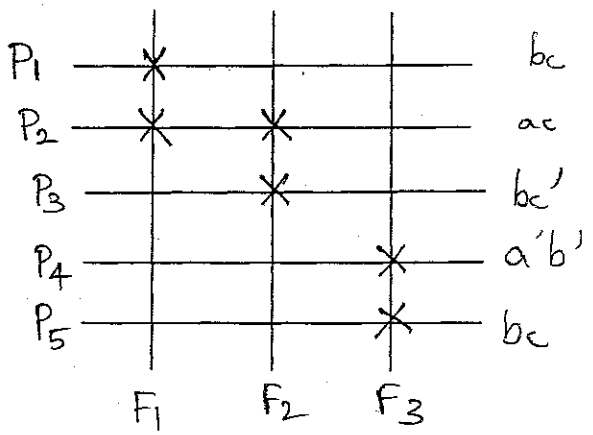
6b) It is desired to generate the following three Boolean functions: [5 M]

$F1 = ab'c + a'bc' + bc$

$F2 = ab'c + ab + a'bc'$

$F3 = a'b'c' + abc + a'c$

By using an OR gate array as shown in figure, where P_1, P_2, P_3, P_4 and P_5 are product terms in one or more of the variables a, a', b, b', c and c'. Find terms P_1, P_2, P_3, P_4 and P_5.



7a) A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are equal to 1, equal to 0 otherwise. Write a Verilog user-defined primitive for a three bit majority function. [4 M]

7b) Draw the logic diagram of the digital circuit specified by the following Verilog description: [5 M]

```
module Compre_circuit(A,B,C,D,F);
input A,B,C,D;
output F;
wire w, x, y, z, a, d;
and (x, B, C, d);
and (y, a, C);
and (w, z, B);
or (z, y, A);
or (F, x, w);
not (a, A);
not (d, D);
endmodule
```

8a) Construct Inverter, NAND gate and NOR gate with n-channel MOS logic circuit. [6 M]

8b) Perform the signed number multiplication for the data -7 X 11, using Booth's algorithm. Give the comments on each step. [4 M]

BITS PILANI DUBAI CAMPUS

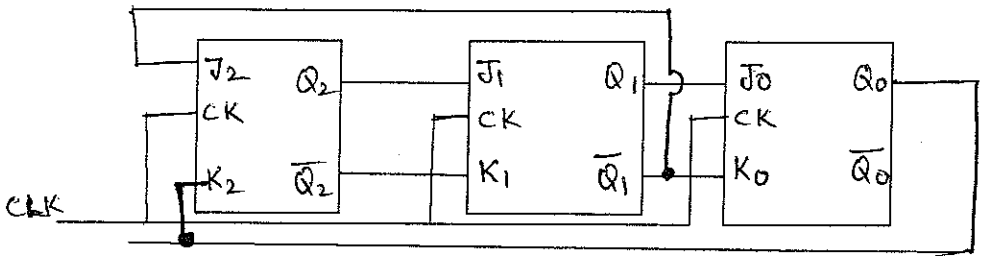
Dubai International Academic City, Dubai
Year III – Semester I 2012– 2013
Test II (Open Book)

Course No.: **CS C391** Course Title: **Digital Electronics and Computer Organization**

Date: December 13, 2012 **Time: 50 Minutes** **Max. Marks = 25**

---

1. For the modified ring counter shown, taking Q_0=0, Q_1=0 and Q2=1. Make a table of readings Q_0, Q_1, Q_2, J_2 and K_2 after each clock pulse. How many pulses are required before the system begins to operate as a divide-by N counter **[5M]**

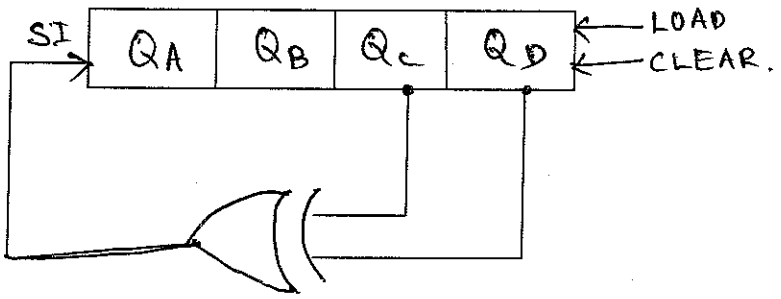


2. Implement the function

F (A, B, C, D) = $\sum$ (1,4,5,7,9,12,13) using **4 X 1** MUX. Choose

Case 1) AB as selection line and
Case 2) CD as selection line and find which design gives less hardware **[8 M]**

3. The fig. shown below is a Serial in and Parallel out 4 bit **shift right** register, which is initially loaded with 1000 show all the sequence of pattern that will be generated in this circuit. **[4 M]**



4. Design a counter using T flip flop with the following repeated binary sequence:0,1,2,3,4,5,6. And check whether the circuit is self correcting. [8 M]

ALL THE BEST

BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai
Year III – Semester I 2012– 2013
Test I (closed Book)

Course No.: **CS C391** Course Title: **Digital Electronics and Computer Organization**

Date: October 21, 2012 **Time: 50 Minutes** **Max. Marks = 25**

---

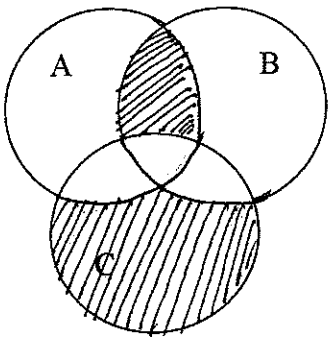
1. Draw a logic circuit which will convert the given 4 bit GRAY code into its equivalent Binary code. **[4M]**

2. In a digital circuit, output is 1 if and only if the majority of the inputs are 1. The output is zero otherwise, obtain the truth table of a 3 input majority function and implement the function obtained using only 4 NAND gates. **[4M]**

3. Design a 4 bit parallel full adder without any initial carry using only half adders and OR gates. **[4M]**

4. Implement the Boolean function f= AB +C using only 2-input NOR gates and what is the minimum number of NOR gated required. **[4M]**

5. Write the Boolean expression for the shaded area. **[4M]**



6. Formulate a weighted binary code for the decimal digits using weights 6,4,2,1. **[2M]**

7. The state of a 12- bit register is 100010010111. What is its content if it represents
   a) three decimal digits in BCD
   b) three decimal digits in excess three code
   c) a binary number. **[3M]**

ALL THE BEST

NAME:----------ID NO:----------

BITS PILANI DUBAI CAMPUS

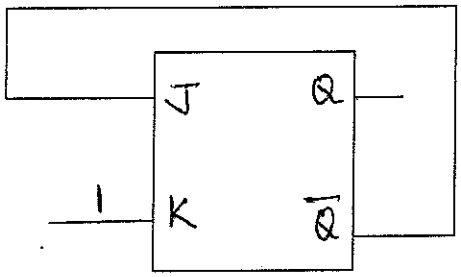
SET B

Dubai International Academic city, Dubai
Year III – Semester I 2012 – 2013
Quiz II (Closed Book)

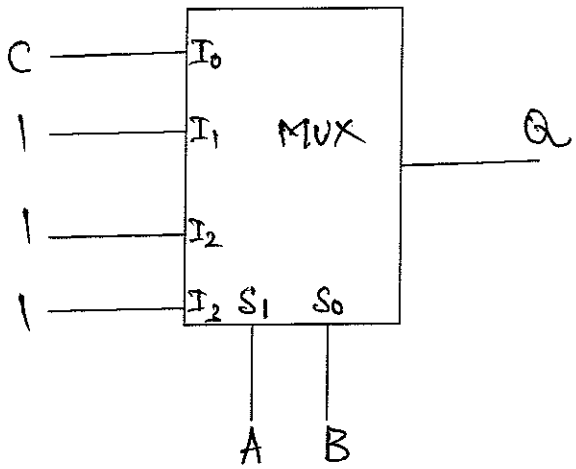
Course No: CS C391 Course Title: Digital Electronics and Computer Organization
Date: 27-11-12 Time: 20 Minutes Max. Marks = 10

---

1. Consider the following J-K flip flop, J= $\overline{Q}$ and K=1. Assume that the flip flop was initially set and then clocked for 6 pulses. What is the sequence at the output? **[3 M]**



2. Find the function F (A, B, C) implemented using the following circuit. **[3 M]**



3. Given the following state table of a Mealy model sequential circuit with one input x, one output z and four states A, B, C and D, draw the state diagram. **[2 M]**

S(t)	S(t+1), z	
	X=0	X=1
A	B,0	A,1
B	B,1	C,0
C	D,0	A,0
D	B,0	C,1

4. Construct a JK flip-flop, using D flip-flop, a 2 X 1 MUX, and an inverter. [3 M]

NAME:----------ID NO:----------

BITS PILANI DUBAI CAMPUS

SET A

Dubai International Academic city, Dubai
Year III – Semester I 2012 – 2013
Quiz I (Closed Book)

Course No: CS C391 Course Title: Digital Electronics and Computer Organization
Date: 09-10-12 Time: 20 Minutes Max. Marks = 10

---

1. Convert the gray code 101011 into its binary equivalent. **1M**

2. Minimized expression for the K-Map shown below is **2M**

CD \ AB				
	1	1	1	1
	0	0	0	0
	1	0	0	1
	1	0	0	1

3. Perform the subtraction $(9)_{10} - (4)_{10}$ in BCD using 10's complement method. **2M**

4. The output of a logic gate is '1' when all its inputs are at logic '0'. The gate is either

---------- or ---------- **1M**

5. When signed numbers are used in binary arithmetic, then ---------- notation, would have unique representation for zero. **1M**

6. Simplify following $\overline{A + AB + ABC + \overline{B}\overline{C} + \overline{C}}$ **2M**

7. Define the term fanout in IC family. **1M**