BITS Pilani, Dubai Campus

I Semester Academic Year 2011-12, Comprehensive Examination (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

Date: 7th Jan. 2012 Max. Marks: 70

Time: 3 Hours Weightage: 35%

Note: 1. Answer ALL QUESTIONS

2. Please state the assumptions, made if any, explicitly.

* * * * *

1) For each of the four (i.e., Voltage, Current, Transconductance and Transresistance) amplifier types
   a) Draw a model, with appropriate input signal source and load connected, that helps characterizing its terminal behavior [4 M]
   b) Define its Gain parameter and [4 M]
   c) State ideal values of its R_i and R_o [4 M]

2) A coupling capacitor is used to couple two amplifier stages as shown in Fig.Q2 below. Assuming the output Voltage, the output resistance of the first stage (R_2) and input resistance of second stage (R_i) are given as: v_s, 1 KΩ and 9 KΩ, respectively,
   a) Draw the resulting equivalent circuit model of this two-stage cascade [2 M]
   b) To perform its frequency response analysis, identify which (of the two types of) Single Time Constant (STC) function can be employed [1 M]
   c) Determine the smallest value for C that will ensure that the 3-dB frequency of this two stage cascade never exceeds 100 Hz [3 M]

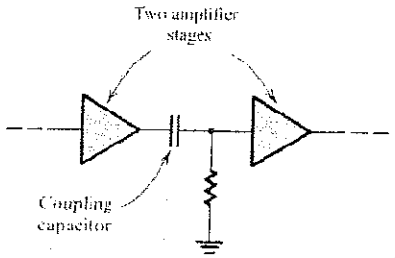


Fig.Q2

3) Employing low-frequency small-signal hybrid-π model, analyze the BJT amplifier in CE Configuration shown in Fig.Q3 below to obtain expressions for its (a) Input resistance, R_{in} (b)Open-circuit voltage gain, A_{vo} (c) Voltage gain, A_v (d)Current gain, A_i (e)Short-circuit current gain, A_{is} (f) Output Resistance, R_{out} (g) Open-circuit overall voltage gain, G_{vo} and (h) Overall Voltage gain, Gv [12 M]

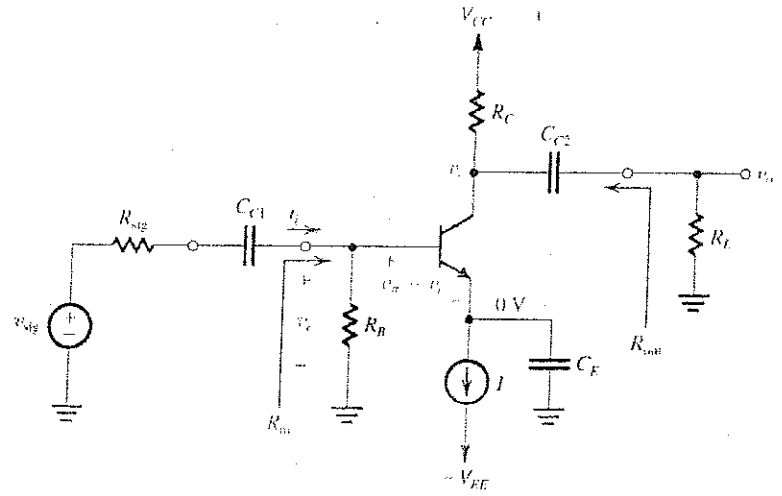


Fig.Q3

(Please Turn Over)

4) A CS amplifier, shown in Fig.Q4 below, is fed with a signal source having internal resistance R_{sig}=200KΩ. Given that the amplifier has: R_G = 10 MΩ, R_D=R_L=15 KΩ, g_m=2.5 mA/V, r_o=100 KΩ, C_{gs}=2 pF, Cgd=0.6 pF.
   a) Replacing MOSFET with its high-frequency, draw its high-frequency equivalent circuit [2 M]
   b) Express its high-frequency gain (V_o/V_{sig}), as a function of ω, in the form of an STC type function [3 M]
   c) Determine its mid-band gain A_M [2 M]
   d) Determine its upper 3-dB frequency f_H [3 M]

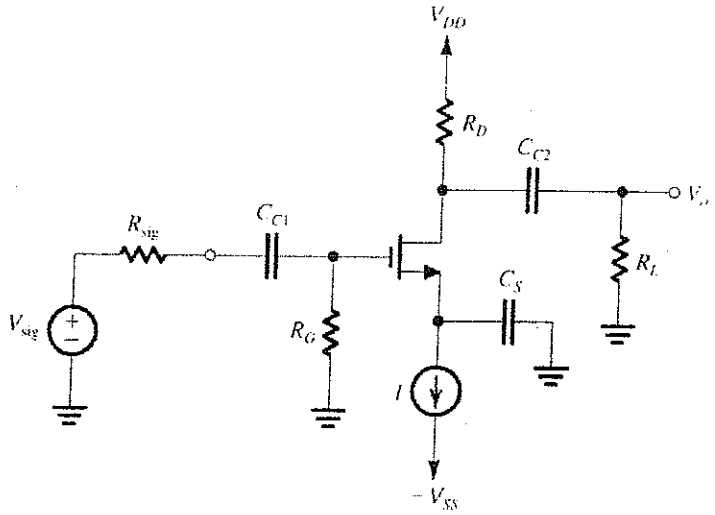
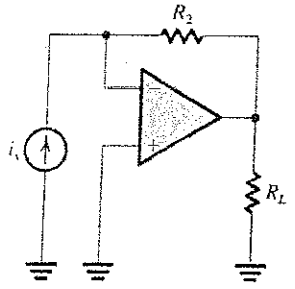
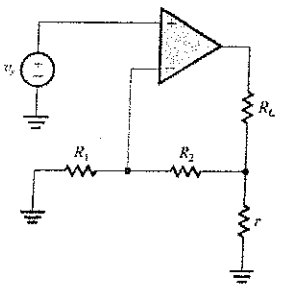


Fig. Q4

5)
   a) An amplifier with open-loop voltage gain Av = 1500 ± 150 is available. It is necessary to have an amplifier whose voltage gain varies by no more than +0.1%. Find [4 M]
      i) β of the feedback network and
      ii) the gain with feedback A_f.
   b) For each of the OPAMP circuits shown below (figures b and c) find expressions for :
      i) Identify the feedback topology, output variable being sampled and the feedback signal [3x2=6 M]
      ii) Obtain expression for the feedback factor β and [1.5x2=3 M]
      iii) Also determine the the gain with feedaback, A_f. [1.5x2=3 M]



(b)



(c)

6) Find the overall lower 3dB frequency (overall f_L) and upper 3-dB frequency (overall f_H) of 6-stage cascade if each identical stage has its f_L=10KHz and f_H=110 MHz if
   a) the stages are non-interacting [2 M]
   b) the stages are interacting [2 M]
7) Draw the transmission characteristics of a typical low-pass chebyshev filter and define all its typical specifications that need to be specified for designing the same. [4 M]
8) Write short notes on ANY TWO of the following topics: [3x2=6M]
   a) Features that distinguishes a Differential amplifiers from General Purpose amplifiers
   b) Biasing scheme in Integrated Circuits
   c) Distinct features & specifications of Tuned Amplifiers vis-à-vis General Purpose amplifers
   d) A description of the Internal Circuit Diagram of an OPAMP Chip

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BITS Pilani, Dubai Campus

I Semester Academic Year 2011-12, Test-2 (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

Date: 4th Dec. 2011 | Max. Marks: 40

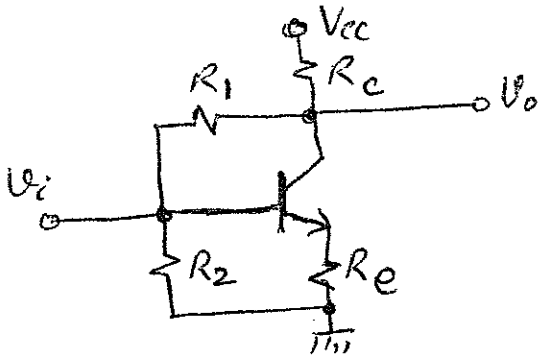
Time: 50 Minutes | Weightage: 20%

Note: 1. Answer ALL QUESTIONS

2. Please state the assumptions, made if any, explicitly.

* * * * *

1) Analyze the Circuit shown below to obtain its bias stability factor S. [8 M]

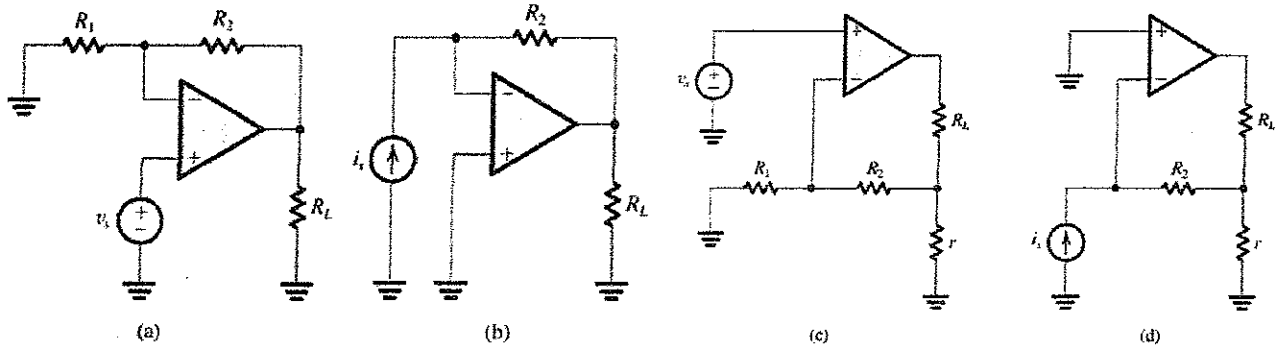


2) An amplifier with open-loop voltage gain Av = 100 ± 10 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.02%. Find [6 M]

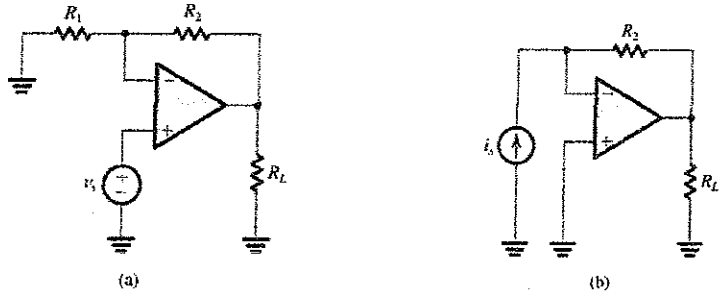
a) β of the feedback network and

b) the gain with feedback A_f.

3) For each of the OPAMP circuits shown identify the feedback topology and indicate the output variable being sampled and the feedback signal. [3x4=12 M]



4) Assuming that the OPAMP in the following circuits is modeled by an input resistance R_{id} and an open-circuit voltage gain μ and an output resistance r_o, Derive an expression for the loop gain of each of the following circuits. [3+3 =6 M]



5) Consider a feedback amplifier for which the open loop gain A(s) is given by $A(s) = \frac{1000}{\left(1+\frac{s}{10^4}\right)\left(1+\frac{s}{10^5}\right)^2}$. If the feedback factor β is independent of frequency, find the frequency at which the phase shift is 180°. [8 M]

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BITS Pilani, Dubai Campus

I Semester Academic Year 2011-12, Test-2 (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

Date: 4th Dec. 2011 | Max. Marks: 40

Time: 50 Minutes | PAGE No. 1/3 | Weightage: 20%

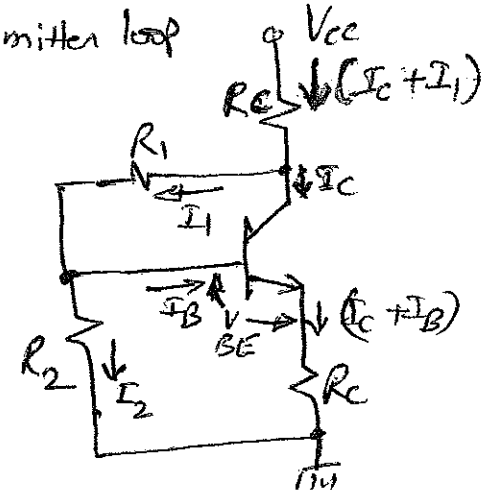
Note: 1. Answer ALL QUESTIONS

2. Please state the assumptions, made if any, explicitly.

Answering Scheme

Q. No.	Solution / Key	Marks

(1) KVL around collector-base-emitter loop gives:



$$V_{CC} = (I_C+I_1)R_C + (I_C+I_B)R_E + I_1R_1 + V_{BE}$$

$$\text{But } I_2 = \frac{V_{BE}+(I_B+I_C)R_E}{R_2}$$

and $I_1 = I_B + I_2$.

$$\text{(OR)} \quad I_1 = I_B + \frac{V_{BE}+(I_B+I_C)R_E}{R_2} = \frac{I_BR_2 + V_{BE} + (I_B+I_C)R_E}{R_2}$$

$$\therefore V_{CC} = I_CR_C + I_1R_C + I_CR_E + I_BR_E + I_1R_1 + V_{BE}$$

$$= I_CR_C + I_CR_E + \left\{\frac{I_BR_2 + V_{BE} + (I_B+I_C)R_E}{R_2}\right\}R_C$$

$$+ I_BR_E + V_{BE} + \left\{\frac{I_BR_2 + V_{BE} + (I_B+I_C)R_E}{R_2}\right\}R_1$$

$$= I_C\left[R_C + R_E + \frac{R_E(R_1+R_C)}{R_2}\right] + I_B\left[R_E + \frac{R_ER_1 + R_2R_1 + R_CR_E + R_CR_2}{R_2}\right]$$

$$+ V_{BE}\left(1 + \frac{R_1+R_C}{R_2}\right)$$

$$\therefore V_{CC} = I_C\left\{R_C + R_E + \frac{R_E(R_1+R_C)}{R_2}\right\} + I_B\left\{R_E + \frac{(R_E+R_2)(R_1+R_C)}{R_2}\right\}$$

$$+ \left[1 + \frac{R_1+R_E}{R_2}\right]V_{BE}.$$

Since $I_C = \beta I_B + (1+\beta)I_{CO}$, $I_B = \frac{I_C - (1+\beta)I_{CO}}{\beta}$.

Contd ... (2)

BITS Pilani, Dubai Campus

I Semester Academic Year 2011-12, Test-1 (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

Date: 9th Oct. 2011 Max. Marks: 50

Time: 50 Minutes Weightage: 25%

Note: 1. Answer ALL QUESTIONS

2. Please state the assumptions, made if any, explicitly.

* * * * *

1)

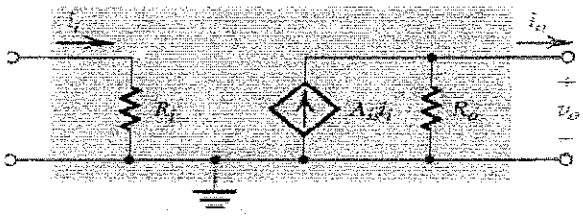
a) Find the voltage, current and power gains (Av, Ai, and Ap, respectively) both as ratios and in dB if rms values measured in an amplifier load combination is: v_i=100 mV; i_i=100mA; v_O=10V; R_L=100 Ω. [1x6=6 M]

b) An amplifier operating from a single 15-V supply provides a 12-V peak-to-peak sine-wave signal to a 1-kΩ load and draws negligible input current from the signal source. The dc current drawn from the 15-V supply is 8 mA. What is the power dissipated in the amplifier and what is the amplifier efficiency? [2x2=4M]

2)

a) Explain what is Amplifier Saturation using a neat sketch of its transfer characteristics. Indicate how it can be avoided while designing an Amplifier. Also define the term "maximum signal handling capacity" of an amplifier. [1.5+2+1.5=5M]

b) Identify the type of amplifier whose model is shown in the figure below. If it is fed with a signal current-source is having a resistance R_s and its output be connected to a load resistance R_L, derive an expression for its overall current gain. [1+4=5M]



3) A Transconductance amplifier with R_i=5kΩ, R_o=50KΩ and G_m=10mA/V is connected to a load of a resistance R_L in parallel with a capacitance C_L.

a) Prove that the voltage transfer function realized, V_o/V_i, is of Low-pass Single Time Constant type. [2 M]

b) Determine the lowest value that R_L can have while a dc gain of at least 40-dB is obtained? [4 M]

c) With the value of R_L (as in b above) connected, find the highest value that C_L can have while a 3-dB bandwidth of at least 100 kHz is obtained. [4 M]

4)

a) Draw the circuit of a BJT Amplifier in CE Configuration employing single power supply. Deduce its ac equivalent circuit employing hybrid-π model and List all the assumptions used in deducing it. [2+3+2=7M]

b) A BJT having β=150 is biased at a dc collector current of 2 mA. Find the model parameters: g_m, r_e, r_π at this bias point. [1+1+1=3M]

5)

a) List the steps to analyze Amplifier Circuits to find its characteristic parameters using Small-Signal Equivalent circuits. [5 M]

b) A BJT Common Emitter Amplifier with R_C=5 kΩ is connected between a source with R_s=0.5 kΩ, and a load of R_L=10 kΩ. Assuming that the parameters of the BJT model are: r_n=2 kΩ, g_m=20mA/V, r_0=75 kΩ,

i) Derive an expression for the overall voltage gain [2 M]

ii) Find the magnitude of the overall voltage gain [1 M]

iii) Recalculate the magnitude of overall voltage gain neglecting r_o [1 M]

iv) Find the short circuit current gain [1 M]

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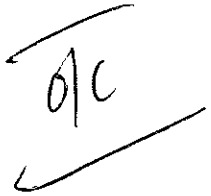

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BITS Pilani, Dubai Campus

I Semester Academic Year 2011-12, QUIZ-2 (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

A

Date: 23rd Nov. 2011 Max. Marks: 14

Time: 20 Minutes Weightage: 7%

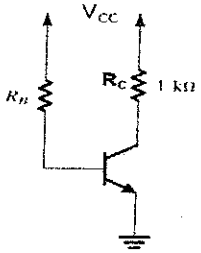
Note: 1. Answer ALL QUESTIONS while stating explicitly the assumptions made, if any.
2. Read the questions carefully and reply with most appropriate answers for a question.

* * * * *

1) In a BJT Amplifier Collector Current, I_C varies with temperature because, with temperature following three parameters of a BJT also vary: [3 M]

a) _____ b) _____ c) _____

2) For the BJT Fixed bias circuit shown, derive an expression for the Stability factor S, in the space given below[2 M]



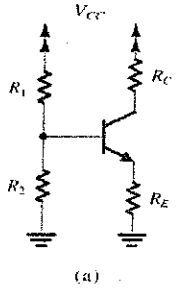
Derivation for S:-

3) In a BJT Self Bias circuit shown, if R_1=18KΩ, R_2=22KΩ, V_{CC}=12V, R_C=1KΩ, R_E=1.2KΩ and assuming BJT's β=149,

a) Estimate S (approximate)

b) Which inequality leads us to arrive at the "S(approx.)" expression from its exact expression?

c) In this circuit, verify and state whether the inequality (as in b, above) is satisfied or not. [3 M]



(a)

a)Computing approximate S:

b) Inequality is:_____

c) Verification of the inequality:

4) Draw BJT's High Frequency hybrid-π model. State physical significance of each of the 3 extra circuit elements of this model, which do not appear in the BJT's low frequency (hybrid-π) model. [2+3 M]

BJT's High Frequency Model:

3 extra circuit elements' Physical Significance is:

1._____

_____.

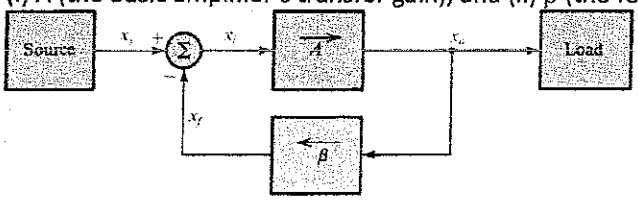
2._____

_____.

3._____

_____.

5) For the Feedback Amplifier shown below, derive an expression for A_f (transfer gain with feedback), in terms of (i) A (the basic amplifier's transfer gain), and (ii) β (the feedback factor). Derivation: [1 M]



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ID No._____; Name:_____

BITS Pilani, Dubai Campus

I Semester Academic Year 2011-12, QUIZ-2 (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

B

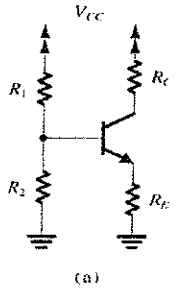
Date: 23rd Nov. 2011 Max. Marks: 14

Time: 20 Minutes Weightage: 7%

Note: 1. Answer ALL QUESTIONS while stating explicitly the assumptions made, if any.
2. Read the questions carefully and reply with most appropriate answers for a question.

* * * * *

1) In a BJT Self Bias circuit shown, if R_1=27KΩ, R_2=33KΩ, V_{CC}=15V, R_C=2KΩ, R_E=1.5KΩ and assuming BJT's β=149,
   a) Estimate S (approximate)
   b) Which inequality leads us to arrive at the "S(approx.)" expression from its exact expression?
   c) In this circuit, verify and state whether the inequality (as in b, above) is satisfied or not. [3 M]



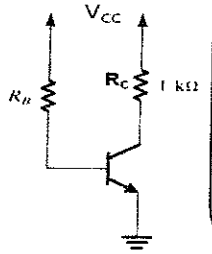
(a)

a)Computing approximate S:

b) Inequality is:_____

c) Verification of the inequality:

2) For the BJT Fixed bias circuit shown, derive an expression for the Stability factor S, in the space given below[2 M]



Derivation for S:-

3) In a BJT Amplifier Collector Current, I_C varies with temperature b'coz with temperature 3 BJT parameters vary as in table below (please fill in the table both parameter symbol & the by how much will it vary with temp) [3 M]

Parameter 1	Rate, by which varies	Parameter 2	Rate, by which varies	Parameter 3	Varies as below

4) In an MOSFET, Source is shorted to its Body (substrate). Draw the MOSFET's High Frequency hybrid-π model ignoring the drain depletion. State physical significance of the 2 extra circuit elements (this model has), which do not appear in MOSFET's low frequency (hybrid-π) model. [2+2 M]

BJT's High Frequency Model:

3 extra circuit elements' Physical Significance is:

1._____

_____.

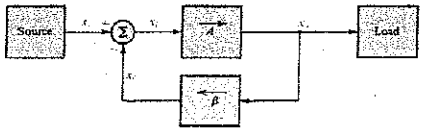
2._____

_____.

3._____

_____.

5) Shown below is a block diagram of a Feedback Amplifier. Derive an exact expression for A_f (transfer gain with feedback) in terms of A & b. State the assumption and prove that under the assumption, A_f is solely a function of feedback block.



Derivation for exact A_f: Proof [1+1 M]

Assumption: _____

Proof:

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A

I Semester Academic Year 2011-12, QUIZ-1 (Closed Book)

EEE C424/ECE C313/INSTR C313 Microelectronic Circuits

Date: 26th Oct. 2011 Max. Marks: 16

Time: 20 Minutes Weightage: 8%

Note: 1. Answer ALL QUESTIONS

2. Please state the assumptions, made if any, explicitly.

* * * * *

1) h-parameters that can be obtained from BJT's Input characteristics are: _____ and _____ [2 M]

2) Draw CCCS version of hybrid-π model of a BJT in the space provide below and indicate expressions to obtain model parameters if ONLY the values α, I_C and V_A of the given BJT are available you. [1+1.5=2.5M]

3) High Frequency side of an amplifier behaves like a _____ type Single Time Constant Circuit. [1 M]

4) BJT CE Amplifier's current gain can be expressed in terms of h-parameters as =_____approximately. [1 M]

5) Describe how to obtain h_{ie} from the characteristics of a BJT [1.5 M]

6) Draw the Circuit of a CC Amplifier employing dual power supply and deduce its Equivalent Circuit employing a real BJT's CCCS version of T-model. [1+1=2M]

7) Draw the Large-signal equivalent circuit model of an N-channel MOSFET in the space provided below[1 M]

8) The output voltage of a voltage amplifier has been found to decrease by 20% when a load resistance of 1 KΩ is connected. Value of the amplifier output resistance is _____ ohms. [1 M]

9) Three amplifiers having a voltage gain of 0dB, 100 dB and 5dB are connected in a Cascade. The overall voltage gain of this 3-stage Cascaded amplifier is _____ when expressed as a ratio. [1 M]

10) An amplifier is modeled as an high-pass Single Time constant Circuit with R = 10KΩ and C=25 pF. Its cut-off frequency is _____ and it is _____ 3-dB frequency of this amplifier. [1.5 M]

11) Among a FET and a BJT which one is more immune to noise and justify your answer?
_____ is more immune to noise and it is so because: _____
_____. [1.5 M]

12) A transistor amplifier is fed with a signal source having an open circuit voltage v_{sig} of 10mV and an internal resistance R_{sig} of 100 kΩ. The Voltage v_i at the amplifier input and output voltage v_o are measured both without and with a load resistance R_L=10KΩ connected to the amplifier output. The measured results are as follows. This amplifier's G_{vo} is _____. [1 M]

	V_i(mV)	V_o(mV)
Without R_L	9	90
With R_L connected	7	60

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