BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai
Year III – Semester I 2011– 2012
COMPREHENSIVE EXAMINATION (Closed Book)

Course No.: **CS / INSTR/ EEE / ECE C 391** Course Title: **DECO**

Date: 09th January, 2012 Time: 3 hrs Max. Marks = 80

Clearly indicate the assumptions made if any
All questions carry equal Marks

1. a. Write all signed integer numbers(Let it be x) that can be represented using three binary bits, assuming that 2's complement is used for representing negative numbers. Tabulate the signed decimal values and its equivalent three bit-binary representation $(a_2,a_1,a_0)_2$

   b. Tabulate the function $f(x) = x^2 - 1$ in binary for the values of x which is explained in question No. 1 (a). What is the range of values of f(x)? How many bits do you need to represent the function f(x)? (Assume two's complement for representing negative numbers)

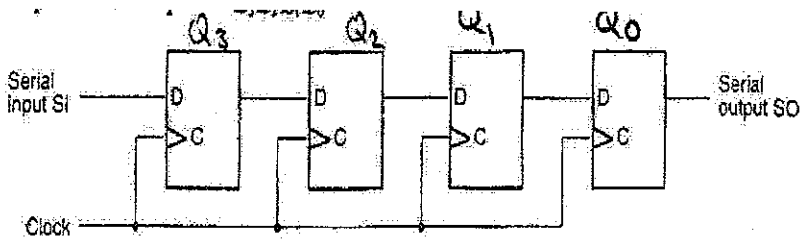
2. a. Given F (w, x, y, z) = Σ (0,2,3,5,6,7,8) and the don't care terms d (w, x, y, z) = 10,11,12,13,14 & 15
   Using K-Map,
   a) Identify the Prime Implicants
   b) Identify the Essential Prime Implicants
   c) Find the reduced expression in the SOP form
   d) Implement the function using NAND gates alone

   b. Using only **one 3 X 8 active low decoder and 3 AND gates** realize the following functions
   F(A,B,C) = A(B+C) + A'B'
   G(A,B,C) = ∑ (0,1,4,5,7)
   H(A,B,C) = ABC + A'B'

3. a. List the PLA programming table for the full adder circuit. Optimize the no. of product terms for true or complimentary outputs.

   b. Draw and explain the logic diagram of a 4 x 1 multiplexer with active low enable pin. Also write the function table of the device.

4. a. The digital logic circuit below represents a 4 bit shift register. Indicate how to load binary 6 into the register. Draw the waveforms of the clock input, all the affected inputs and outputs (Q_3 MSB and Q_0 LSB)



b. A sequential circuit has two T flip flops A and B, two inputs x and y and one output z. The flip flop input equations are given as $T_A = B\,x$; $T_B = A + xy'$; $z = A'\,xy$;
   a) Draw the circuit diagram
   b) Write the State table
   c) Draw the state diagram

5. Using a positive edge triggered MN flip flop whose characteristics table is given below, derive the excitation table of the flip flop. Also design a synchronous mod-5 counter using the MN flip flop to count in the sequence 6,4,3,2,1 repeatedly. (10M)

M	N	Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q(t)′
1	1	1

6. Answer any two of the following three questions
   a. Write short notes on I/O data transfer schemes
   b. Clearly explain the Booth's algorithm used for signed number multiplication using 12 and -7 as example.
   c. With a neat circuit diagram, explain the function of an universal 4-bit shift register

7. a. With a neat circuit diagram, Explain the principle of operation of a TTL NAND gate with Totem-Pole output

   b. The specification of a 7400 IC is given below. For the specifications, find the Fan-out, Power Dissipation, Propagation Delay and Noise Margin of the IC.
   $t_{PHL} = 3ns$; $t_{PLH} = 4$ ns; $V_{cc} = 5$ V; $I_{ccH} = 10$ mA; $I_{ccL} = 20$ mA;
   $I_{oH} = 1mA$; $I_{oL} = 20$ mA; $I_{IL} = 2mA$; $I_{IH} = 0.05mA$;
   $V_{oH} = 2.7V$; $V_{oL} = 0.5V$; $V_{IH} = 2V$; $V_{IL} = 0.8V$

8. a. Write an HDL behavioral description module of a 4-bit arithmetic logic unit (ALU). The circuit performs two arithmetic and two logic operations that are selected by a 2-bit input. The four operations are **add, subtract, AND** and **OR**.

   b. Write a stimulus for the above module and show the result of the HDL program.

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International Academic City, Dubai

Year III – Semester I 2011– 2012

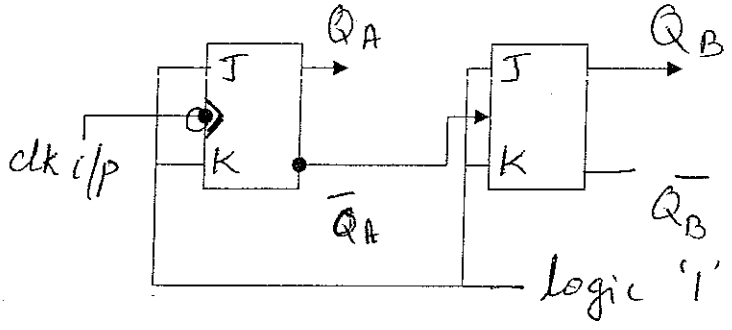
TEST II (OPEN BOOK)

Course No.: CS / EEE / ECE / INSTR C 391 **Course Title: DECO**

Date: December 11, 2011 Time: 50 min Max. Marks = 25

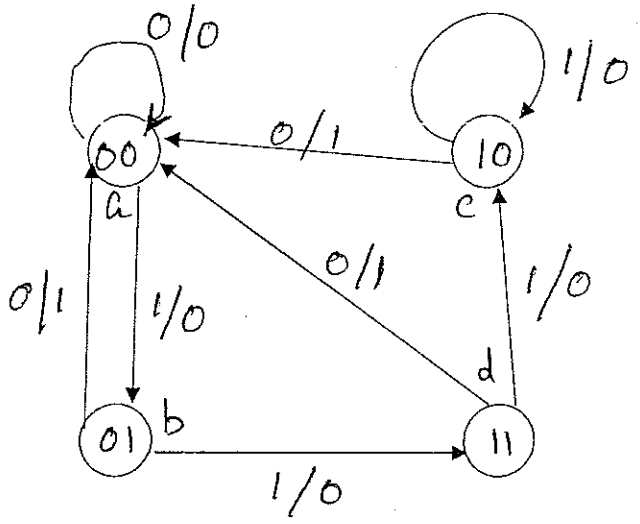
Clearly indicate the assumptions made if any

1. For the ripple counter shown in figure below, draw the complete timing diagram for eight clock pulses showing the clock inputs, Q_A and Q_B waveforms. Assume that Q_A and Q_B are initially cleared to zero.



(1 + 2 + 2)

2. Starting from the state 00, in the following state diagram, determine the state transitions and output sequence that will be generated when an input sequence of 01001110011010 is applied (6)



3. Design a synchronous binary counter to count the sequence 1, 3, 4, 5, 6 repeatedly using JK flip flop.(8)

4. Implement the following two Boolean functions with a PLA using minimum number of product terms. Also write the PLA programming table. (6)

$F_1(A,B,C) = \Sigma\ (0,2,3,6)$ $F_2(A,B,C) = \Sigma\ (1,2,6,7)$

**********GOOD LUCK**********

BITS PILANI DUBAI CAMPUS

DIAC, Dubai
Year III – Semester I, 2011 – 2012
Test1 (Closed Book)

Course No.: **CS C391/INSTR C391** Course Title: **DECO**

Date: October 16, 2011 Time: 50min Max. Marks = 25

Calculators are not allowed. State clearly the assumptions made if any.
Assume all logics using positive logic.

1. a) Given the following equation, determine the base x that permits the equation to be true. $(42)_x + (19)_x = (60)_x$

   b) Assuming the two input AND gate delay is T seconds, write a formula for the optimum gate delay of an N (may be odd / even) input AND gate implemented using 2-input AND gates. What would be the worst case delay of the circuit?

   c) What range of decimal values can be represented by a three-digit hexadecimal number?

   (1+3+2)

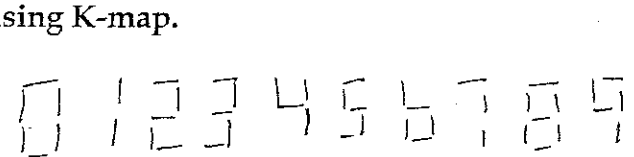
2. a) Reduce the Boolean function F(X,Y,Z) = XZ + Y'Z + Z' using Boolean laws.
   b) Draw the Multi level NOR realization for the expression F = W (X + Y + Z) + XYZ

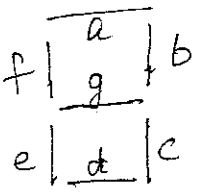
   (1.5 + 2.5)

3. What is a full adder? Write the truth table of a full adder. Design a Full adder circuit using an active low 3x8 decoder and two input AND gates. Draw the logic diagram. (Use Block diagram representation for the decoder) (5)

4) A BCD code is being transmitted to a remote receiver. The bits are $A_3A_2A_1A_0$ with A_3 being the MSB. The receiver circuit includes a BCD error detector circuit that examines the received code to see if it is a **valid BCD code**. Design a logic circuit to produce a **LOW output** for any error condition. (3)

5. a) The display pattern for a BCD to seven segment decoder is given below. Write the truth table for the decoder circuit. Also find the reduced Boolean expression for the segment **"b" using K-map.**





   b) What would be the output for segment "b" if the input to this decoder is "1111"? If you want the seven segment display corresponding to this input to be 'F', what modification should be done on the design for the segment "b"? (4 + 3)

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Name :

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SET A

BITS PILANI, DUBAI CAMPUS

International Academic City, Dubai

Year III – Semester I 2011– 2012

Quiz II

Course No.: ECE / EEE / CS / INSTR C 391 **Course Title: DECO**

Date: November 30, 2011 Time: 20 min Max. Marks = 10

Clearly indicate the assumptions made if any

1. In a Johnson's ring counter, the MSB of the register is A and LSB is D. If the data is shifted right (A → D) continuously, what would be the hexadecimal count sequence of the shift register for the clock inputs (2M)

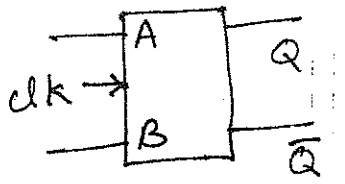
0000
1000
1100
1110
1111
0111
0011
0001

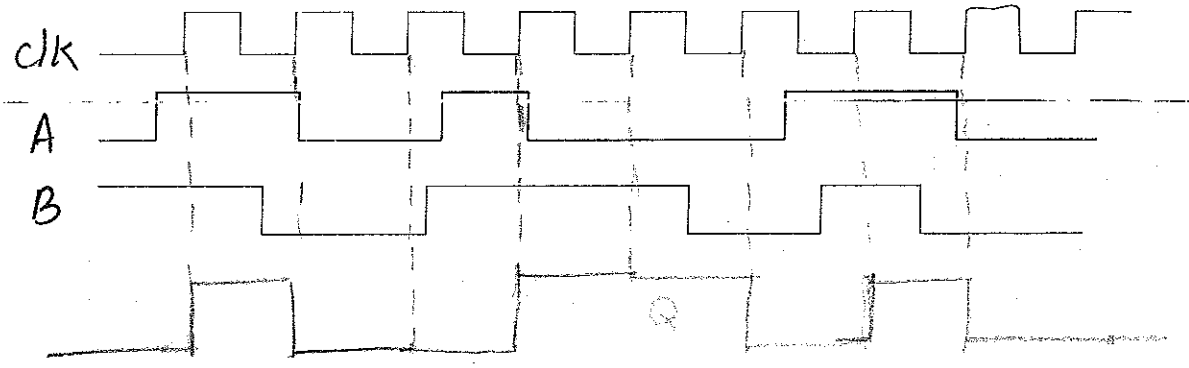
0, 8, 12, 14, 15, 7, 3, 1, 0

0, 8, C, E, F, 7, 3, 1, 0.

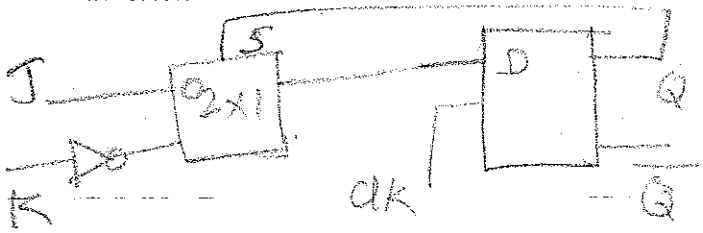
2. The Characteristic table of a positive edge triggered **AB** flip flop is given below. Draw the wave form of the output Q(t+1) for the inputs A and B as shown below. (2M)

i/p A	i/p B	o/p Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q'(t)
1	1	1



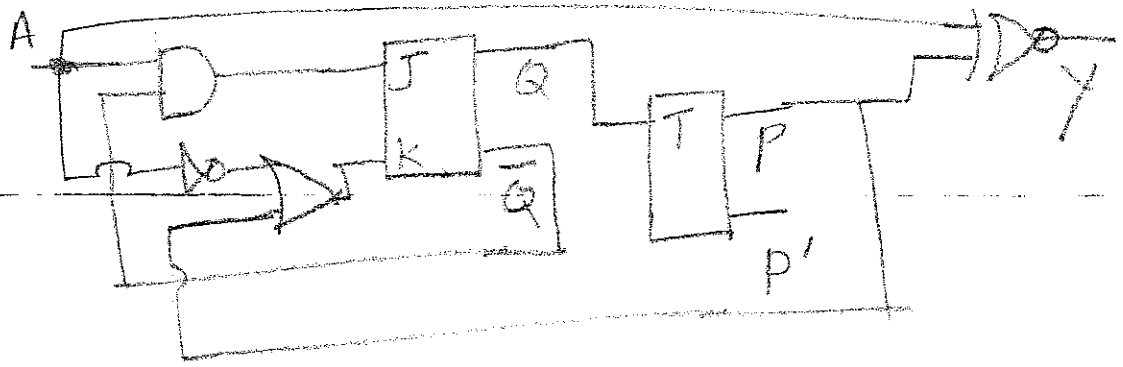


3. Construct a JK Flip-flop, using a D Flip-flop, a two-to-one- Multiplexer and an Inverter. (2M)



4. In a sequential circuit there is one JK flip flop whose output is denoted as Q and one T flip flop whose output is denoted as P, one input 'A' and one output 'Y'. The input and output equations of the flip flop are given as below. Draw the sequential circuit. (2M)

J = A Q' ; K = A' + P ; T = Q ; Y = A ⊕ P' ;



5. In question No.4, if the **present state (Q,P) is (1,0)** and the input **A is applied as '0'**, what would be the **next state and the output of the circuit.** (2M)

$J = 0$ $Q(t+1) = 0$ $Q(t) = T = 1$

$K = 1$ $P(t) = 0$; $P(t+1) = 1$

(0,1) $Y = 0$

********** GOOD LUCK **********

Name :

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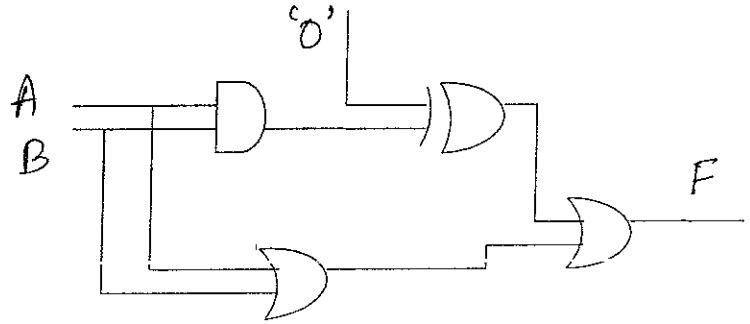
BITS PILANI DUBAI CAMPUS
DIAC, Dubai
Year III – Semester I 2011 – 2012
Quiz 1 (Closed Book)

SET B

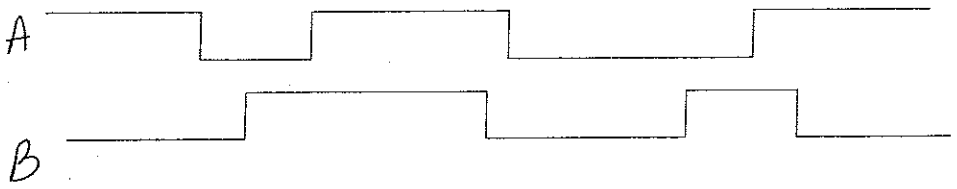
Course No.: **CS / INSTR C391** Course Title: **DECO**

Date: NOVEMBER 2nd, 2011 Time: 20 Minutes Max. Marks = 10

1. Write the Boolean expression for the output '**Y**' of the circuit shown in figure below.



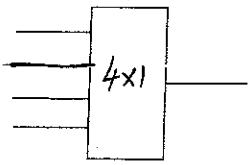
If the inputs A & B are as shown in the waveform below, Draw the output wave form for F.



2. Represent the following Boolean expression in the Sum of minterm and Product of maxterm forms.

   S (A,B,C) = AB + C

3. Implement the function **F = A'BC' + AB'C** using single 4-to-1 multiplexor



4. Implement a half adder using one 2x4 active high decoder and basic logic gates

5. For the following truth table write POS (product of sums) expression for F

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0