BITS-Pilani Dubai, Dubai International Academic City, Dubai

FIRST SEMESTER 2009 – 2010

III Yr. B.E.(Hons.), COMPREHENSIVE EXAMINATION (Closed Book)

Course Code : **EEE C424 / INSTR C313** Date: **28.12.09**

Course Title : **Microelectronic Circuits** Max Marks: **80**

Duration : **3 Hrs** Weightage: **40%**

NOTE: 1. Answer ALL questions.

2. Make assumptions, if any, but explicitly indicate the assumptions made

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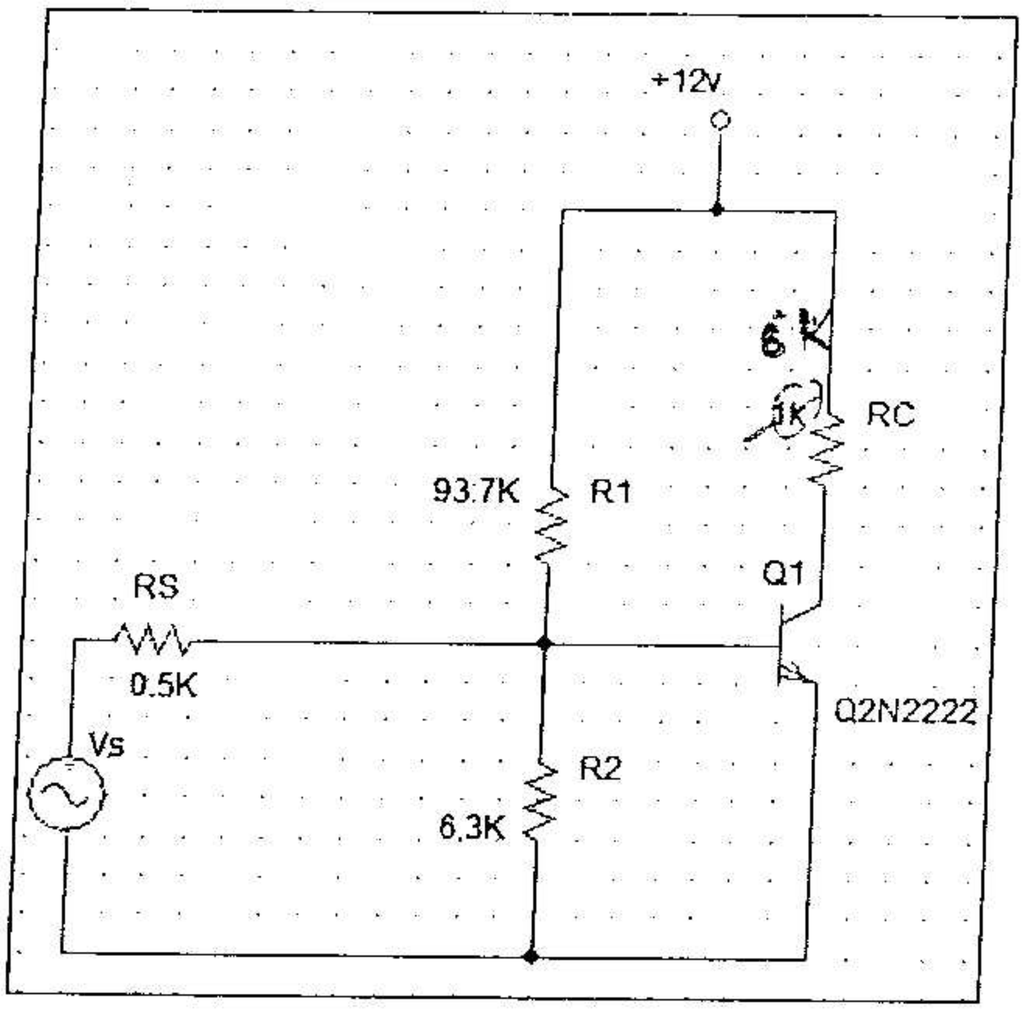
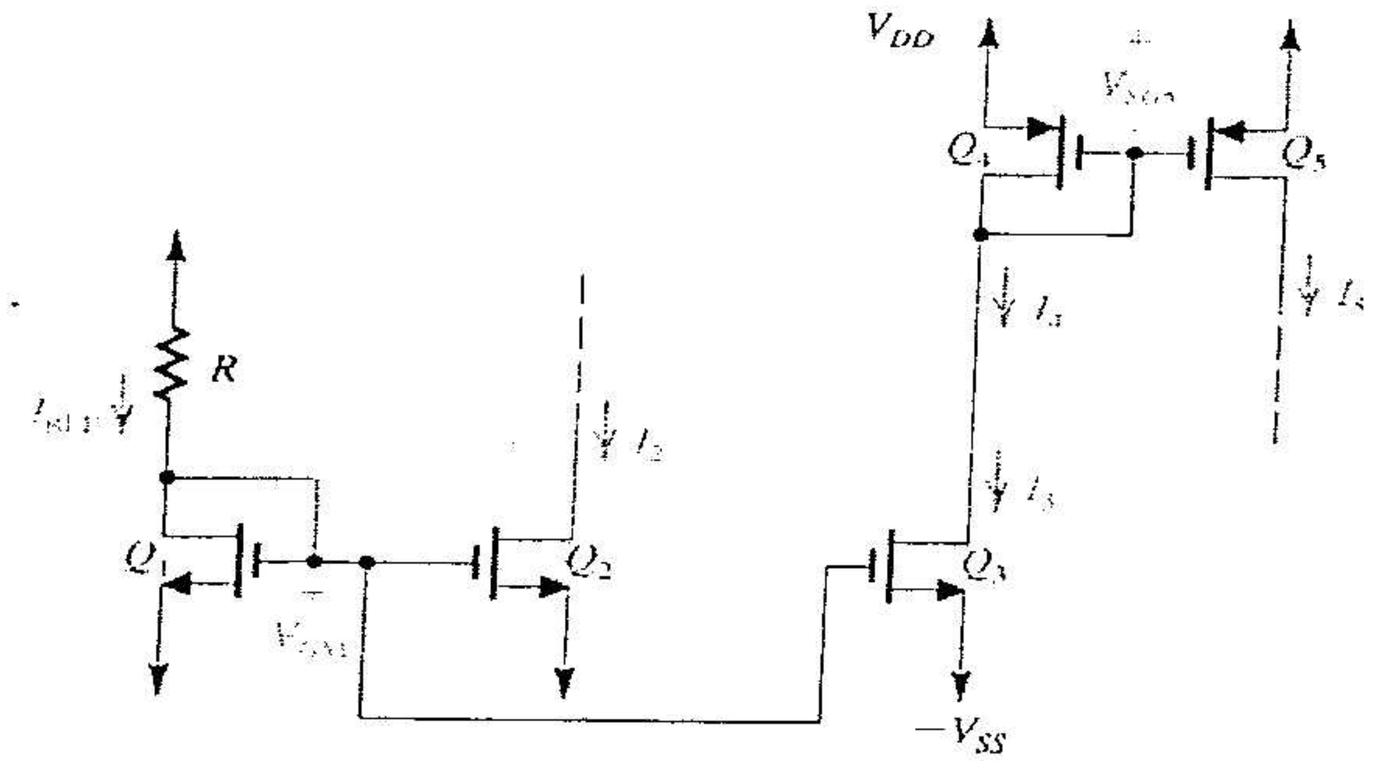
1) Draw high frequency model of MOSFET. Draw the circuit diagram of Common Source amplifier circuit and obtain the expression for higher cutoff frequency using its equivalent circuit. **(2+2+4=8)**

2) Draw small signal equivalent circuit of the Common Emitter amplifier circuit shown below and find the voltage gain, A_M, input resistance, R_{in}, output resistance, R_{our}. Given that: β=100; V_{BE}=0.7 V; V_{CE}=6.31 V and V_A=100 V **(2+3+2+2=9)**

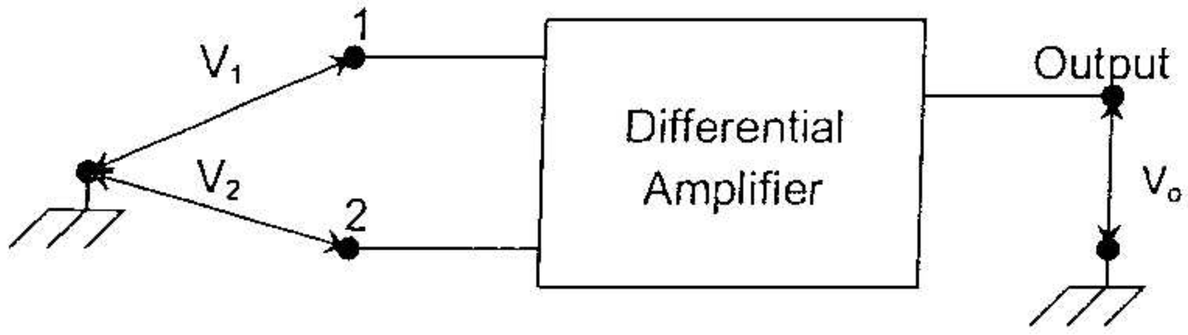


3) From the circuit given below: identify & redraw (a) current mirror circuit and (b) current steering circuit. (c) also Derive an expression for I_5 current in terms of I ref.the operation of the following circuit **(1+1+3=5)**



4)

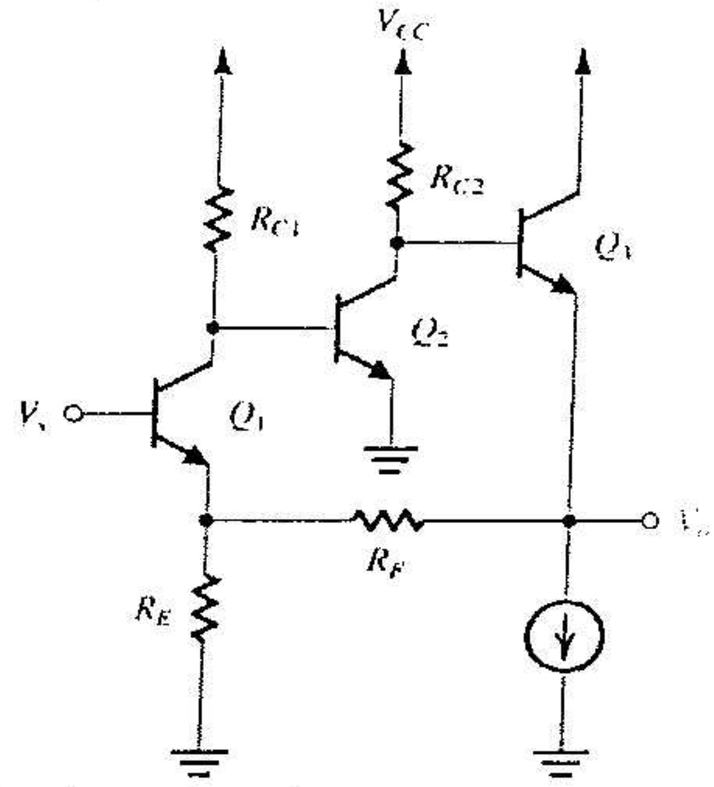
a) Obtain an expression for the output voltage of the following differential amplifier in terms of CMRR (ρ), Common-mode voltage (V_c) and the Differential voltage (V_d) **(5)**



b) Define CMRR of differential amplifier. Write the parameters affecting CMRR. Obtain the expression for CMRR due to changes in transconductance g_m of MOSFET. **(2+1+3=6)**

5)

a) Consider the Feedback amplifier circuit shown below:



i) Identify type of feedback employed **(1)**

ii) Sketch the A(s) circuit to enable determination of feedback factor β. **(1)**

iii) Show that if $A\beta$ is larger than the closed loop gain is given approximately by $A_f=\frac{V_o}{V_s}=\frac{(R_F+R_E)}{R_E}$ **(2)**

iv) If R_E is selected equal to 50Ω, find R_F that will result in a closed loop gain of 25 V/V. **(2)**

v) If Q_1, Q_2, Q_3 are biased at 1 mA, 2 mA and 5 mA, respectively, find the approximate value of R_{C1} and R_{C2} that provides a voltage gains of -10 & -50, respectively at Q_1 & Q_2 stages. Given that the transistors have h_{fe}=100. **(1+1=2)**

b) A series-series feedback amplifier employs a basic amplifier with input and output resistances each of 1kΩ and gain A=2000 V/V. The feedback factor β=0.1 V/V. Find

i) the gain, A_f; **(1)**

ii) the input resistance, R_{if}; and **(1)**

iii) the output resistance, R_{of} **(2)**

6)

a) Draw LC band pass filter in T section and π-section. **(2+2=4)**

b) Design a band pass RC active filter with midband voltage gain of 30, center frequency of 200 Hz, and Q=5. Hint : Choose $C_1=C_2=0.1\mu F$. **(5)**

c) Define Skirt frequency of a tuned amplifier. Draw the circuit and explain the operation of a stagger-tuned amplifier. **(2+2+2=6)**

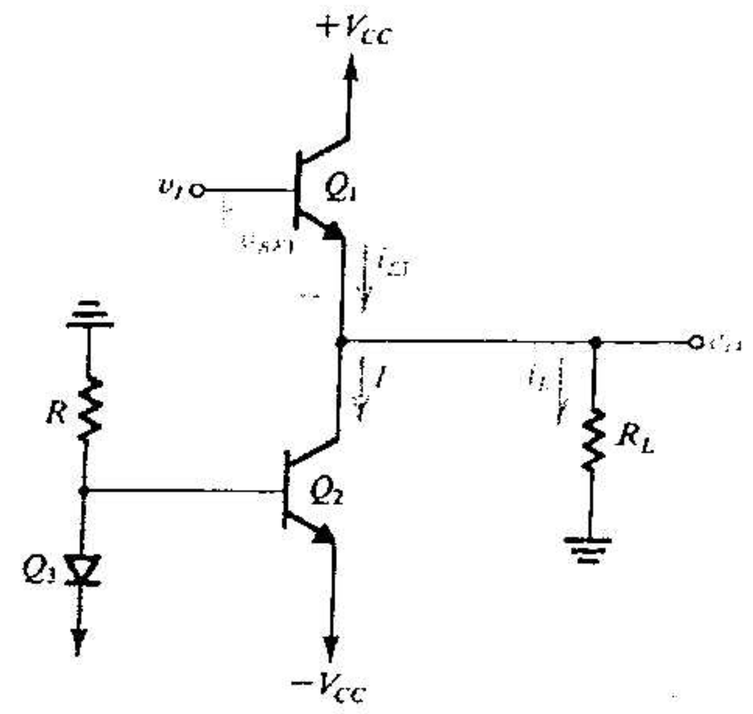
7)

a) In a Class B push-pull output stage / power amplifier,

i) By drawing the circuit, prove, from fundamentals, that theoretical maximum conversion efficiency that can be obtained is 78.5%. **(2+4=6)**

ii) What is crossover distortion w.r.t. Class B operation of power amplifiers & indicate its source **(2+1=3)**

b) For the power amplifier shown in figure below, $V_{CC}=15V$, $V_{CE,Sat.}=0.2$ V, $V_{BE}=0.7$ V and constant, and β is very high. Find (i) the values of R that will establish a bias current sufficiently large to allow the largest possible output signal swing across $R_L=1K\Omega$. Also determine (ii) the resulting output swing and (iii) minimum and maximum emitter currents. **(2+2+2=6 M)**



8) Write Short Notes on any <u>TWO</u> of the following topics: **(2.5x 2=5)**

a) Transistor pairs: Draw each of the Cascode, Darlington and Totem-pole configurations & write any two important features of each.

b) Stability analysis of Amplifiers employing root-locus technique

c) Dominant pole frequency compensation technique

d) PSPICE as an Electronic Design Automation (EDA) tool

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FIRST SEMESTER 2009 – 2010

Test-II [Open Book]

III Yr. B.E.(Hons.)

Course Code: **EEE C424 / INSTR C313** Date: 2**0.12.09**
Course Title: **Microelectronic Circuits** Max Marks: **40**
Duration: **50 minutes** Weightage: **20%**

NOTE: 1.ANSWER All the questions.
2. Make assumptions, if any, but explicitly indicate the assumptions made

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1)

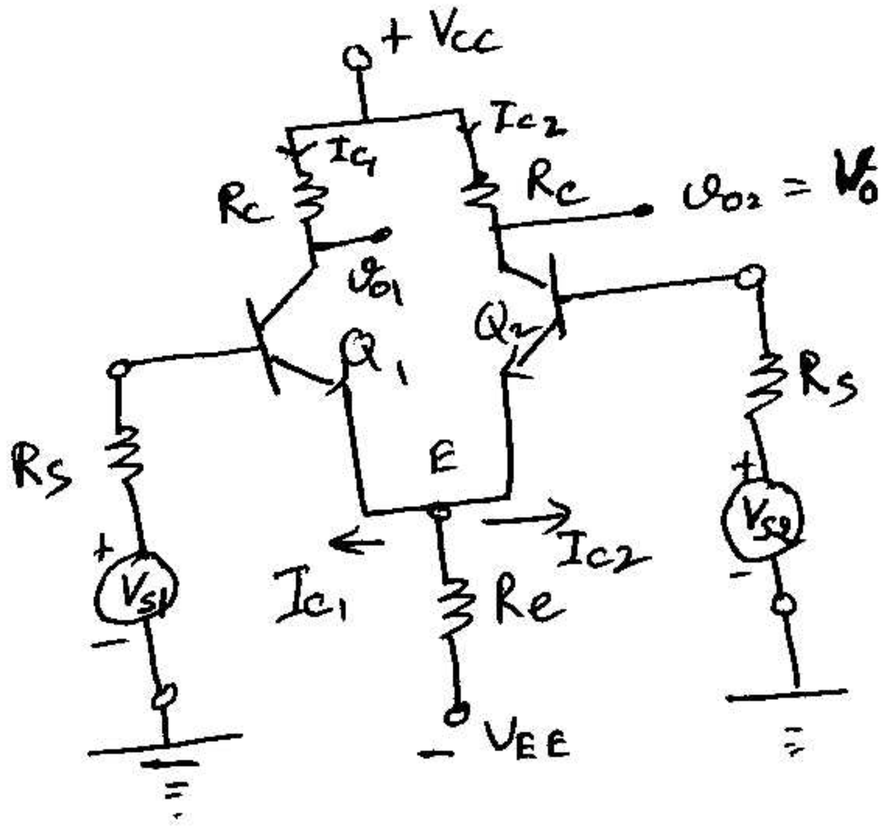
a) An amplifier of 60dB open loop voltage gain has output resistance of 10kΩ and input resistance of 500Ω.Calculate (i)the value feedback factor β required to modify this output resistance to 500 Ω by applying series-shunt feedback. (ii)Find the input resistance with feedback. (1.5 + 1.5 =3M)

b) A series-series feedback amplifier employs a trans-conductance amplifier having G_m=100mA/V, input resistance of 10 kΩ, and the output resistance of 100 kΩ. The feedback network has β=0.1 V/mA, an input resistance (with port 1 open-circuited) of 100Ω and an input resistance (with port 2 open-circuited) of 10 kΩ. The amplifier operates with a signal source having a resistance of 10 kΩ and with a load resistance of 10 kΩ. Find (i)the gain, A_f, (ii)the input resistance, R_{in}; and (iii)the output resistance, R_{out}. (1+1.5+1.5 = 4 M)

2)

a) An NMOS differential amplifier is operated at a bias current I of 0.5 mA and has a W/L ratio of 50, $\mu_n C_{ox}$ =250 μA/V^2,V_A=10V R_D=4kΩ. Find
   i) device break over voltage, V_{ov},
   ii) transconductance, g_m,
   iii) output resistance, r_o and
   iv) differential gain, A_d (4x2=8 M)

b) For the differential amplifier circuit shown below, assuming that R_s=0, $h_{oe}(R_c+2R_e)$ <<1, h_{fe}>>1, and h_{ie}<<$2R_eh_{fe}$, show that the CMRR (ρ) is given by ρ = ($h_{fe}R_e$) / h_{ie}. (5 M)



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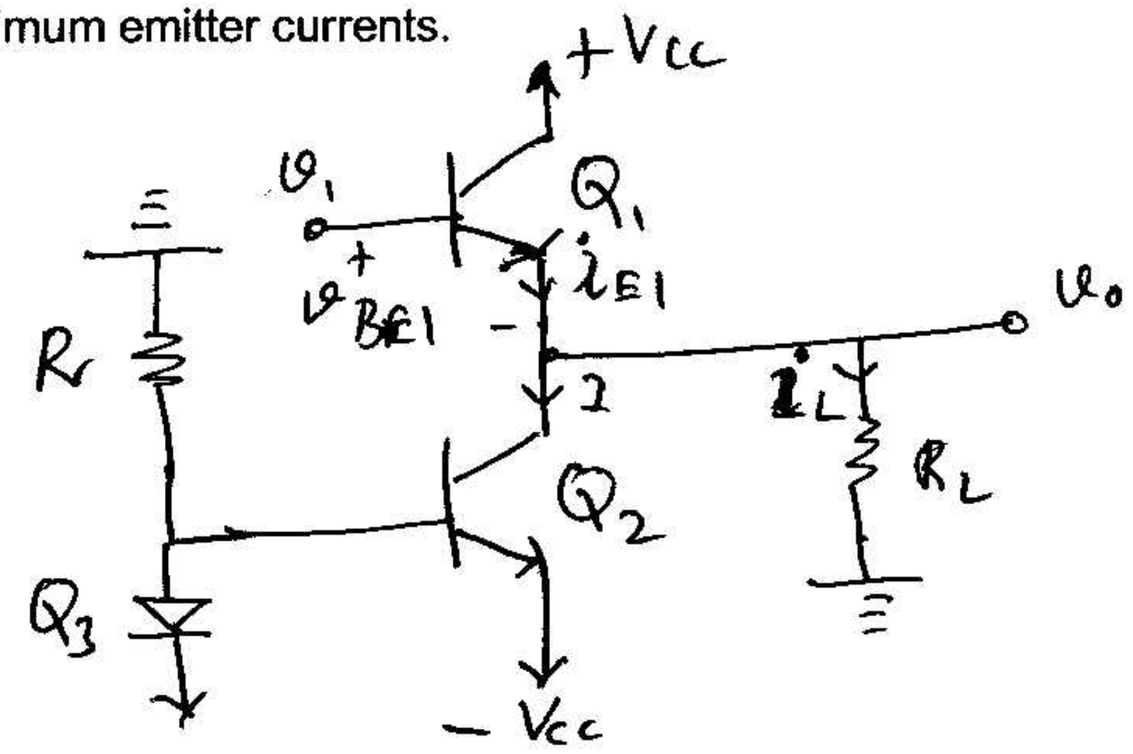
3)

a) For the amplifier in fig below V_{cc}=15V, V_{CEsat}=0.2 V, V_{BE}=o.7 V and constant, and β is very high. Find (i) the values of R that will establish a bias current sufficiently large to allow the largest possible output signal swing for R_L=1KΩ. Also determine (ii)the resulting output swing and (iii)minimum and maximum emitter currents. (2+2+2=6 M)



b) A transistor supplies 0.85 W to a 4 KΩ load. The Zero-signal dc collector current is 31 mA, and the dc collector current with signal is 34 mA. Determine the percent second harmonic distortion. (2M)

c) A single transistor is operating as an ideal class B amplifier with 1 KΩ load. A dc meter in the collector circuit reads 10 mA. How much signal power is delivered to the load? (2M)

4)

a) Design a bandpass RC active filter with midband voltage gain of 30, center frequency of 200 Hz, and Q=5. Hint : Choose C_1=C_2=0.1μF. (5 M)

b) Design an active sixth order Butterworth low-pass filter with a cutoff frequency (f_H) of 1 KHz. (5 M)

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BITS, PILANI – DUBAI

FIRST SEMESTER 2009 – 2010

Test-1 [Closed Book]

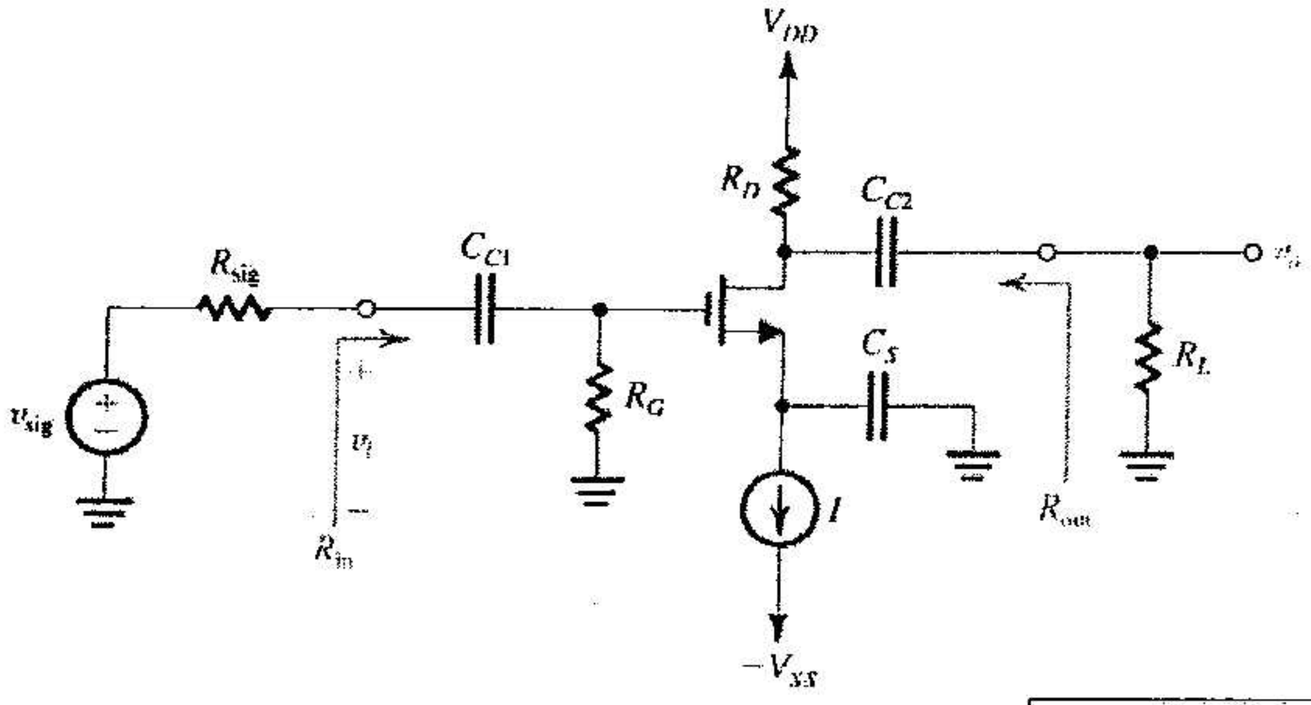
III Yr. B.E.(Hons.)

Course Code: **EEE C424 / INSTR C313**
Course Title: **Microelectronic Circuits**
Duration: **50 minutes**

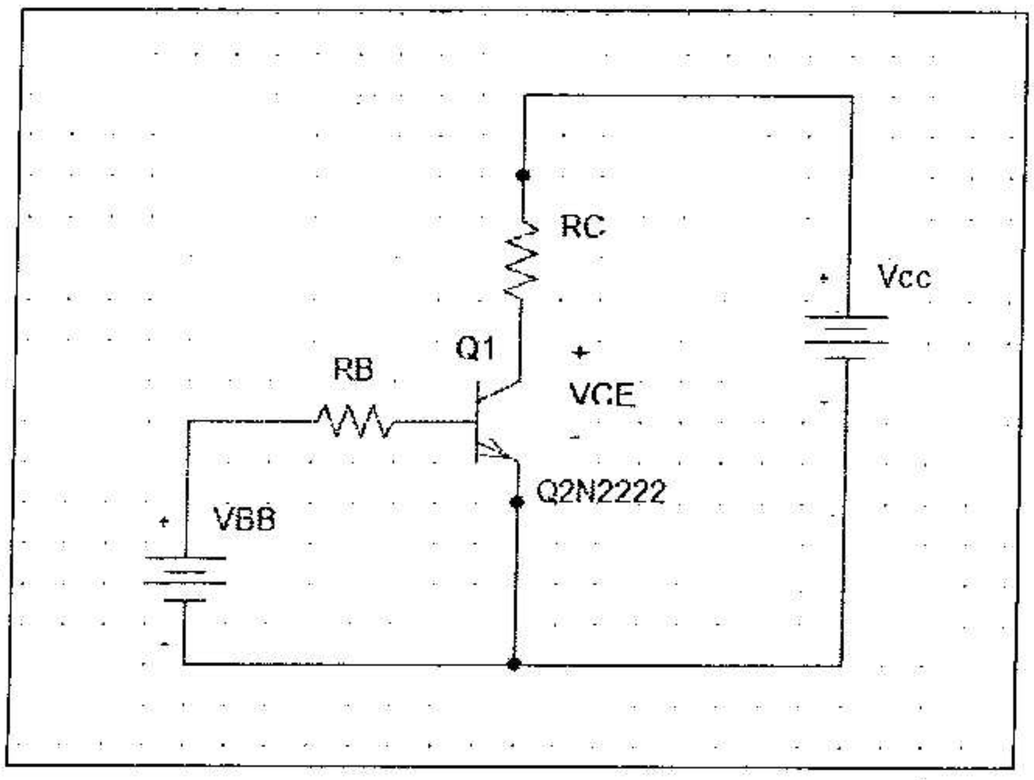
Date: **08.11.09**
Max Marks: **40**
Weightage: **20%**

Instructions: 1.ANSWER All the questions.
2. Make assumptions, if any, but explicitly indicate the assumptions made

1. Define the following terms w.r.t. an amplifier (a) Transfer Gain (b)Figure of merit (c)Bandwidth (d)Amplifier Saturation (e)Input Resistance. [10M]
2.
   a. Draw the both the hybrid-π models of a BJT when used as an amplifying device. Also indicate expressions for each of the model parameters [2+2=4M]
   b. If BJT has a β=120 and is biased to operate at a dc collector current of 1.2 mA. Find values of parameters of any one of two models of part (a) above. [2M]
3. Compare/contrast "the NMOS" and "the n-p-n" Transistors in respect of (a)Circuit symbol (b)the conditions (in terms of equations to be satisfied) under which each act as Amplifier (c)Low Frequency hybrid Model (d)High Frequency Model and (e)the Design Parameters[1+2+2+2+2=9M]
4. List five steps involved in the small signal analysis of a transistor amplifier [5M]
5. A MOSFET CS amplifier with R_{in}=2 MΩ and R_D=10kΩ, shown in figure below, is fed from a voltage source with an internal resistance (R_{sig}) of 500 kΩ and is connected to a 10-kΩ load (R_L). Device parameters are: g_m=4 mA/V, r_o=100kΩ, C_{gs}=2pF, and C_{gd} = 0.5pF. Find (a)the overall mid band gain A_M and (b) the upper 3-dB frequency f_H and (c)R_{out}. [2+2+2=6M]



6. In the BJT amplifier circuit shown, if β=100, I_{BQ}=20μA, V_{CC}=15V and R_C=3kΩ. If I_{CBO} = 0 Find (a) I_{EQ}(b)V_{CEQ} (c) Find V_{CEQ} if R_C is changed to 6 kΩ and all else remain same [1+1.5+1.5=4M]



ALL THE BEST

NAME: _____; ID NO:_____; Sec.: _____;

Prog.: B.E. (Hons.) _____ Version B

BITS, PILANI – DUBAI

FIRST SEMESTER 2009 – 2010

Course Code: **EEE C424 / INSTR C313** **THIRD YEAR** Date: **23.11.09**

Course Title: **Microelectronic Circuits** Max Marks: **20**

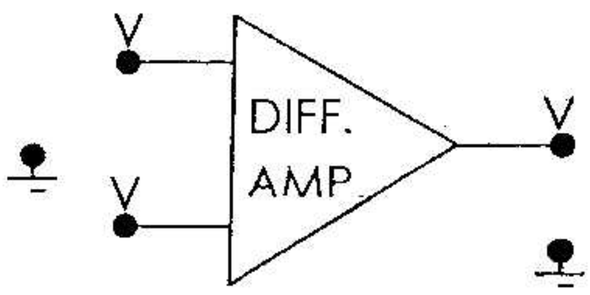
Duration : **20 minutes** Weightage: **10%**

Instructions: 1.ANSWER All the questions **with most appropriate answer(s)**, at the space provided.

2. Make assumptions, if any, but explicitly indicate the assumptions made

1. Draw the circuit of a two stage BJT Amplifier consisting of a CE-CC cascade. Indicate the expected mid-band voltage gain for this cascade (either in terms of a value or expression for both). (2+2=4)

2. Derive an expression for the output voltage of the differential amplifier shown below in terms of differential gain, differential and common mode voltages and CMRR. (4)



3. What is the value of CMRR for an Ideal Differential Amplifier? – Justify the same. How this value for an ideal Differential Amplifier can be interpreted in most of the applications? (1+2+2=5)

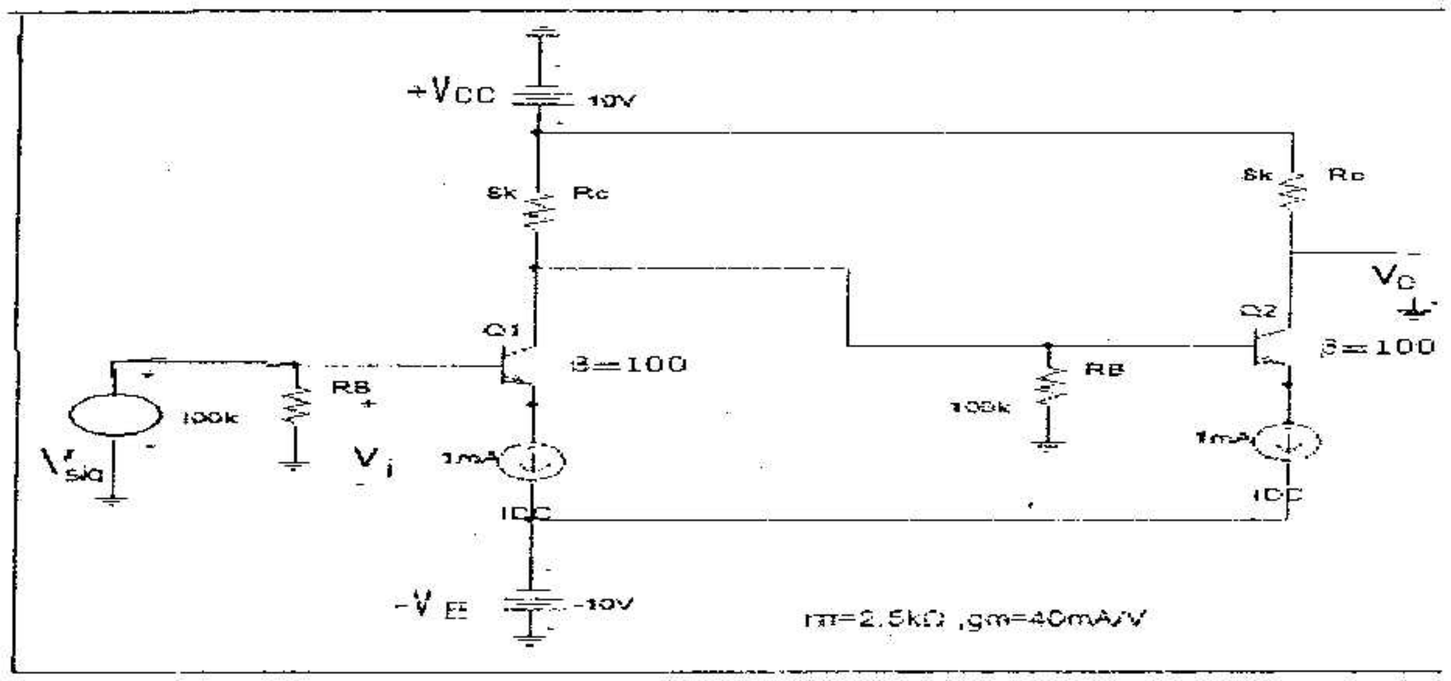
NAME: _____; ID NO:_____; Sec.: _____;

Prog.: B.E. (Hons.) _____ Version B

4. List the main feature that distinguishes an interacting cascade from that of a Non-interacting cascade. (2)

5. Answer Either ONLY (a) OR both (b) & (c).

a. If $|V_{BE} = 0.7V|$ and β=100, find (i) the DC bias current in each of transistor (ii)the DC voltage at the output (iii)output resistance. (iv) the voltage gain (1+1+1+2=5)



OR

b. Match the following configuration of feedback shown under I with the corresponding pair of the way "mixing and sampling" is accomplished as given under II ...by indicating the serial no. of item under I in the braces: "[ ]" of II. (4)

I	II	
i. Series Series	current mixing and current sampling	[ ]
ii. Shunt Series	current mixing and voltage sampling	[ ]
iii. Shunt Shunt	voltage mixing and current sampling	[ ]
iv. Series Shunt	voltage mixing and voltage sampling	[ ]

c. Upon Application of Shunt-Shunt feedback to an open loop Amplifier, its input resistance will _____(increase / decrease / remain unchanged) – Justify the same. (1)

Justification:

* * * *

NAME: _____; ID NO:_____; Sec.: _____;

Prog.:B.E. (Hons.) _____

Version A

BITS, PILANI – DUBAI

FIRST SEMESTER 2009 – 2010

Course Code: **EEE C424 / INSTR C313** **THIRD YEAR** Date: **12.10.09**

Course Title: **Microelectronic Circuits** Max Marks: **20**

Duration : **20 minutes** Weightage: **10%**

Instructions: 1.ANSWER All the SEVEN questions **with most appropriate answer(s)**, at the space provided.
2. Make assumptions, if any, but explicitly indicate the assumptions made
3. Write on back side if the space is insufficient.

1. Define each of the following terms: [1 mark each = 3 M]
   a. Amplifier:

   b. Amplifier Saturation:

   c. Amplifier Efficiency:

2. An Amplifier has a voltage gain of 300 V/V and a current gain of 5000 A/A. Express the voltage and current gains in decibels (dB) and find the power gain. [0.5 + 0.5 + 1 = 2 M]
   a. Expressing Voltage gain in dB:

   b. Expressing Current gain in dB:

   c. Computation of the Power gain:

3. List the three configurations in which a BJT can be used as amplifier: [0.5 mark each = 1.5 M]
   a. Configuration No.1:
   b. Configuration No.2:
   c. Configuration No.3:
4. What is the current gain of a CB amplifier? Justify your answer – as why is it so? [0.5+1=1.5 M]
   a. Current gain of a CB Amplifier is:
   b. It is so because:

5. List the four most important terminal characteristics of an Amplifier: [0.5 mark each=4 M]
   A. C.
   B. D.

NAME: _____; ID NO:_____; Sec.: _____;

Prog.:B.E. (Hons.) _____

Version A

6. Determine the following for the circuit shown in Fig. (1). [2+1+1+1=5M]

   a. BJT's Operating point:

   b. Voltage across base emitter Junction:

   c. Base current:

   d. Important assumptions made in the above computation are (please write "NIL", if you have not made any assumptions; else state the two most important assumptions):
   (1):

   (2):

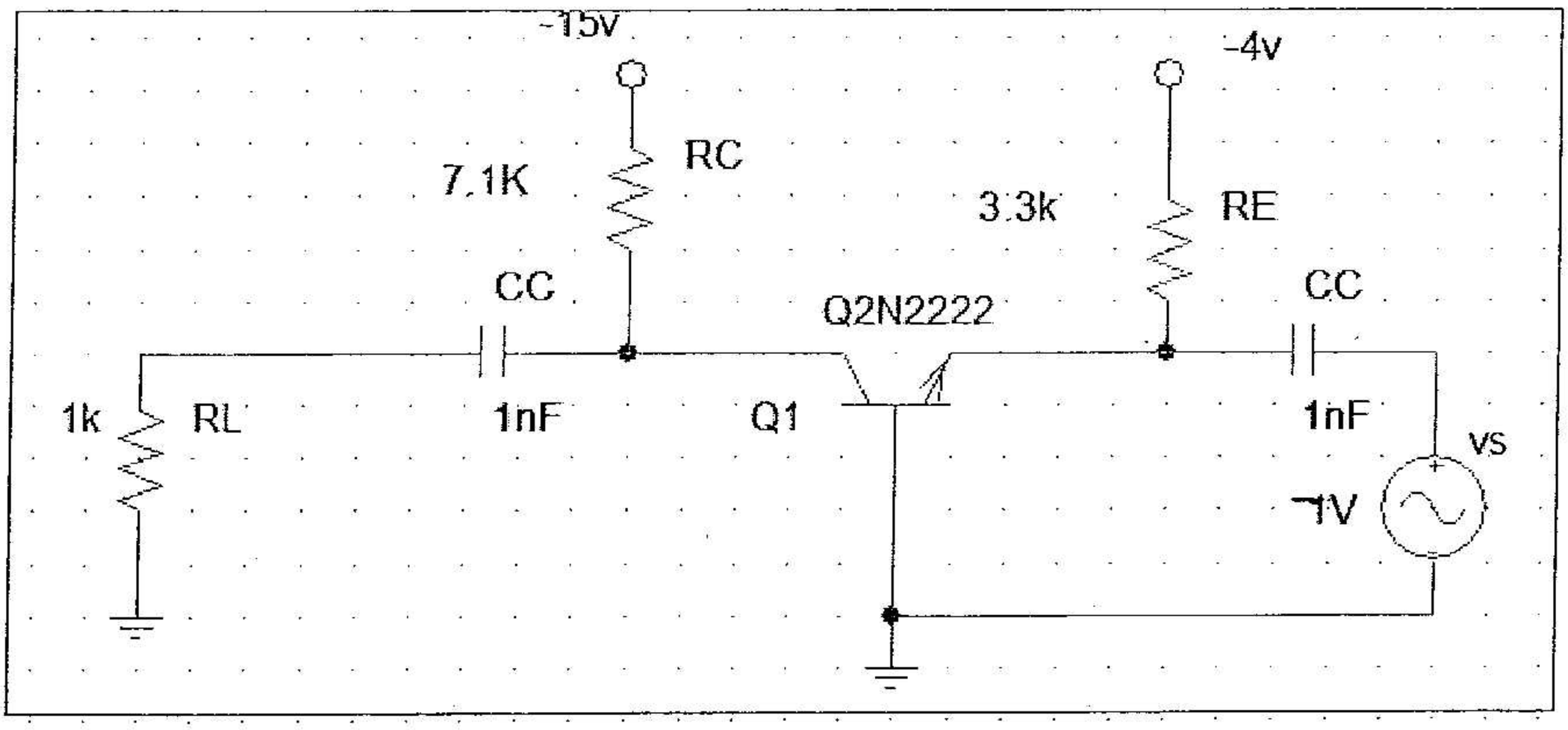


Fig. (1) Circuit for Question No.5

7. Draw BJT's Hybrid π-model and indicate expressions using which model parameters can be determined. [1+2=3 M]

   a. BJT's Hybrid π-model is as follows:

   b. Expressions to compute model parameters are: