BITS, PILANI – DUBAI

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI

Year III – Semester I 2009 – 2010

Comprehensive Examination (Closed Book)

Course No.: **CS / INSTR C 391** Course Title: **DECO**

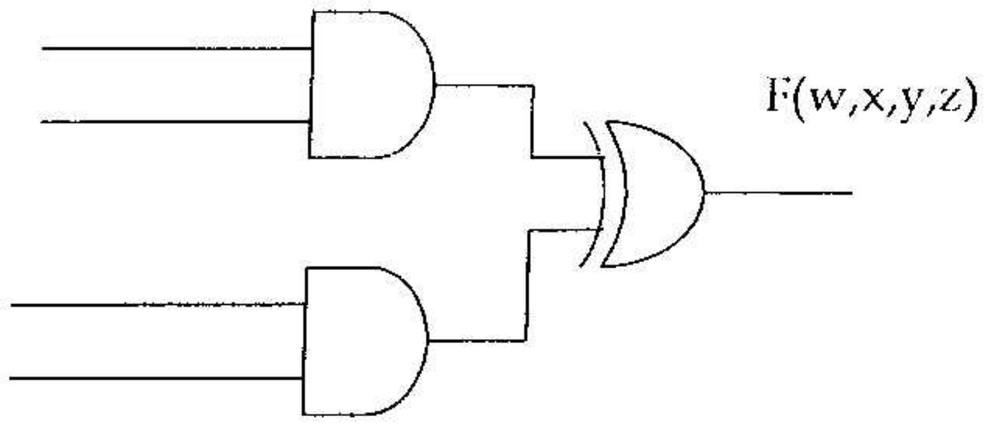
Date: Dec 29, 2009 Time: 3 Hours Max. Marks = 80

(Answer questions from Part A and Part B on separate answer sheets . All parts of a question should be answered continuously. Clearly state any assumptions made.
Assume all logic gates are using positive logic. **Calculators are not allowed.**)

PART A

1. a) Given the following equation, determine the base x that permits the equation to be true. $(37)_x + (24)_x = (60)_x$
   b) Assuming the two input OR gate has delay of T seconds, write a formula for the gate delay of an N input OR gate implemented using 2-input OR gates.
   c) What range of decimal values can be represented by a four-digit hex number?
   (3+2+2)

2. a) Prove that $XZ + Y'Z + Z' = X + Y' + Z'$ using Boolean laws.
   b) Draw the Multi level NOR realization for the expression $F = W (X + Y + Z) + XYZ$. Assume only true inputs are available.
   c) Draw the K-map and assign variables to the inputs of the AND-XOR circuit in the following figure so that the circuit output is $F(w,x,y,z) = \sum (6,7,12,13)$



(2 + 3 + 5)

3. a) Write the Boolean expressions for a three bit magnitude comparator which compares two three bit binary word $A_2A_1A_0$ and $B_2B_1B_0$. Implement the circuit using basic logic gates.

   b) A BCD code is being transmitted to a remote receiver. The bits are $A_3A_2A_1A_0$ with A_3 being the MSB. The receiver circuit includes a BCD error detector circuit that examines the received code to see if it is a legal BCD code. Design this circuit to produce a HIGH for any error condition. (5 + 4)

4. Design a **combinational circuit** which will convert a 3-bit number into its 2's complement. In your design use only the following components. **Four 2- input XOR** gates and **one 2-input AND** gate. (8)

5. Design a feedback sequential circuit using a four bit universal shift register which has the facility of loading new data, clearing data, shifting left and shifting right. The circuit is to generate the sequence 111001 repeatedly. Assume the bits of the register are A, B, C and D with A as MSB and the shift register is used in the shift left mode (A to D). (6)

(P.T.O)

PART B

6. a) Draw the PROM programming fuse map for a four bit binary to gray code converter. Also tabulate the PROM programming table.
   b) What is the need for data transfer in I/O devices ? Explain the following with reference to I/O devices. i) Modes of data transfer ii)Control of data transfer (4+4)

7. The specification of a 7408 IC is given below. Find the Fan-out, Power dissipation, Propagation delay and Noise Margin of the IC
   I_{OH} = 1 mA; I_{OL} = 20 mA; I_{IH} = 0.05 mA; I_{IL} = 2 mA;
   I_{CCH} = 10mA; I_{CCL} = 20 mA; t_{PHL} = 3ns; t_{PLH} = 4ns;
   V_{CC} = 5 V; V_{OH} = 2.7 V; V_{OL} = 0.5V; V_{IH} = 2V; V_{IL} = 0.8 V (2 x 4)

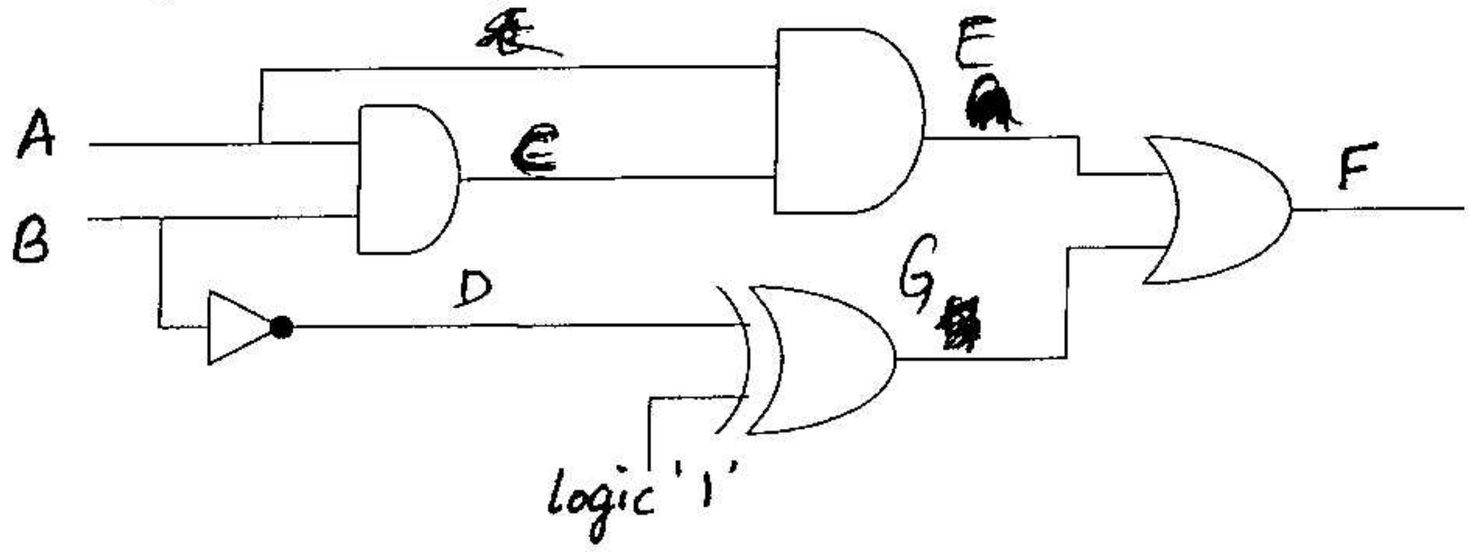
8. With the help of a flow chart, explain the working of the integer division algorithm using **Non-restoration method**. Perform the division of the following two unsigned binary numbers 1110 / 0011 and show the working in steps (2+4)

9. A logic circuit is given below with its inputs as 'A', 'B' and 'logic 1' respectively.

   a. Write the corresponding HDL codes for the gate level description of the logic circuit clearly marking the wire signals. Assume all the two input logic gates have propagation delay of 5ns each and the inverter has a propagation delay of 3ns.

   b. Write a stimulus to give the inputs A and B as follows. Both the inputs A and B were at logic low initially at t =0. **After 20ns,** B is made high and **after another** 10ns A is also made high. **At t=40ns,** input B is made low. The simulation should run for **50ns.**

   c. Draw the input and the output waveforms along with the wire signals.



(2+3+3)

10. A sequential circuit has two D flip flops A and B and one input x and one output y. The circuit is described by the following next state and output equations.
    A(t + 1) = AB + A'x ; and B(t+ 1) = A'B + B'x y = Ax + B'
    i) Draw the sequential circuit
    ii) Write the state table of the circuit
    iii) Draw the state diagram of the circuit
    iv) What will be the output sequence if the following input sequence (01101001011) is applied to the circuit starting from the state '00'. (2 + 2 + 3 + 3)

********** Good Luck **********

BITS – PILANI DUBAI

Dubai International Academic City, Dubai

I semester III Year 2009-2010

Digital Electronics & Computer Organisation / CS / INSTR C 391

Test -II **(Open Book)**

16 – 12 – 09 **Time : 50min.** Max. Marks : 25 **Weightage : 12.5 %**

(Answer all questions)

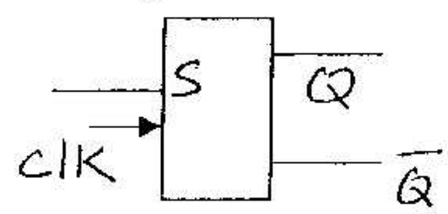
(ONLY Text book and H/W notes are allowed)

1. How many 16K x 8 RAM chips are needed to provide a memory capacity of 56KB? How many address lines will be needed to address this memory bank? Show the decoding of address lines to generate the chip select signals of the memory units using a decoder. Also specify the size of the decoder (6)

64KB

2. Using the positive edge triggered S flip flop whose characteristics table is given below, design a synchronous mod-6 counter to count in the sequence 1,3,5,2,4,6 repeatedly. (Drive the unused states to "1" as next state) (6)

S	Q(t+1)
0	Q'
1	Q



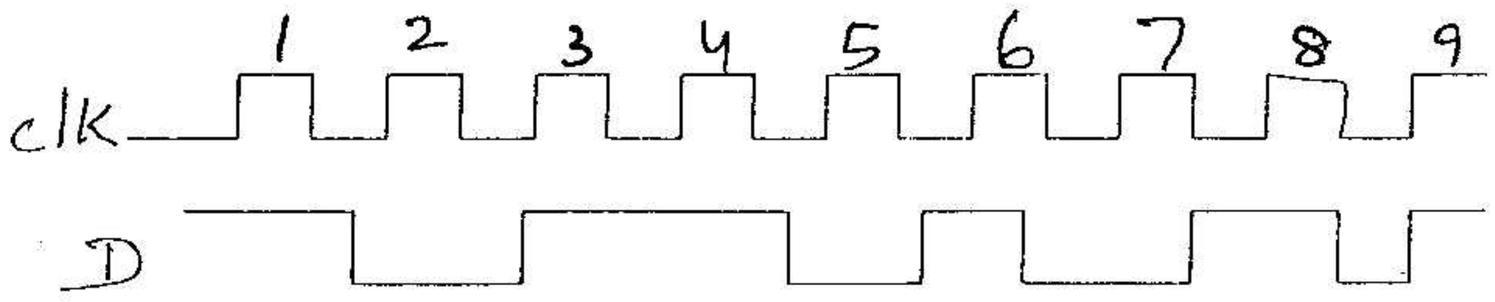
3. A sequential circuit has two JK flip flops P and R and one input x . The circuit is described by the following flip flop input equations.

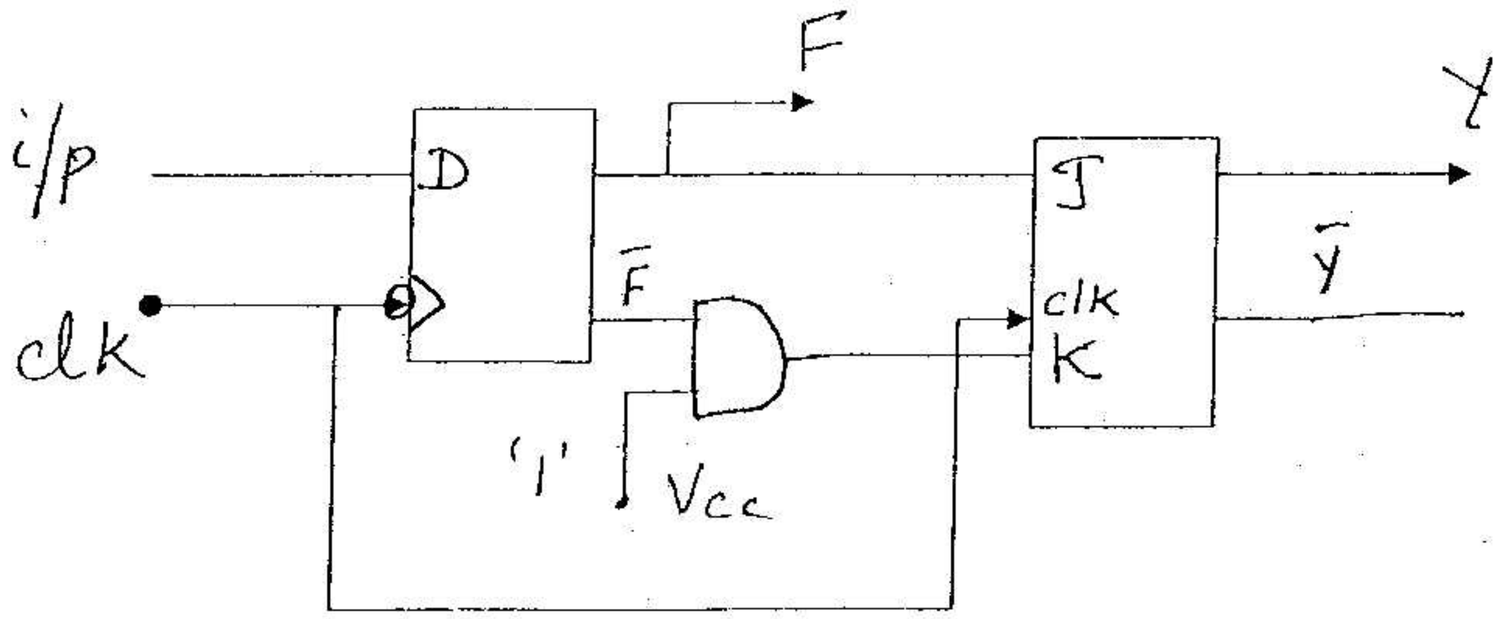
$J_P = x$; $K_P = B'$; R' $J_R = x$; $K_R = A$; P.

a) Derive the state equations P(t+1) and R(t+1) b) write the state table

c) draw the state diagram of the circuit. d) Draw the sequential circuit (7)

4. In the sequential circuit given below, the input applied to the D flip flop along with the clock pulse applied is shown in Figure 1. Draw the out put F and Y of the circuit. Assume that the outputs F and Y are at zero initially. (6)





$\overline{A}B + \overline{A}C$

BITS, PILANI – DUBAI

Dubai International Academic City
Year III – Semester I 2009 – 2010
Test I (Closed Book)

Course No.: **CS / INSTR C391** Course Title: **DECO**

Date: November 01, 2009 Time: 50 Minutes Max. Marks = 25

(Answer all questions. Calculators are not allowed.)

1. a) Using BCD arithmetic perform the operation $(682 + 394)_{10}$ and explain the result.

   b) Consider the Boolean function $F=\bar{X}Y+X\bar{Y}$. At time t = 0 , all the variables are set to zero. At t=20 msec, X toggles and again toggles at t = 50 msec. Y toggles at t = 25 msec, and again toggles at t = 55 msec. Sketch the timing diagram for the logic circuit inputs and the circuit output (Note : Toggle means that the variable switches to the opposite value from the one it was in) (2 + 3)

2. a) Using De morgan's theorem, represent the function below
   F(a,b,c) = ac' + a'c' + bc'
   i) with only OR & NOT operations
   ii) with only AND & NOT operations

   b) A network Router Connects multiple computers together and allows them to send messages to each other. If two or more computers send messages simultaneously they collide and the message has to be sent again. Design a collision detector circuit which has 4 inputs labeled A , B , C & D respectively (corresponding to the computers) that are '1 ' when the corresponding computer is messaging and '0' otherwise. The collision detection circuit has its output labeled ' F ' which is one whenever a collision is detected and '0' otherwise.
   Draw the truth table for the collision detection problem and find the minimum SOP expression for F(A,B,C,D) using K-map. (3+4)

3. Implement the following function 'F' along with the don't care conditions 'd', **using no more than two NOR gates.**
   F(p,q,r,s) = $\sum$ (0,1,2,9,11); d(p,q,r,s) = (8,10,14,15); (3)

4. a) What is a full adder? Draw the block diagram level representation of a full adder circuit **using two half adders and external logic gates.**

   b) Explain **four bit Carry look ahead generator**. Using the same circuit and external logic gates draw a circuit which will add two four bit binary words to produce the sum and the carry. (Use Block diagram representation of four bit Carry look ahead generator). (2+ 3)

5. a) Using **one 3 X 8 active low decoder** and any **three 3- input logic gates** realize the following three functions
   F(A,B,C) = A(B+C) + A'B'
   G(A,B,C) = $\sum$ (0,1,4,5,7)
   H(A,B,C) = ABC + A'B'

   b) Show how to build an 8X 1 multiplexer by using two 4 x 1 and one 2 x 1 multiplexers only
   (3+2)

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Good Luck

SET A

Name :

Id :

BITS, PILANI – DUBAI CAMPUS

Dubai International Academic City

Year III – Semester I 2009 – 2010

Quiz II (closed Book)

Course No.: **CS / INSTR C 391** Course Title: **DECO**

Date: 09- 12- 2009 Time: 20 Minutes Max. Marks = 10

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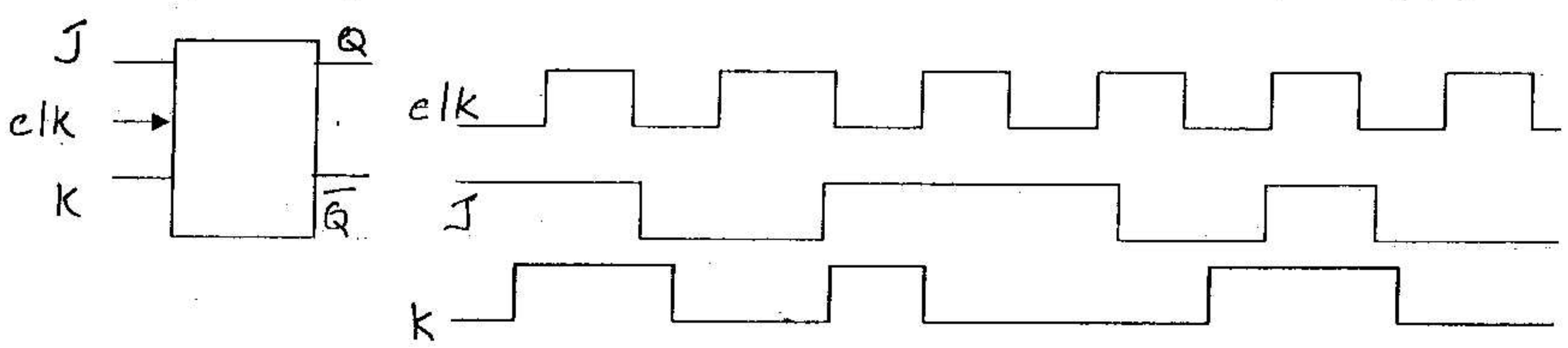
1. In a Jkflip Flop, the input is applied as shown in the figure. Draw the out put Q of the flip flop assuming initial state was zero. (2M)



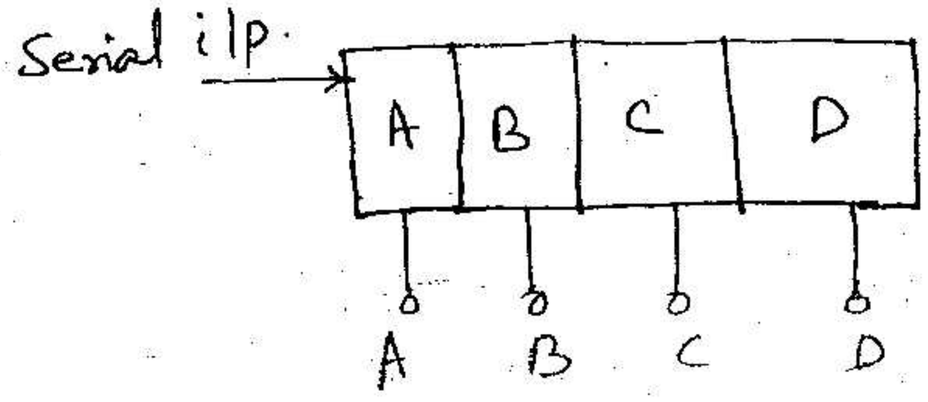
2. Draw the present state-next state table for the T flip-flop. Hence, derive the characteristic equation of the T flip-flop (2M)

3. If you are given 512 x 8 capacity memory ICs and one 3 x 8 decoder, what is the maximum size of memory bank you can address in kilobytes? (2M)

4. Match the following definitions of programmable logic devices (2M)

i. PROM	A) Programmable AND array Programmable OR Array
ii. PLA	B) Programmable AND array fixed OR array
iii. PAL	C) Fixed AND Gate array Programmable OR array
iv. FPGA	D) Programmable encoders and Programmable decoders
	E) Field Programmable arrays

5. In a 4 bit shift register ABCD initially loaded with 0110, What would be the data after three clock pulses if the serial input at A given is 0-1-0-1. (2M)



Name : Id. No :

BITS, PILANI – DUBAI **SET A**

International Academic City, Dubai

Year III – Semester I 2009– 2010

Course No.: **CS / INSTR C 391** Quiz I Course Title: **DECO**

Date: October 14, 2009 Time: 20 Minutes Max. Marks = 10

(Calculators are not allowed. Clearly state the assumptions made.
All functions are based on positive logic.)

1. Simplify the following expression using Boolean algebra: x' + y' + xyz'

2. Impliment the following function using only OR and NOT logic operations:
   F(A,B,C) = AC' + A'C' + BC'

3. Convert the following 2's complement signed number to a decimal number 1111 1101 1010

4. Add -5 and -4 using two's complement arithmetic

5. Find the complement of the following function and simplify it: **x'(y'+z')(x+y+z')**

6. Determine the canonical sum of products of the expression: $P(x,y,z) = z + (x'+y)(x+y')$

7. Show the truth table for the following function: $f(x,y,z) = xy + yz$

8. Convert $(A4)_{16}$ to Octal

9. Convert the given Gray code into its equivalent Binary code: 101101

10. Write the min terms for the following expression: $\sum(4,5,8)$ (assume the input variables)

Good Luck