BITS-Pilani Dubai, International Academic City, Dubai

Evaluation Component : **Comprehensive Examination (Closed Book)**

I semester Academic Year 2007-2008, III B.E.(Hons.) EEE and EIE

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 7th Jan. 2008 **Max. Marks: 80**

Duration: Three hours **Weightage: 40%**

Note:- 1. ANSWER ALL QUESTIONS
2. Make assumptions, if any, but explicitly indicate the assumptions made

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1)

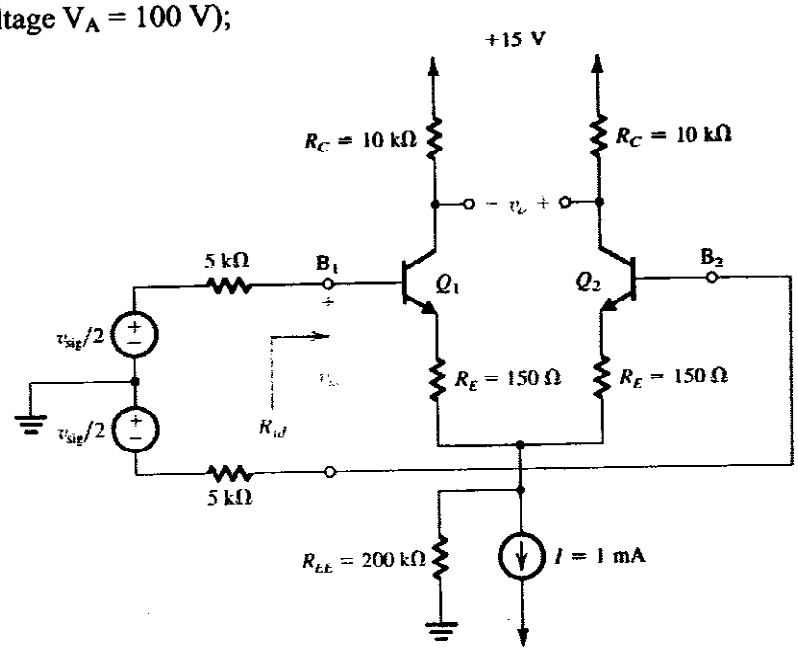
a) A MOSFET amplifier is fed with a signal source having an open circuit voltage v_{sig} of 10mV and internal resistance R_{sig} of 100 kΩ .The voltage v_i at the amplifier input and the output voltage v_o are measured both without and with a resistance R_L =10 kΩ connected to the amplifier output. The measured results are as in table below. Find A_{vo}, G_{vo}, A_v, G_v, G_m, R_i, R_o and A_{is}. (6 M)

Load	v_i (mV)	v_o (mV)
Without R_L	10	100
With R_L connected	7	72

b) Draw the circuit of a CE Amplifier including its source and load. Analyze the circuit using h-parameter model to obtain expressions for its (i) Voltage Gain (ii) lower 3dB frequency cutoff and (iii) higher 3dB frequency (10 M)

2)

a) Assuming BJTs used in the circuit shown below have the same β=100, evaluate (i) the differential input resistance R_{id}; (ii)the over all differential voltage gain v_o / v_{sig} (Neglect the effect of r_o); (iii) the worst case common mode gain if the two collector resistance are accurate to within ±1%; (iv) the CMRR in dB; (v)the input common mode resistance(assuming that early voltage V_A = 100 V); (7.5 M)



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b) A typical CE amplifier is constructed employing (a BJT with its $\beta_{dc} = 100$) the following values for various circuit components:
$R_C = 3.6\ k\Omega$, $R_E = 1.K\Omega$ with an emitter bypass capacitance of C_E, the bias resistors: R_2 (between base and Ground)$=2.2K\Omega$, R_1 (between Base and V_{cc})$= 10\ K\Omega$. The amplifier receives ac input from a voltage source having resistance of $600\ \Omega$ through a blocking capacitance C_b. The output of the amplifier is connected to $10K\Omega$ load resistance through coupling capacitor C_c.; $V_{cc} = 10V$
In the circuit as above, V_{CE}, when measured is found as 6V. Draw the circuit diagram, as above, and analyze for
i) values of V_{BE}, I_C and I_B.
ii) the reason as why the ac voltage across the load resistance is found to be zero, when the circuit constructed as above, in practice, is fed with a 1mV ac swing from the ac source at the input, while ac voltmeter connected across collector and ground reads 70mV. (6 M)

3)

a) A single transistor is operating as an ideal class B amplifier with a $1K\Omega$ load. A dc meter in the collector circuit reads 10mA. How much signal power is delivered to the load? (2.5M)
b) Why Non linear distortion should be considered while designing power amplifiers (2 M)
c) What is cross over distortion with reference to power amplifiers? With a neat sketch of the circuit diagram, explain how cross over distortion can be eliminated in power amplifiers. (5 M)
d) Show through a mathematical analysis, that in a push-pull complementary symmetry circuit, no even harmonics are present. (4 M)

4)

a) List and discuss the steps involved in the design of Butterworth Low pass filter indicating the typical specifications to be considered for designing the same. Compare and contrast its frequency response features with those of Chebyshev filter. (6 M)
b) A voltage signal source with a resistance $R_s = 100\ K\Omega$ is connected to the input of a common emitter BJT amplifier. Between base and emitter a tuned circuit is connected with $L = 1\mu H$ and $C=200$ pF. A transistor is biased at 1 mA and has $\beta = 200$, $C_\pi = 10pF$; $C_\mu = 1pF$; The load resistance is $5\ K\Omega$. For this single tuned amplifier find
i) Resonance frequency, ω_0; (1 M)
ii) Quality factor, Q, (2 M)
iii) 3 dB bandwidth and (1 M)
iv) the center frequency gain (1 M)

5)

a) An amplifier with open-loop gain $A_V = 1{,}000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than $\pm 0.1\%$.
i) Find the reverse transmission factor β of the feedback network used (2.5 M)
ii) Find the gain with feedback (2.5 M)
b) Indicate, in tabular form, the following for both the Voltage Series and Current Shunt feedback configurations / topologies (i) fed-back signal, (ii) sampled signal, (iii)feedback factor, (iv)open loop transfer gain (v)transfer gain with feedback, (vi)output resistance with feedback, (vii) input resistance with feedback and (viii)desensitivity factor (8 M)

6) Write short notes on the following (12 M)
a) Stagger tuned amplifier
b) IC biasing employing Current Mirrors
c) Sub-systems / circuit blocks that make an IC OPAMP and their specifications

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Evaluation Component : **TEST-II (Closed Book)**

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 9th Dec. 2007 **Max. Marks: 20**
Duration: 50 mts **Weightage: 20%**

Note:- 1. ANSWER ALL QUESTIONS
2. Make assumptions, if any, but explicitly indicate the assumptions made

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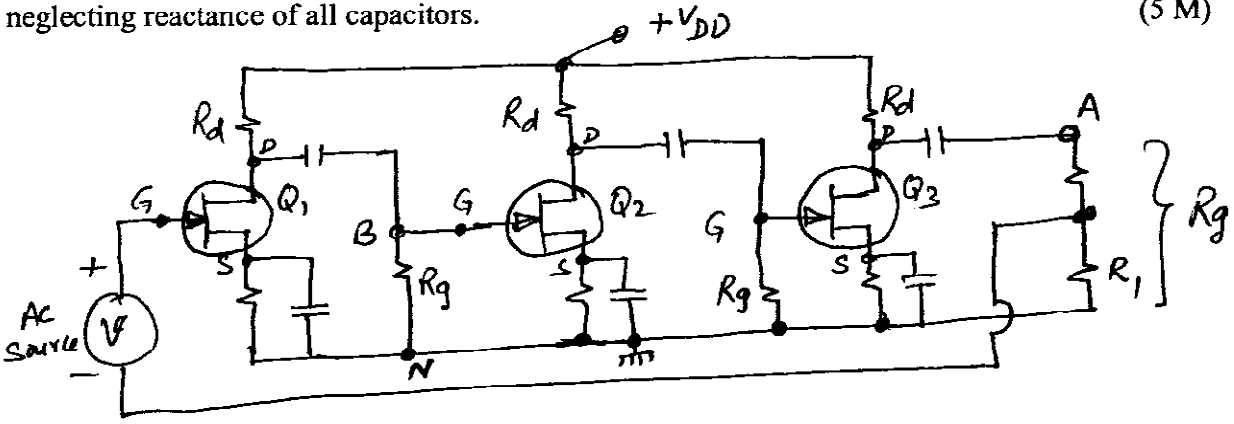
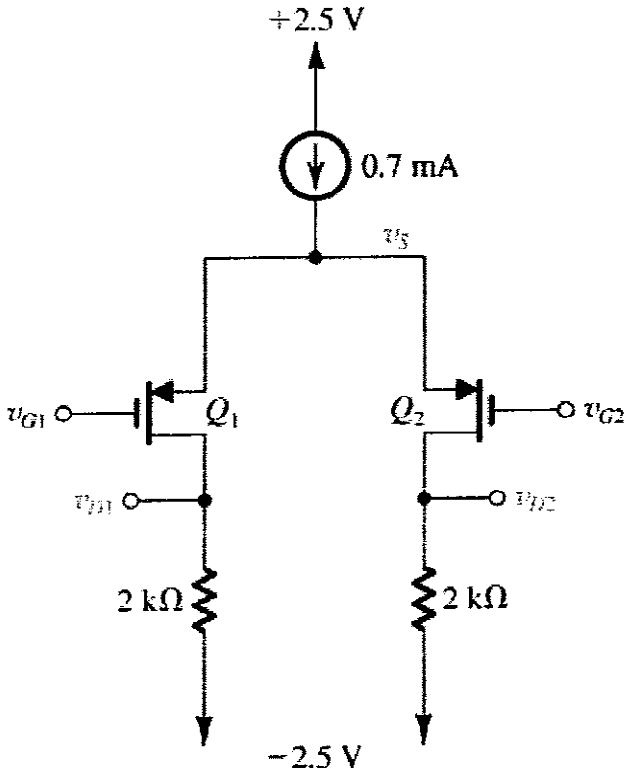
1) For the circuit shown below, Find the (A)Voltage gain and (B)output impedance at the terminals (i)AN and (ii)BN of the circuit assuming that g_m=6 mA/V and r_d=10 KΩ, R_g=1MΩ; R_d=50 KΩ, neglecting reactance of all capacitors. (5 M)



2) For the PMOS differential pair shown figure, let Vtp=-0.8 V, and k_n'W/L=3.5mA/V^2 .Neglect channel length modulation λ=0 (4 M)

a. find Vov and V_{GS} for each of the MOSFET
b. find v_S
c. If the current source requires a minimum voltage of 0.3V,find the input common mode voltage



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3) Justify the following statements conceptually from fundamentals (1.5M)
   a. Input impedance of Voltage amplifier is large
   b. Output Impedance of Voltage amplifier is small
   c. CMRR of a Differential Amplifier is very high close to infinity(theoretically)

4) An amplifier with open-loop gain A_V=1,000±100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.1%.
   a. Find the reverse transmission factor β of the feedback network used (2 M)
   b. Find the gain with feedback (2.5M)

5)
   a) A voltage signal source with a resistance R_s = 100 KΩ is connected to the input of a common emitter BJT amplifier. Between base and emitter a tuned circuit is connected with L = 1μH and C=200 pF. A transistor is biased at 1 mA and has β = 200, C_π=10pF; C_μ=1pF; The load resistance is 5 KΩ. For this single tuned amplifier find
      i) Resonance frequency, ω_0; (1 M)
      ii) Quality factor, Q, (2 M)
      iii) 3 dB bandwidth and (1 M)
      iv) the center frequency gain (1 M)

OR

   b)
      i) A single transistor is operating as an ideal class B amplifier with a 1-K load. A dc meter in the collector circuit reads 10mA. How much signal power is delivered to the load? (2.5M)
      ii) Show through a mathematical analysis, that in a push-pull complementary symmetry circuit, no even harmonics are present. (2.5 M)

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Evaluation Component : TEST-I (Closed Book)

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 28th Oct. 2007 **Max. Marks: 25**
Duration: 50 mts **Weightage: 25%**

Note:- 1. ANSWER any 5 QUESTIONS
2. Make assumptions, if any, but explicitly indicate the assumptions made

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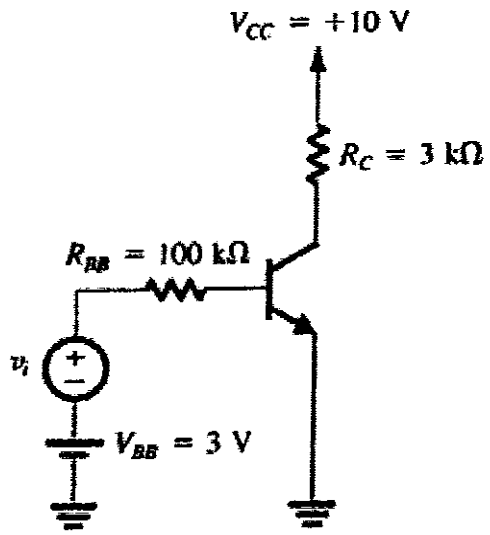
1) a) List the important considerations in choosing the BIAS POINT while designing of a BJT Amplifier (2.5M)
b) Draw the h-parameter model of a BJT and define all the four parameters. Also indicate how they can be obtained from the characteristics of the active device (2.5M)

2) a)List the steps in performing ac analysis of an Amplifier employing either BJT or FET (2.5M)
b)Define the following terms with reference to a General Purpose Amplifier: (i)Voltage Gain; (ii)Bandwidth (iii) Amplifier saturation (iv) Maximum signal handling Capacity (v)Efficiency (2.5M)

3) Determine the voltage gain for circuit given below. Assume $\beta = 100$ (5.0M)



4) Derive the expression for Rin, Rout Avo, Ais and Gv of CE amplifier circuit having
i) Emitter Resistance Re
ii) Load Resistance R_L
iii) The signal source voltage with series resistance Rsig (5.0 M)

5) a) Write various factors affecting the frequency response of BJT amplifier (2.5M)

b) Draw the circuit of BJT Self Bias and Fixed Bias schemes. Also list the advantages and disadvantages of each scheme. (2.5M)

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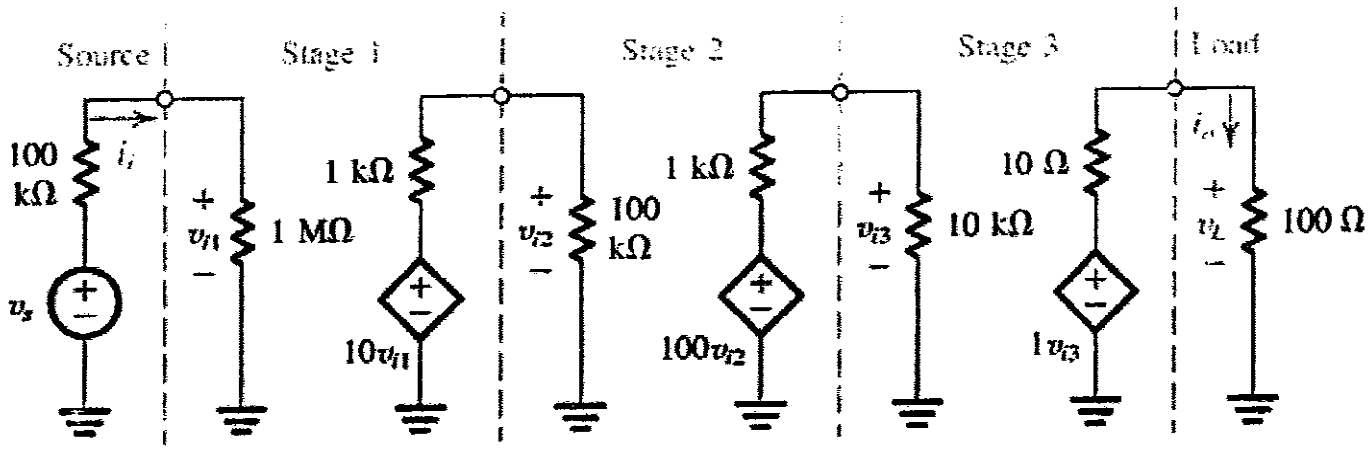
6) The following figure shows an amplifier composed of a cascade of three stages.Find its voltage gain, current gain and power gain (5.0M)



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