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Name:

ID Number:

BITS PILANI DUBAI CAMPUS
EEE UC424/INSTR UC313
MICROELECTRONIC CIRCUITS
QUIZ 1

Date: 21/09/06
Weightage: 10%

Max. Marks: 10
Time: 30 mts

Answer ALL Questions

1) An amplifier has a voltage gain of 100 and a current gain of 1000. The voltage gain is ___ dB and current gain is ___ dB. The power gain is ___ dB.

2). Show the circuit model of a voltage amplifier.

3 Show the equivalent circuit of trans resistance amplifier.

4 Show the frequency response of Direct coupled and Tuned amplifiers

5 Define amplifier bandwidth.

6 Draw the small signal circuit model for a bipolar junction transistor (BJT).

8. Show the High pass magnitude response of single time constant network.

7. Show the low pass single time constant network.

9. Show the output characteristics of BJT in common emitter configuration.

10. Define h parameters of two port network.

BITS-Pilani Dubai Campus, Knowledge Village, Dubai

Evaluation Component : **Comprehensive Examination (Closed Book)**

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 26th Dec. 2006

Duration: THREE Hours **Max. Marks: 100**

Weightage: 40%

Note:- 1. ANSWER ALL QUESTIONS
2. Students are permitted to use their own blank graph sheets after taking signature of invigilator on it just before its usage
3. Make assumptions, if any, but explicitly indicate the assumptions made

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1.

A. Define the following terms with reference to a general purpose amplifier
   i. Voltage Gain in dB
   ii. Current Gain in dB
   iii. Amplifier Efficiency
   iv. Transfer Characteristics
   v. Amplifier Saturation

[10 M]

B. Draw the circuit model for a voltage amplifier. With the input signal source and the load connected to it, derive expressions for (i)the amplifier's output voltage, v_o; (ii)voltage gain A_v; (iii)amplifier's input voltage, v_i and (iv)the overall voltage gain, v_o/v_s. [6 M]

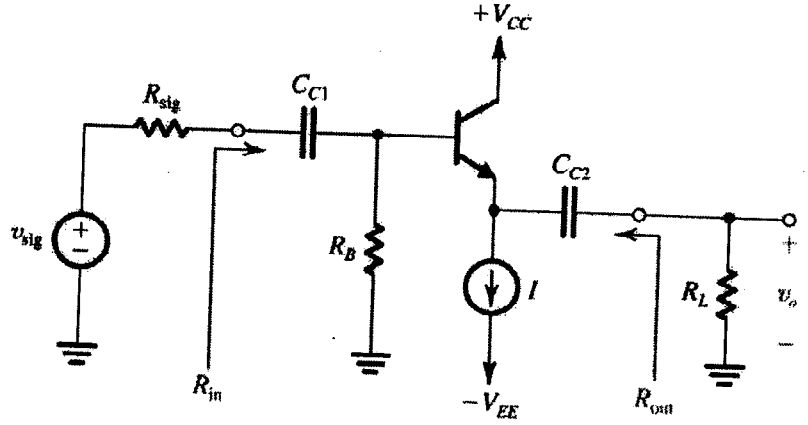
C. Consider a voltage amplifier having a frequency response of a low pass Single Time Constant type with a dc gain of 60dB and a 3 dB frequency of 1000Hz. Find the gain in dB at f = (i)10Hz, (ii)10 KHz; (iii)100 KHz, and (iv)1 MHz. [4 M]

2.

A. A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find, at the bias point, the value of transconductance,g_m; and the small signal resistances between base and emitter viz, the one looking into the base, r_e; and that looking into the emitter r_π. [4 M]

B. List the FIVE important steps in the systematic process of analyzing BJT transistor amplifier circuits employing small signal BJT circuit models. [5 M]

C. The emitter follower shown in figure is used to connect a source with $R_{sig} = 10$ KΩ to a load $R_L = 1$ KΩ. The transistor is biased at I = 5 mA, utilizes a resistance R_B=40 KΩ, and has β =100, Early Voltage (V_A) =100V.

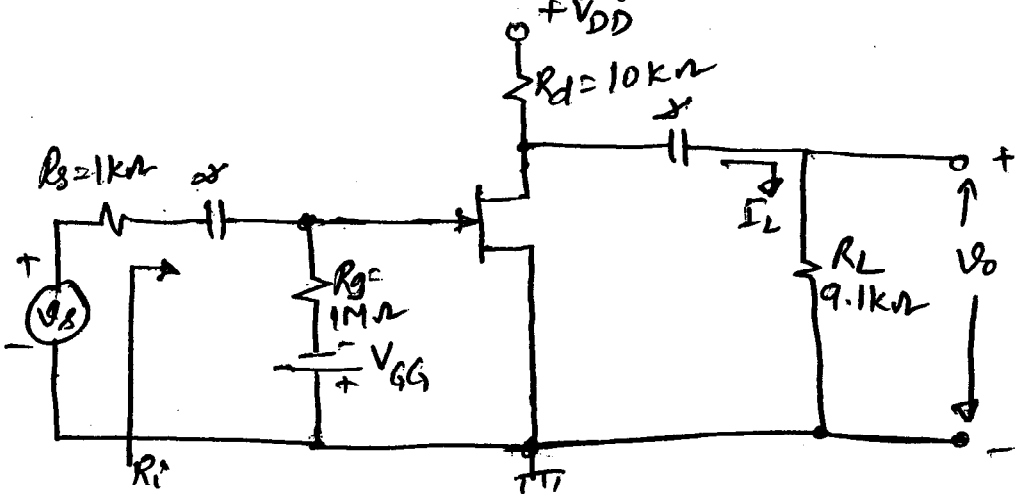


i. Find R_{ib}, R_{in}, G_v, G_{vo} and R_{out}. [5 M]
ii. What is the largest peak amplitude of an output sinusoid that can be used without the transistor cutting off? [2 M]
iii. If in order to limit nonlinear distortion the base-emitter signal voltage is limited to 10mV peak, what is the corresponding amplitude at the output? [2 M]
iv. What will the overall voltage gain become if R_L is changed to 2 KΩ to 500Ω? [2 M]

3.

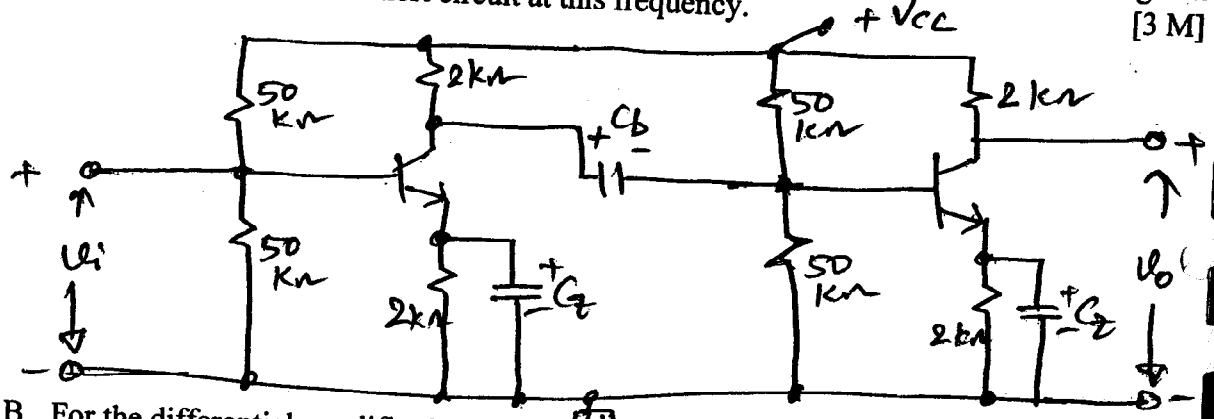
A. An amplifier with open-loop gain A_V=1,000±100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.1%.
   i. Find the reverse transmission factor β of the feedback network used [2 M]
   ii. Find the gain with feedback [2 M]

B. For the circuit shown below, assuming that g_m=5 mA/V and r_d=100 KΩ, find
   i. the Current gain, $A_I = I_L/I_s$;
   ii. the Voltage gain $A_V = V_o/V_s$;
   iii. Transconductance, $G_M = I_L/V_s$;
   iv. The Transresistance, $R_M = V_o/I_s$;
   v. the Input resistance seen by the source, R_i and
   vi. the Output resistance seen by the load, R_o. [6 M]

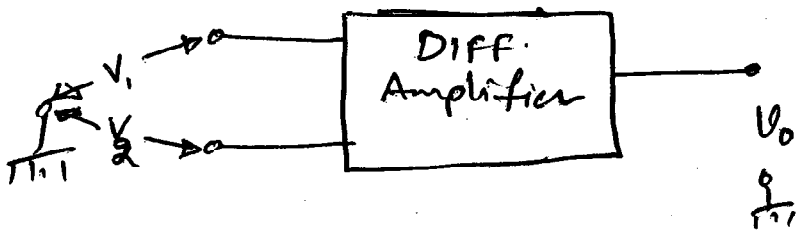


4.

A. The parameters of the transistors in the circuit shown below are h_{fe}=50; h_{ie}=1.1K, $h_{re}=h_{oe}$=0. Find
   i. the mid band gain, [2 M]
   ii. the value of C_b necessary to give a lower 3-dB frequency of 20 Hz assuming that C_z represents a short circuit at this frequency. [3 M]



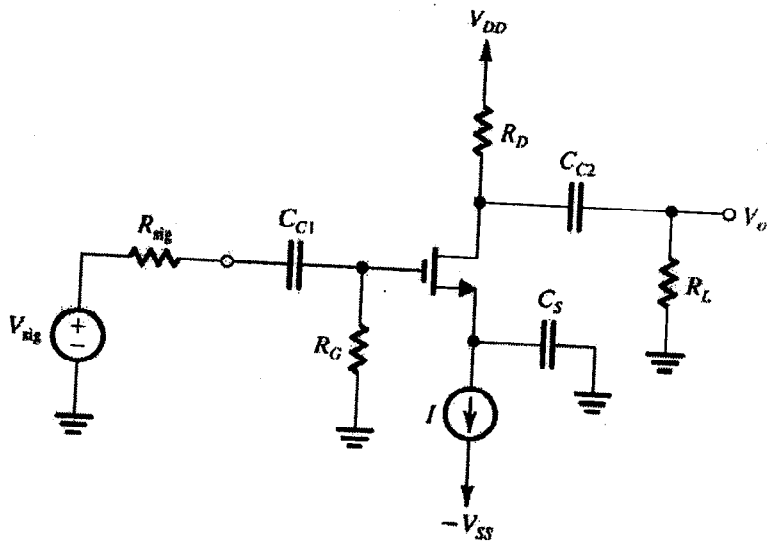
B. For the differential amplifier block shown below obtain an expression for the output in terms of its Differential gain A_d; differential and common mode voltages (v_d and v_c) and the CMRR, ρ. [5 M]



5.

A. Draw the MOSFET high frequency model indicating all its components using standa notation and derive an expression for the figure of merit (f_T) of MOSFET's hi frequency operation from fundamentals. [8 M

B. Consider a CS amplifier, shown below, which is fed with a signal source having a



internal resistance R_{sig}=100 KΩ. The amplifier has R_G=4.7 MΩ; R_D=R_L= 15KΩ; g_m = 1mA/V; r_o=150KΩ, C_{gs}=1pF and C_{gd}=0.4pF. Find

i. the mid band gain [3 M]
ii. upper 3-dB frequency f_H [3 M]
iii. both (i) and (ii) above if R_{sig} is reduced to 10 KΩ. [6 M]

6.

A. Draw the Circuit of a Class B push-pull output stage and prove, from fundamentals that, it offers a theoretical maximum conversion efficiency of 78.5%. Indicate the source of crossover distortion in Class B operation. [5 M]

B. Draw a neat sketch to depict the specification of the transmission characteristics of a Chebyshev low pass active filter both in terms of magnitude response and pole zero plot and list the four important parameters that aptly specify its magnitude response. Also enumerate the steps in designing the same meeting these specifications. [5 M]

7. Write Short notes on any TWO of the following: [10 M]

A. Issues in the design of Tuned amplifiers
B. Features and importance of multistage amplifiers employing compound devices
C. PSPICE as a tool in Electronic Design Analysis
D. Current Mirrors and Sources employed in IC Biasing

*********) ALL THE BEST (*********

BITS-Pilani Dubai Campus, Knowledge Village, Dubai

Evaluation Component : **TEST-II (Open Book)-Makeup**

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 23rd Nov. 2006

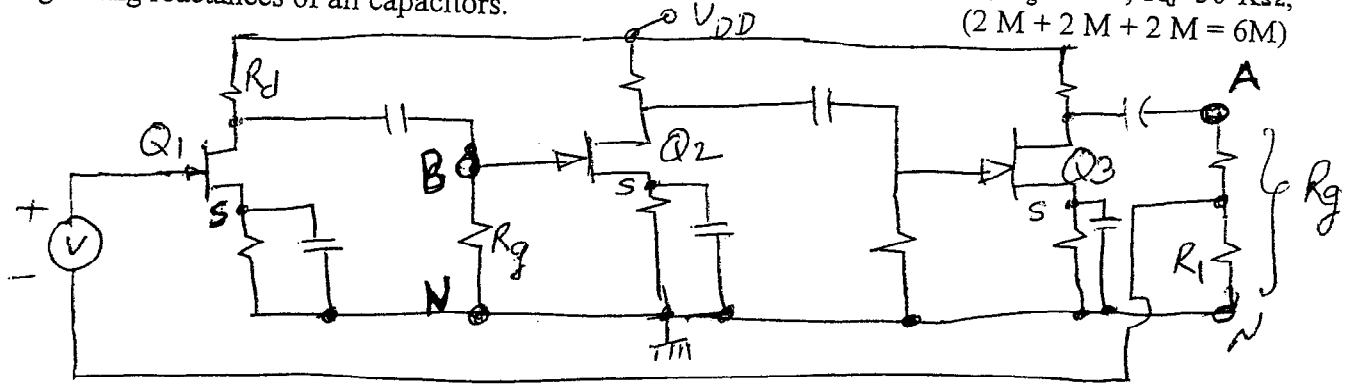
Duration: 50 mts **Max. Marks: 20**

Weightage: 20%

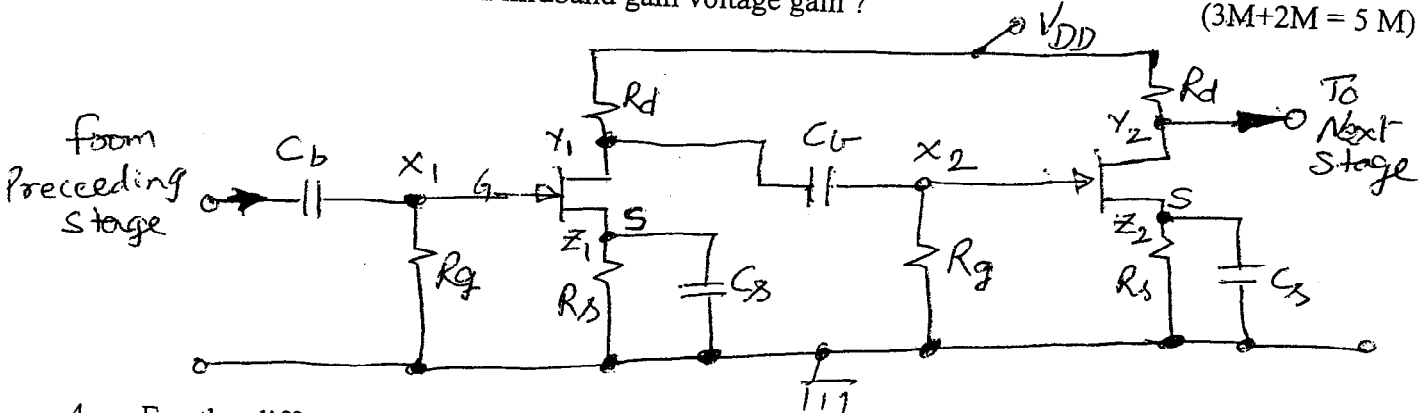
Note:- 1. ANSWER ALL QUESTIONS
2. Students are permitted to use their own blank graph sheets after taking signature of invigilator on it just before its usage
3. Make assumptions, if any, but explicitly indicate the assumptions made

1. An amplifier consists of three identical stages connected in cascade. The output voltage is sampled and returned to the input in series opposing. If it is specified that the relative change dA_f/A_f in the closed loop gain A_f must not exceed ψ_f, show that the minimum value of the open-loop gain A of the amplifier is given by $A = 3.A_f\,|\psi_1| / |\psi_f|$ where $|\psi_1| = dA_1/A_1$ is the relative change in the voltage gain of each stage of the amplifier (5 M)

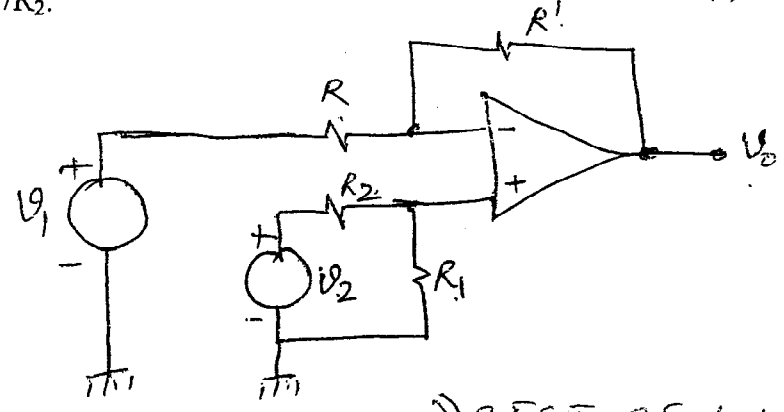
2. For the circuit shown below, Find the (A)Voltage gain and (B)output impedance at the terminals (i)AN and (ii)BN of the circuit assuming that g_m=6 mA/V and r_d=10 KΩ, R_g=1MΩ; R_d=50 KΩ, neglecting reactances of all capacitors. (2 M + 2 M + 2 M = 6M)



3. The FET RC coupled amplifier has the following parameters: g_m=10 mA/V and r_d=5.5 KΩ, R_g=10KΩ; R_g=0.5 KΩ for each stage. Assume C_s is arbitrarily large. (a) What must be the value of C_b in order that the frequency characteristic of each stage be flat within 1 dB down to 10 Hz.? (b) What is the overall midband gain voltage gain ? (3M+2M = 5 M)



4. For the differential amplifier using an ideal OP AMP block shown below (a) find the output voltage v_o. (b) Show that the output corresponding to the common-mode voltage $v_c = 0.5\,(v_1+v_2) = 0$ if $R'/R = R_1/R_2$. Find vo in this case. and (c)the CMRR, ρ of the amplifier if $R'/R \neq R_1/R_2$. (4M)



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BITS-Pilani Dubai Campus, Knowledge Village, Dubai

Evaluation Component : **TEST-II (Open Book)**

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 12th Nov. 2006 **Max. Marks: 20**

Duration: 50 mts **Weightage: 20%**

Note:- 1. ANSWER ALL QUESTIONS

2. Students are permitted to use their own blank graph sheets after taking signature of invigilator on it just before its usage

3. Make assumptions, if any, but explicitly indicate the assumptions made

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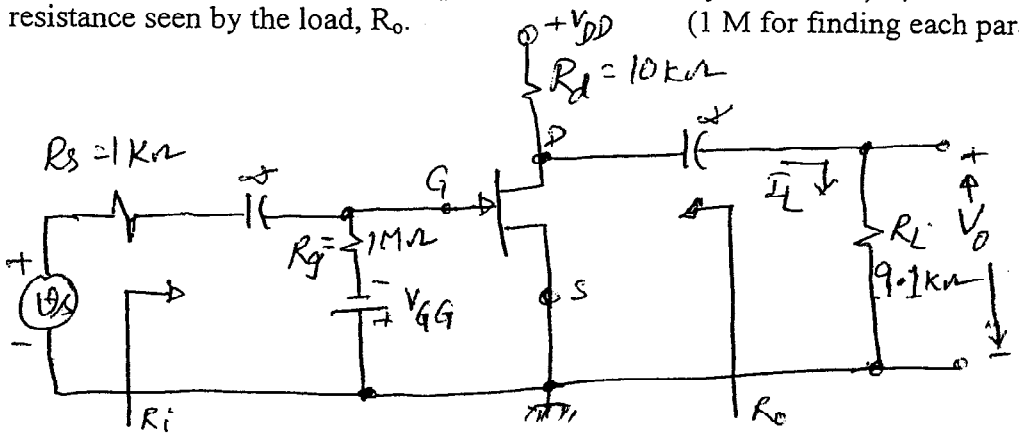
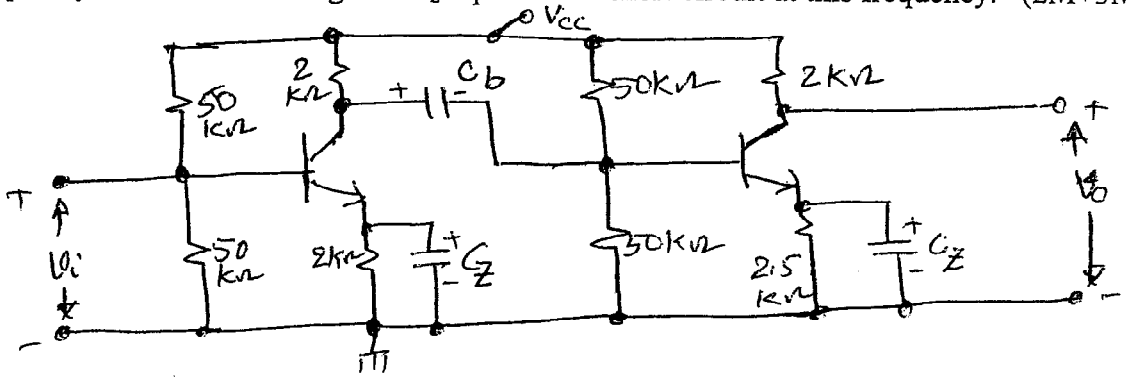
1. An amplifier with open-loop gain A_V=1,000±100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ±0.1%.
   A. Find the reverse transmission factor β of the feedback network used (2.5M)
   B. Find the gain with feedback (2.5M)

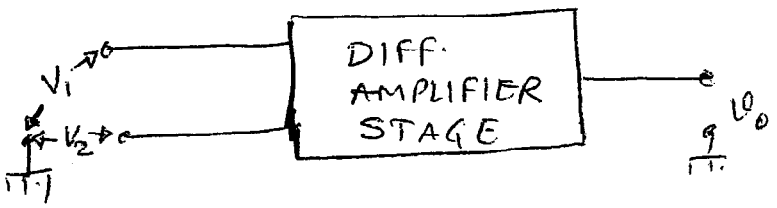
2. For the circuit shown assuming that g_m=5 mA/V and r_d=100 KΩ, find the Current gain, $A_I = I_L/I_s$; the Voltage gain $A_V = V_o/V_s$; Transconductance, $G_M = I_L/V_s$; The Transresistance, $R_M = V_o/I_s$; the Input resistance seen by the source, R_i and the Output resistance seen by the load, R_o. (1 M for finding each parameter= 6 M)



3. The parameters of the transistors in the circuit shown below are h_{fe}=50; h_{ie}=1.1K, $h_{re}=h_{oe}$=0. Find (a)the mid band gain, (b)the value of C_b necessary to give a lower 3-dB frequency of 20 Hz assuming that C_z represents a short circuit at this frequency. (2M+3M)



4. For the differential amplifier block shown below obtain an expression for the output in terms of its Differential gain A_d; differential and common mode voltages (v_d and v_c) and the CMRR, ρ. (4 M)



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Student Name: | A | BITS ID No.:

BITS-Pilani Dubai Campus, Knowledge Village, Dubai

Evaluation Component : **QUIZ-II**

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 02nd Nov. 2006
Duration: 30 mts

Max. Marks: 30
Weightage: 10%

Note:- 1.Respond ALL questions
2. Fill the blanks, show the working and / or indicate the **"most appropriate answer"** or **"most appropriate combination of Answers"** as required for each question.
2.Make your assumptions, if any, explicit

- - -

1. Expand the Acronym : IG FET _____
2. Consider the statement : "A 0.1 μm CMOS technology is being employed in several applications of consumer electronics." Here "0.1 μm" represents:_____
3. The Output characteristics of a FET can broadly be divided into three distinct regions of operation namely :
   1. _____ 2._____ and
   3._____
4. In order to obtain linear amplification, the MOSFET is biased to operate somewhere near the _____ of the _____ region of its characteristics.
5. A good bias design ensures that the parameters of the bias point namely _____ , _____ and _____ are predictable and stable.
6. An Alternate method of biasing instead of "fixing of V_{GS}" of a FET in amplifier applications is by the use of a Resistance in the Source. This resistance is called _____
7. Other than the use of two bias methods namely "fixing of V_{GS}" OR "use of R_S" list / indicate two other techniques of BIASING an FET
   1._____
   2._____
8. The Fourth terminal brought out by almost every manufacturer other than Source(S), Drain (D) and Gate(G) of a FET is designated in the manufacturer's data sheets as the _____or the _____ terminal.
9. A Depletion type MOSFET can be operated in both "Enhancement Mode" and "Depletion Mode". State whether this statement is TRUE of FALSE. _____.
10. Process transconductance parameter determined by the process technology used to fabricate an NMOS can be expressed as _____ and is designated as _____
11. The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region is called _____ and the region is called the _____
12. When biased in _____ Region of an NMOS device, it can be used as an Amplifier and the Characteristic i_D - V_{DS} relationship is expressed as :

13. Draw the Large-Signal Equivalent-Circuit Model of an NMOS device operating in saturation region that can be employed to analyze a practical circuit. Indicate all components of the equivalent circuit and the significant voltages and currents with most appropriate symbol notation.

14. The relationship between v_{GS}, V_t and v_{DS} to operate an NMOS device in saturation region is

_____

15. In Integrated circuits to maintain a constant zero bias in all the substrate to channel junctions, the substrate is usually connected to the most negative Power Supply in an _____(NMOS /PMOS) and the most positive in a _____ (NMOS / PMOS) circuit.
16. As the voltage on the drain is increased, a value is reached at which the pn junction between the drain region and the substrate suffers _____ Breakdown (known also as Punch through) and it occurs at voltages ranging from _____ V to _____ V.

17. Draw the circuit symbol of NMOS and PMOS transistors.

(i)Circuit symbol of NMOS: (ii)Circuit Symbol of PMOS:

18. Match the following process parameters shown under I with their dimensions / units shown under II …by indicating the serial no. of I in the braces: "[ ]" of II.

I	II	
A. C_{ox}	$V^{-1/2}$	[ ]
B. K'_n	V/m	[ ]
C. V'_A	F/m^2	[ ]
D. λ	A/m^2	[ ]
E. γ	V^{-1}	[ ]

19. The characteristic equation representing the "load line" of a CS Amplifier can be mathematically expressed as a relationship between i_D, V_{DD}, R_D and v_{DS} and it is given by:

20. In the following two non-linear transistor biasing circuits, the resistors R_A and R_B are suitably employed to provide appropriate compensation against Bias Point drift, then, choose and indicate the most appropriate choice of the nature of resistors : [ ]
    A. R_A and R_B, both have negative temperature coefficient
    B. R_A and R_B, both have positive temperature coefficient
    C. R_A has negative temperature coefficient and R_B has positive temperature coefficient
    D. R_A has positive temperature coefficient and R_B has negative temperature coefficient

21. The Gain Bandwidth product of an FET amplifier is _____
22. In the MOSFET shown below, the signal outputs V_1 and V_2 obey the relationship [ ]

    A. $V_1=V_2/2$
    B. $V_1=-(V_2/2)$
    C. $V_1=2V_2$
    D. $V_1= -2V_2$

23. A two stage amplifier is required to have an upper cut off frequency of 2 MHz and a lower cutoff frequency of 30 Hz. The upper and lower cutoff frequencies of the individual, but identical, stages are
    A. 4 MHz, 60 Hz [ ]
    B. 3 MHz, 20 Hz
    C. 3 MHz, 60 Hz
    D. 4 MHz, 20 Hz
24. The threshold voltage of an n-channel MOSFET can be increased by [ ]
    A. Increasing the channel doping concentration
    B. Reducing the channel length
    C. Reducing the gate oxide thickness
    D. Decreasing the channel doping concentration
25. A source follower using an FET usually has a voltage gain which is [ ]
    A. greater than +100
    B. slightly less than unity but positive
    C. exactly unity but negative
    D. about -10

26. The MOSFET if designed to operate as an "electronic switch", in its own state may be considered equivalent to
    A. Resistor
    B. Inductor
    C. Capacitor [ ]
    D. Battery

27. A properly biased JFET will act as a [ ]
    A. Current controlled current source
    B. Voltage controlled voltage source
    C. Voltage controlled current source
    D. Current controlled voltage source

28. When source terminal is not connected to the body terminal of a FET, the expression for body transconductance g_{mb}, involves a parameter "χ" . Employing it, g_m and g_{mb} are related as _____. The Expression for "χ" = _____ and typically it varies in the range from _____ to _____ .

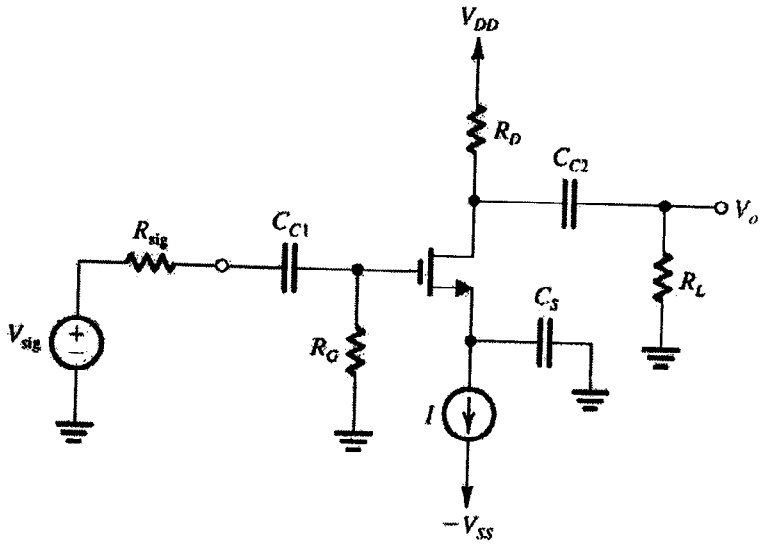
29. The figure of merit of an amplifier "f_T" of an FET can be expressed as :

    f_T = _____

    The physical significance of f_T of an FET w.r.t. its use in the _____ FET model in designing of amplifiers is:

    _____

30. The mid band voltage gain of the amplifier shown below is _____ if R_{sig} = 100 kΩ; R_G = 4.7MΩ; R_D=R_L=15kΩ; g_m=1mA /V and r_o=150kΩ;



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*********) ALL THE BEST (*********

BITS, Pilani – Dubai Campus, Knowledge Village, Dubai

Academic Year 2006-2007 III B.E.(Hons.) I Semester – EEE & EIE

Course No. EEE UC 424 / INSTR UC 313 Microelectronic Circuits

Test-1 (Make-up) – Closed Book

Date : 12-10-2006
Duration : 50 mts.

Max. Marks : 20
Weightage : 20%

Note :- 1. Answer ALL Questions
2. Indicate explicitly the assumptions, if any, made by you.

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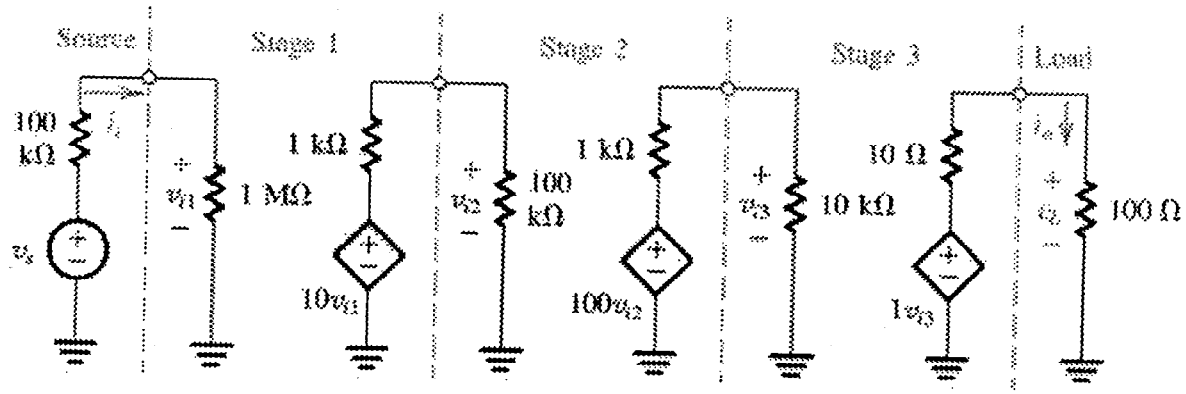
1) Consider a transistor amplifier with its transfer characteristics defined as: $v_O=10-10^{-11}e^{40v_I}$ which applies for $v_I>0V$ and $v_o>0.3V$. Find the value of the dc bias voltage V_I that results in $V_O = 5V$ and the voltage gain at the corresponding that operating point. Assuming that, to this amplifier a positive input signal of 1mV superimposed on the dc bias voltage (v_I) has been applied, find the corresponding signal at the output for the following two situations, assuming:

A. the amplifier is linear around the operating point;
B. the applied input signal is (i)5 mV and (ii)10 mV (1+1+1+2= 5 Marks)

2) Model the 3-stage amplifier shown below (without the source and load) using the voltage amplifier model. What are the values of the input resistance (R_i), open circuit voltage gain (A_{vo}) and the output resistance (R_o). If R_L varies in the range 10Ω to 1000Ω, find the corresponding range of overall voltage gain (v_o/v_s). (1+1+1+2 =5 Marks)



3) A pnp BJT is biased to operate at I_C=2.0mA What is the associated value of g_m ? If β=50, what is the value of the small signal resistance seen looking into the emitter (r_e)? Into the base (r_π)? If the collector is connected to 5kΩ load with a signal of 5-mV peak applied between base and emitter, what output signal voltage results? (1+1+1+1 = 4 Marks)

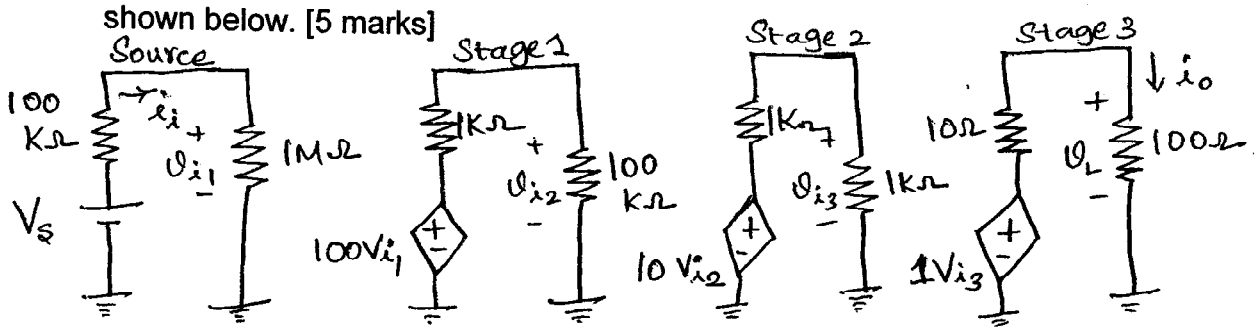
4) An amplifier is measured to have R_i=10KΩ, A_{vo}=100, and R_o=100Ω. Also, when a load resistance R_L of 1 KΩ is connected between the output terminals, the input resistance is found to decrease to 8 KΩ. If the amplifier is fed with a signal source having an internal resistance of 2kΩ, find Short circuit transconductance (G_m), Voltage Gain (A_v), Open circuit-overall voltage gain (G_{vo}), Overall Voltage gain (G_v), Output Resistance (R_{out}) and Current gain (A_i)
(1+1+1+1+1+1=6Marks)

=====)B E S T OF L U C K(=====

BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
FIRST SEMESTER 2006 – 2007
EEEUC424 MICRO ELECTRONIC CIRCUITS
TEST 1(CLOSED BOOK)

MAXIMUM MARKS: 20 **WEIGHTAGE: 20%**
DATE: 01/10/06 **DURATION: 50 MINUTES**

1. Evaluate the overall gain, current gain and power gain of the amplifier shown below. [5 marks]



2. (a) Draw the equivalent circuit of a common emitter amplifier with a resistance in the emitter. [1 mark]
   (b) Derive the expressions for R_i, A_v, R_o and A_i. [4 marks]

3. A common base amplifier biased at an emitter current of 3mA employs a base resistor R_B=2KΩ ohm with R_c= 3KΩ, R_E=3KΩ and R_L = 1KΩ. For β=150, what is the input resistance. What is the voltage gain from a 100 Ω source? [5 marks]

4. Analyze the circuit shown below to find all node voltages and branch currents. Assume that β is specified to be 50. [5 marks]