BITS PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester I 2006– 2007
COMPREHENSIVE EXAMINATION (Closed Book)

Course No.: **CS UC 391 / EIE UC 391** Course Title: **DECO**

Date: 18th December, 2006 Time: 3 hrs Max. Marks = 80

Clearly indicate the assumptions made if any
Answer questions Part A and Part B separately
All questions carry equal marks

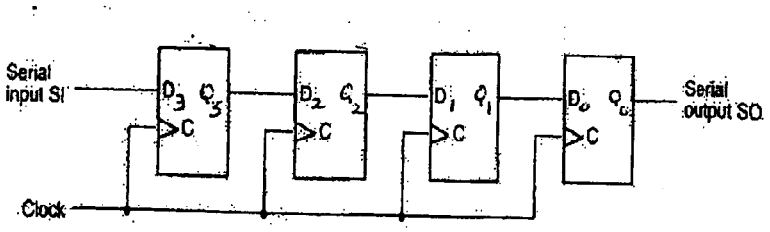
PART A

1. In what follows, we want to implement the function $f(x) = x^2 - 1$ for three-bit integer inputs. Read the instructions carefully and answer each part separately:

   a. For the inputs, we want to use three bit-signed numbers $(a_2,a_1,a_0)_2$. Give all signed integer numbers that can be represented using three bits, assuming that 2's complement is used for representing negative numbers (5M)
   b. Plug in all the numbers represented in 1(a) into $f(x) = x^2 - 1$. What is the smallest number ? What is the largest number? (3M)
   c. Based on your result in 1(b), how many bits do we need in order to represent the result? For your answer, assume that we are using two's complement for representing negative numbers (2M)

2. i) Use only one 3 X 8 decoder and 3 OR gates to realize the following functions
   $F(A,B,C) = A(B+C) + A'B'$
   $G(A,B,C) = \sum (0,1,4,5,7)$
   $H(A,B,C) = ABC + A'B'$
   (5M)

   ii) The digital logic circuit below represents a 4 bit shift register. Indicate how to load binary 5 into the register. Show the clock input, and all the affected inputs and outputs



(5M)

3. Using T flip flops, design a binary counter that counts through the 3 bit binary numbers: 000, 001, 010, 100 and then repeat from 000. Assume that there is a reset signal that will force counting to start to 000.
   a. Derive the state table for implementing the counter (6M)
   b. Use K maps to minimize the inputs (3M)
   c. Indicate the final circuit (1M)

4. Answer any two of the following three questions
   a) Write short notes on I/O data transfer schemes
   b) Multiplication of binary numbers are performed in the same way as in decimal numbers. Draw a binary multiplier to perform 3-bit by 2- bit multiplication and explain.
   c) Distinguish between ring counter and switch tail ring counter with an example and draw the waveforms (Assume three bit counter)

PART B

5. Given F (w, x, y, z) = Σ (0,2,3,5,6,7,8) and d (w, x, y, z) = 10,11,12,13,14 & 15
   Using K-Map,
   a) Identify the Prime Implicants
   b) Identify the Essential Prime Implicants
   c) Find the reduced expression in the SOP form
   d) Implement the function using NAND gates alone

6. List the PLA programming table for the full adder circuit. Optimize the no. of product terms for true or complimentary outputs.

7. A sequential circuit has two JK flip flops A and B, two inputs x and y and one output z. The flip flop input equations are given $J_A = B\,x$; $K_A = B'\,x\,y'$
   $J_B = A'x$; $K_B = A + xy'$; $z = A\,x'y'$;
   a) Draw the circuit diagram
   b) Write the State table
   c) Draw the state diagram

8. Answer any two of the following three questions
   a. With a neat circuit diagram, Explain the principle of operation of a TTL NAND gate with Totem-Pole output
   b. Derive the expressions for carry generate and carry propagate for a 4-bit serial adder
   c. Draw the logic diagram of the digital circuit specified by the following HDL description:

```
module circt (A,B,C,D,F);
input A,B,C,D;
output F;
wire w,x,y,z,a,d;
and (x,B,C,d);
and (y,a,C);
and (w,z,B);
or (z,y,A);
or (F,x,w);
not (a,A);
not (d,D);
endmodule
```

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Year III Sem I 2006 - 2007

Test 2 (Open Book)

Course No: CS UC 391 / INSTR UC 391 Course Title: DECO

Date: 04 Dec 2006 Time: 50 min Max Marks: 40

Note:

1. **Answer all questions**
2. **All questions carry equal marks**
3. **Only text book (Morris Mano) and handwritten notes are allowed. Photocopies are not allowed**

1. Design a binary counter that counts through prime numbers less than 10. This means that your counter is to count : 1, 2, 3, 5, 7 and then go back to 1. For your design assume there is no reset signal and you are thus forced to send any of the states 0, 4, 6 back to 1

a. Derive the state table for implementing using D flip flops
b. Use K maps to minimize the inputs
c. Draw the final circuit.

2. Draw the logic diagram of a 4 bit register with four D flip flops and four 4 X 1 multiplexers with mode selection inputs S1 and S0. The register operates according to the following function table:

S1	S0	Register operation
0	0	Load parallel data
0	1	Complement the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	No change

3. An application of PROM is to realize look up tables for arithmetic functions. Using a PROM of appropriate size, it is required to realize the expression:

$f(x) = 3x + 2$ for $0 \leq x \leq 7$.

Draw the ROM truth table and program the ROM.

4. For the circuit shown in figure 1(a) assuming that all flip flops are cleared initially, sketch the D_{out} and F_{out} for the input combination applied as shown in figure 1(b).

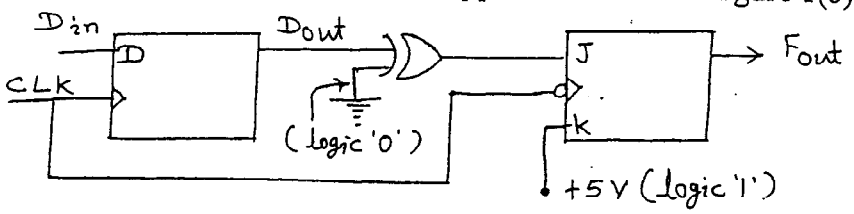

Figure 1 (a)

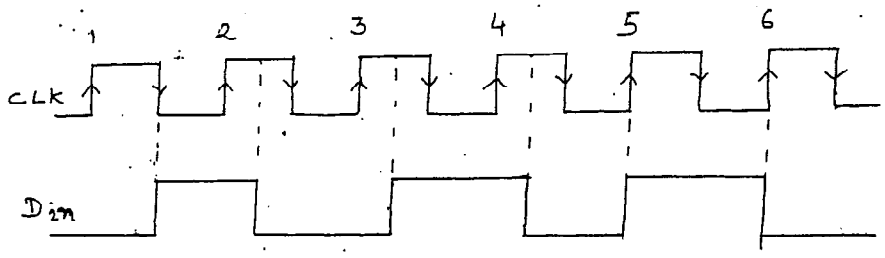

Figure 1 (b)

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Knowledge Village, Dubai
Year III – Semester I 2006 – 2007
Test I (Closed Book)

Course No.: CS UC 391/ INSTR UC 391 Course Title: DECO

Date: October 30, 2006 Time: 50 Minutes Max. Marks = 40

1. (a) Prove the identity: xy+x'y'+yz = xy +x'y'+x'z

   (b) Simplify the following expression: (x+y)[x'(y'+z')]' + x'y' +x'z' (3 + 3)

2. Draw the truth table of a full subtractor and design the circuit for the Difference and the Borrow using NAND gates alone. Assume complimented inputs are also available. (6)

3. Write the Boolean expression and Explain the design of two 4-bit word comparator circuit which will give the outputs as AEB for A=B, AGTB for A>B and ALTB for A<B. (5)

4. Implement the following Boolean function F together with the don't care conditions d, using no more than two NOR gates.
   $F(A,B,C,D) = \prod(3,4,5,6,7,12,13)$: $d(A,B,C,D) = \prod(8,10,14,15)$
   (Assume that both the normal and complement inputs are available) (5)

5. Implement the following Boolean function F, using the two-level forms
   a) OR – NAND b) NOR – OR :
   $F(A,B,C,D) = \Sigma(0,1,2,3,4,8,10,12)$ (6)

6. Implement the following Boolean function using a 8 x1 Multiplexer (5)
   $F(A, B, C, D,) = \Sigma(0, 1, 3, 4, 5, 7, 10, 12)$

7. A combinational circuit is specified by the following three Boolean functions
   $F_1(A,B,C) = \Sigma(2,4,7)$; $F_2(A,B,C) = \Sigma(0,3)$; $F_3(A,B,C) = \Sigma(0,2,3,4,7)$
   Implement the circuit using a decoder (constructed with NAND gates) and NAND gates or AND gate connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates. (7)

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