Id No	Name

BITS, PILANI – DUBAI CAMPUS, KNOWLEDGE VILLAGE, DUBAI
FIRST SEMESTER 2006 – 2007
ESUC364 ANALOG ELECTRONICS
LAB QUIZ (CLOSED BOOK)

MAXIMUM MARKS: 15 **WEIGHTAGE: 10%**
DATE: 12/12/06 **SET I** **DURATION: 30 MINUTES**

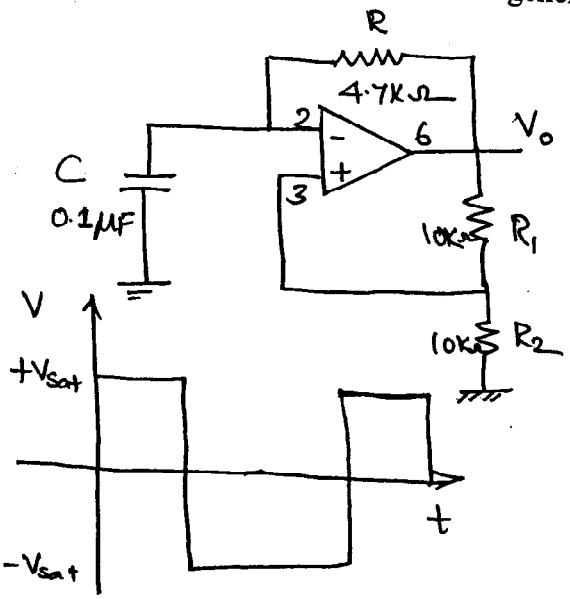
1. Draw the transfer characteristics of a negative half wave rectifier using Op-amp. [1 mark]

2. For a particular phase shift oscillator the following specifications are given C=0.1 μF, R=3.9Ω and RF/R1=29. Determine the frequency of oscillation.[2 marks]

3. Negative feedback increases the ---------- impedence of a non – inverting amplifier. [1mark]
   (a) input
   (b) output
   (c) input & output
   (d) None of the above

4. Diodes can be used as [1 mark]
   (a) an amplifying device
   (b) a rectifying device
   (c) Both (a) & (b)

5. Modify the given circuit to generate the following waveform [3 marks]



6. Op- amps with low slew rate are used in clipping circuit (True/False) [1mark]

7. For an amplifier having a slewrate of 60V/ μs, what is the highest frequency at which a 20V peak to peak sine wave can be produced at the output?[2mark]

8. An ideal power supply will have voltage regulation equal to _____[1 mark]

9. The capture range is always ___ _____than the lock range. [1 mark]

10. What is the relation between phase of the output signal & signal at base in CE configuration amplifier ? [1 mark]

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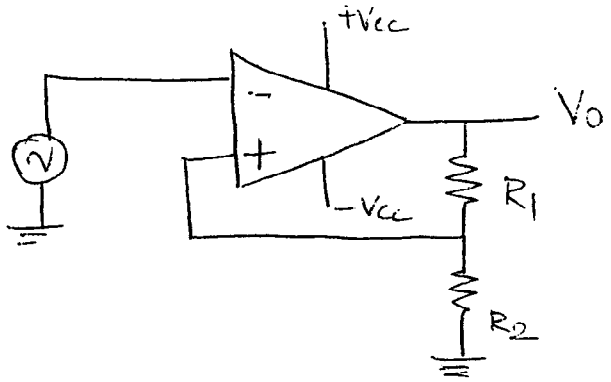
ESUC364 ANALOG ELECTRONICS
TEST 2(OPEN BOOK)

MAXIMUM MARKS: 20 WEIGHTAGE: 10%
DATE: 04/12/06 DURATION: 50 MINUTES

1. For the schmit trigger circuit shown in figure, calculate the ratio of R1 & R2 , if saturation voltages are +12V & -12 V. Assume hysteresis width = 6v. [5 marks]



2. If the free running frequency is 100 KHz. Supply voltage is ±6V. Demodulation capacitor is 1μF. Find out the lock and capture frequencies and range of PLL employing LM565. Design components of this PLL for given free running frequency. [5 marks]

3. Design the astable multi – vibrator to generate the output signal with frequency of 1 KHz and duty cycle of 75%. [5marks]

4. Design the voltage regulator using IC723 to meet the following specifications, V_0 = 5v, I_0 = 100 mA, V_{in} = 15 ± 20 %, I_{sc} = 150 mA, V_{ref} = 0.7V. [5 marks]

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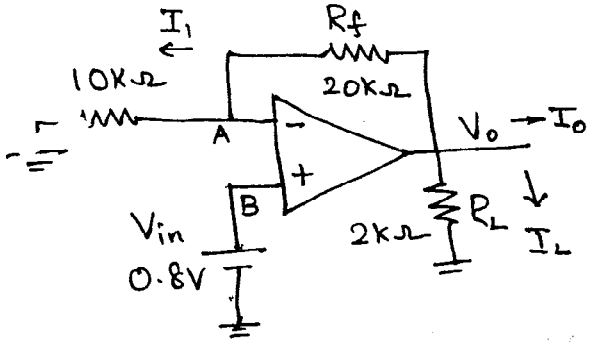
ES UC 364 ANALOG ELECTRONICS
COMPREHENSIVE EXAMINATION

MAXIMUM MARKS: 90 WEIGHTAGE: 30%
DATE: 18.12.06 DURATION: 3 HOURS

Answer all the questions

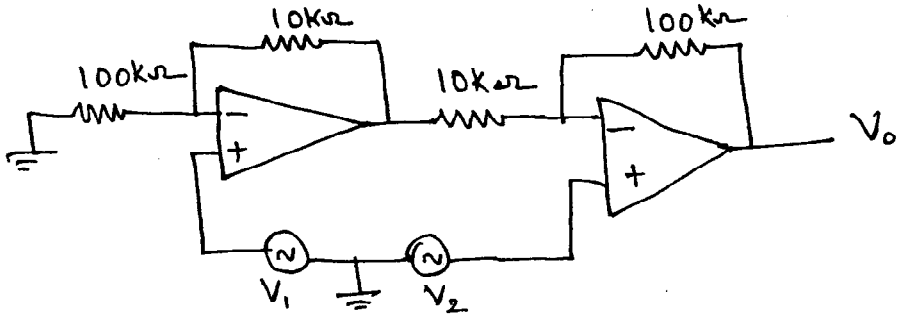
1. (a) Design the op-amp circuit which can give the output as $V_0 = 2V_1-3V_2+4V_3-5V_4$. (5MARKS)

   (b) For an inverting amplifier shown in figure calculate I_L&I_0. (5MARKS)

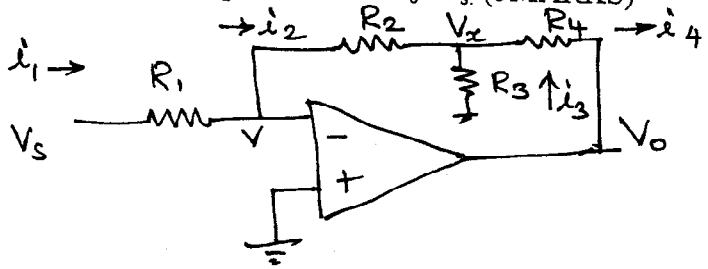


   (c) Draw the circuit diagram for inductance simulation and derive the expression for Q of the inductor. (5MARKS)

2. (a)Find the output voltage V_0 in terms of V_1 and V_2 for the op-amp circuit shown in figure. (5 MARKS)



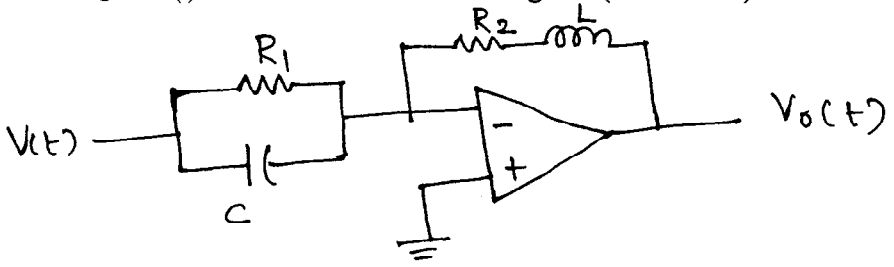
   (b) Derive the expression for V_0 /V_s. (5MARKS)



(c) Draw the circuit diagram for first order low pass butter worth filter and design low pass filter at a cut off frequency of 15.9 kHz with a pass band gain 1.5. Choose C=0.01μF. (5MARKS)

3. (a) Draw the negative clamper circuit and explain its working principle.(5 Marks)

(b) Derive the expression in the form of a differential equation for the output voltage $V_{0(t)}$ of the circuit shown in figure. (5MARKS)



(c) Design second order butter worth filter at cut off frequency of 1 KHz . Choose C=0.1 μF& A_F = 1.586. (5 MARKS)

4. (a) Design astable multi vibrator IC555 which will flash the electric bulb such that is ON time will be 3 seconds and off time will be 1 second. Choose C= 0.1μF.

(b) Draw the circuit for log amplifier realization and derive the expression for V_0. (5MARKS)

(c) Draw the phase shift oscillator and design a phase shift oscillator to oscillate to 500 Hz. Supply voltage ± 11Volts and current I1 = 5 μA. (5MARKS)

5. (a) Design a frequency multiplier circuit using PLL IC565 to multiply frequency by 5 center frequency by 50 KHz and power supply is ± 10V d.c. Find the lock and center frequency output and state related tracking range & capture range limits for input.(5 Marks)

(b) Draw the circuit diagram for fold back current limiting and design the regulator using IC723 to meet the following specifications V_0 = 6V, I_0 = 100 mA, V_{in} = 15±20%, Isc= 150 mA, Vsense=0.7V, Vref = 7v, I_D= 1 m.A. (5MARKS)

(c) (i) With neat sketch explain briefly about ultra sonic sensors. (2.5 MARKS)
(ii) With neat circuit diagram and gain table explain about programmable gain amplifier. (2.5 Marks)

6. (a) Explain the working principle for class B amplifier with its circuit and design class B amplifier which output voltage to deliver average power = 10W to 8 Ω load. Power supplies to be selected such that Vcc above 5volts >Vpeak. Determine supply voltage required and power conversion efficiency. (5 Marks)

(b) Design tuned amplifier having center frequency 1Mhz, bandwidth = 10KHz, center frequency gain = -9, FET available has bias point g_m = 6 mA/v & r_0 = 10 Kohm. C_0 is very small. Determine R_L, C_L, L. (5 Marks)

(c) A dual slope analog to digital converter uses a 8 bit counter and a 3 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8V. When the counter cycled through two's counts, the capacitor used in the integrator is 0.1 μF. Find the value of R of the integrator. (5MARKS).

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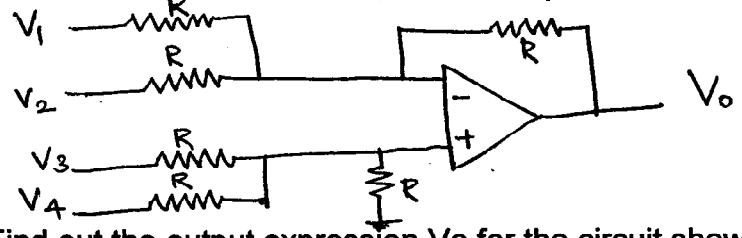
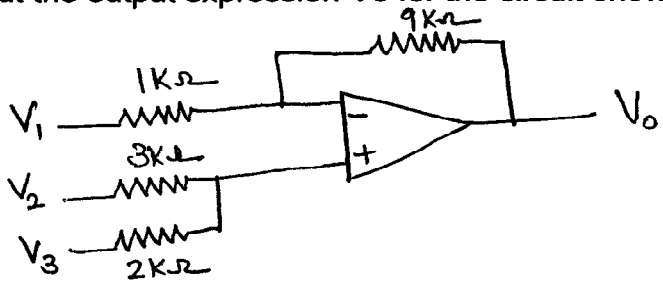
FIRST SEMESTER 2006 – 2007
ESUC364 ANALOG ELECTRONICS
TEST 1(CLOSED BOOK)

MAXIMUM MARKS: 20 **WEIGHTAGE: 10%**
DATE: 30/10/06 **DURATION: 50 MINUTES**

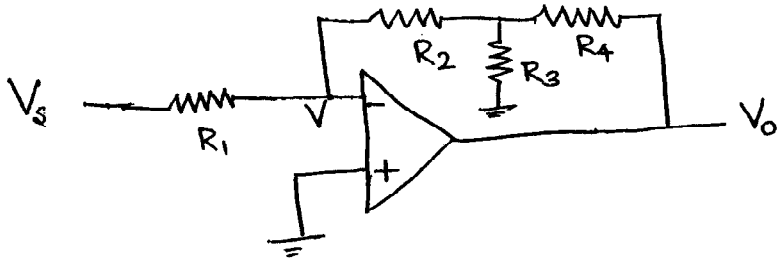
1. (a) For the circuit shown below, find the expression for Vo. [2.5 marks]



1. (b) Find out the output expression Vo for the circuit shown below.[2.5 marks]

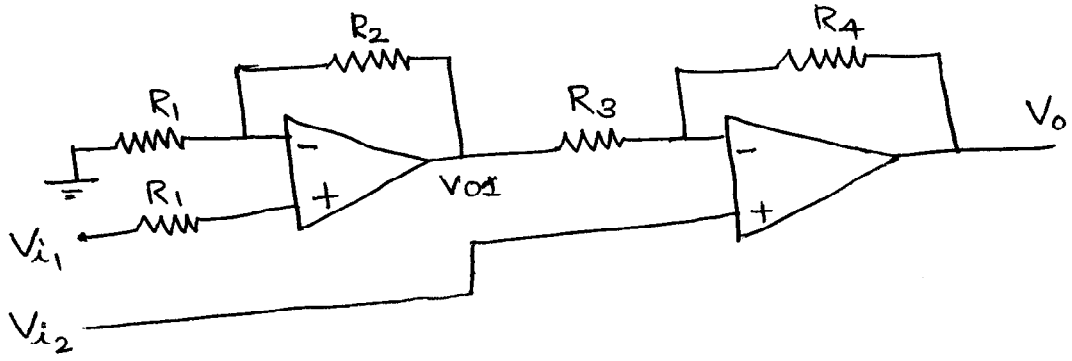


2. Find the output expression Vo for the circuit shown below. [5 marks]



3. Draw the bridge amplifier circuit and derive the output expression for the circuit. [5 marks]

4. For the circuit shown below, find the expression for Vo. [5 marks]



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ESUC364 ANALOG ELECTRONICS
QUIZ 1(CLOSED BOOK)

MAXIMUM MARKS: 10 **WEIGHTAGE: 5%**
DATE: 12.10.06 **SET I** **DURATION: 30 MINUTES**

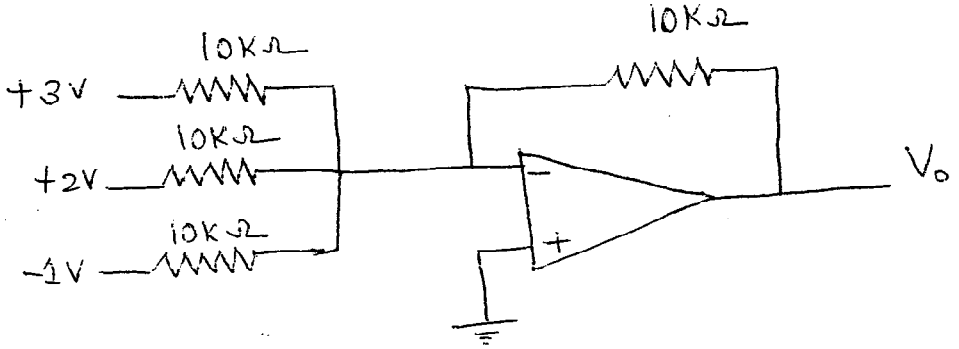
1. Draw the symbol of an Instrumentation amplifier.

2. Define CMRR in OPAMP.

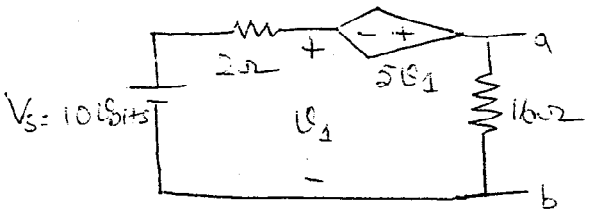
3. Draw the inverting integrator circuit using OPAMP and write the expression for output voltage.

4. Define Slew rate.

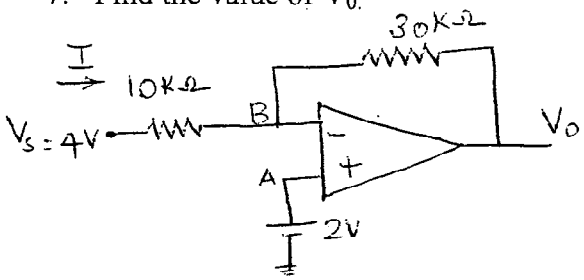
5. Find out the output voltage Vo.



6. Find the open circuit voltage across terminals a and b.



7. Find the value of V_0.



8. Draw the circuit diagram of current controlled voltage source using OPAMP.

9. Draw the symbol of an isolation amplifier.

10. Draw the voltage follower circuit and write the expression for the output voltage.