BITS, Pilani – Dubai Campus, Knowledge Village, Dubai

III B.E.(Hons.) I Semester – EEE & EIE

Course No. ~~EEE UC~~ 424 / INSTR UC 313 Microelectronic Circuits

Comprehensive Examination – Closed Book (MAKE UP)

Date : - -2006 **Max. Marks : 80**

Duration : 3 hours. **Weightage : 40%**

Note :- 1.**Answering of Question No.1 is Compulsory**
2.**Answer ANY SIX from the remaining Questions**
3.Make your Assumptions, if any, explicit
4.Students can answer in their own unused Semi-Log./ Ordinary Graph sheets, only after obtaining invigilator's signature (with date) on it as an endorsement that it is empty before its use by the student concerned during the examination.

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1)

a) A BJT is specified to have T_{Jmax} = 150°C and to be capable of dissipating maximum power as follows : 40 W at T_C = 150°C; 20 W at T_A= 25°C; Above 25 °C, the maximum power dissipation is to be de-rated linearly with θ_{JC}=3.12°C/W and θ_{JA}=64.5°C/W. Find the maximum power dissipated safely by this transistor when operated at T_A= 50°C (i) using an infinite heat sink. (ii)with a heat sink for which θ_{CS}=0.5°C/W and θ_{SA}= 4°C/W (3 Marks)

b) It is required to design the circuit shown in figure below to establish a dc drain current I_D = 0.5mA. The MOSFET is specified to have V_t=1V and k'_nW/L = 1 mA/V^2. Employ a power supply V_{DD}=15V. Also compute the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same k'_nW/L but V_t=1.5V (3 Marks)

c) Compare "the NMOS" and "the n-p-n" Transistors in respect of (i)Circuit symbol (ii)the conditions (in terms of equations to be satisfied) under which each act as Amplifier (iii)Low Frequency hybrid Model (iv)High Frequency Model and (v)the Design Parameters(5 Marks)

d) Obtain an expression for the output voltage v_o of a typical Differential amplifier in terms of its C.M.R.R., common mode gain and Differential Mode gain . (2 Marks)

e) Explain the steps and the way to arrive at "A" circuit and "β" circuit of a typical feedback amplifier in which a Voltage Shunt Feedback Amplifier. (2Marks)

f) Design a MOSFET based Tuned Amplifier having f_o=1MHz, 3-dB Bandwidth =10KHz, and center frequency gain = -10 V/V. The FET available has g_m = 5mA/V; and r_o = 10 KΩ. (5 Marks)

2)

a) Given the following BJT measurements made at I_C=5mA, V_{CE} = 10V and at room temperature (27°C) : h_{fe} = 100, h_{ie} = 600Ω, $|A_{ic}|$ =10 at 10 MHz, $C_{b'c}$=3pF. Find f_β, f_T, $C_{b'e}$, $r_{b'e}$, and $r_{bb'}$. (5 Marks)

b) A MOSFET CS amplifier has R_{in}=2 MΩ, g_m=4 mA, r_o=100kΩ, R_D=10kΩ, C_{gs}=2pF, and C_{gd} = 0.5pF. The amplifier is fed from a voltage source with an internal resistance of 500 kΩ and is connected to a 10-kΩ load. Find (a)the overall mid band gain A_M and (b)the upper 3-dB frequency f_H. (2.5 + 2.5 = 5 Marks)

P.T.O

3)

a) A CE amplifier using npn BJT having R_C = 10KΩ is supplied with an ac signal from generator of 1KΩ resistance. A Resistance R_f = 100KΩ connected from its collector to the base provides necessary negative feedback. (A)Identify the feedback topology whether it is current shunt / voltage shunt / voltage series / current series and justify your identification with pure conceptual explanation – no equations please. (B) Analyze the feedback amplifier to obtain (i)its transfer gain (ii)Voltage gain, V_o/V_s and (iii) Input resistance (all the three parameters with feedback) (1+2 +2+2=7Marks)

b) A three-pole amplifier without feedback has a dc gain of -10^3 and poles located at f_1 = 1MHz, f_2 = 10 MHz and f_3 =30MHz. Dominant pole compensation is applied to this amplifier. (a)Find the location of the dominant pole so that the open-loop gain is first constant and then falls to 0dB at a rate of -20dB per decade for frequencies f ≤ 1MHz. Also find the maximum value of β for which this compensated amplifier is stable. Use Bode plot (2 + 1 = 3 Marks)

4) Sketch the Ideal Transmission Characteristics of the four major filter types and discuss typical specifications, features, steps to design and a performance comparison of Low pass filter realization employing Chebyshev Transfer function vis-a-vis Butterworth Transfer function. (2+2+2+2+2=10 Marks)

5) Using a neat Sketch of the circuit of a class B Push Pull Output Stage, explain its operation and analyze quantitatively to show that the total harmonic distortion is significantly reduced as compared to a Class A Output Stage. Also illustrate how cross over distortion results in a typical class B Stage. (2+2+4+2 = 10 Marks)

6) It is desired to have Butterworth transfer function that meets the low pass filter specifications: f_p=10KHz, A_{max}=1dB, f_s=15KHz, A_{min}=25dB and dc gain =1. Obtain the Chebyshev transfer function that meets the same specifications. Also sketch the Chebyshev transmission characteristics & associated Butterworth pole zero pattern. (3+3+2+2)

7) Draw the Circuit of a BJT Differential amplifier employing silicon npn transistors biased by a non-ideal current source (as in a practical current mirror). Employing h-parameter model of a BJT, Analyze and obtain an expression for its common mode gain, A_c and differential mode gain, A_d. (2+4+4 Marks)

8) Draw the internal circuit diagram of an IC OPAMP 741. Identify the basic four functional stages it consists of and describe analysis methods to arrive at the features of each functional stage. (4+2+4=10 Marks)

9) Write a Short Notes on any TWO of the following: (5 x 2= 10 Marks)
   a) Current Mirrors and Current Sources
   b) Sources of Instability & Methods to tackle stability related issues in Feedback Amplifiers
   c) A Comparison of the characteristics of different BJT Amplifier circuit configurations
   d) Use of Darlington Pair & Cascode configurations in improving Amplifier Characteristics

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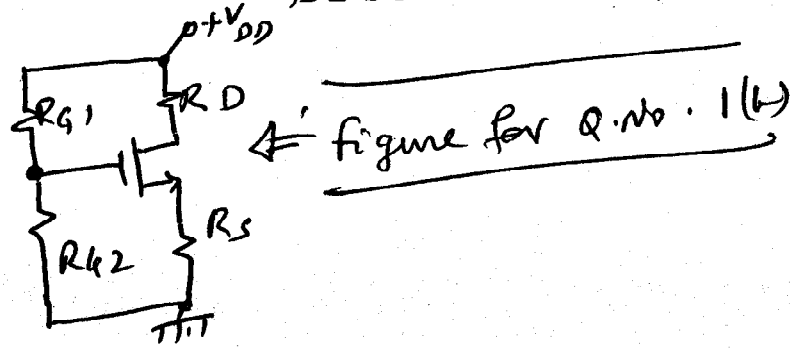

figure for Q.No. 1(b)

BITS, Pilani – Dubai Campus, Knowledge Village, Dubai

III B.E.(Hons.) I Semester – EEE & EIE

Course No. EEE UC 424 / INSTR UC 313 Microelectronic Circuits

Comprehensive Examination – Closed Book

Date : 28-12-2005 **Max. Marks : 80**

Duration : 3 Hours **Weightage : 40%**

Note :- 1.**Answering of Question No.1 is Compulsory**
2.**Answer ANY SIX from the remaining Questions**
3.Make your Assumptions, if any, explicit
4.Students can answer in their own unused Semi-Log./ Ordinary Graph sheets, only after obtaining invigilator's signature (with date) on it as an endorsement that it is empty before its use by the student concerned during the examination.

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1)

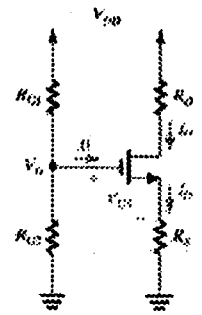
a) 

Figure: (c)

It is required to design the circuit shown in Figure:(c) to establish a dc drain current I_D = 0.5mA. The MOSFET is specified to have V_t=1V and k'_nW/L = 1 mA/V^2. Employ a power supply V_{DD}=15V. Also compute the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same k'_nW/L but V_t=1.5V (3 Marks)

b) Compare "the NMOS" and "the n-p-n" Transistors in respect of (i)Circuit symbol (ii)the conditions (in terms of equations to be satisfied) under which each act as Amplifier (iii)Low Frequency hybrid Model (iv)High Frequency Model and (v)the Design Parameters(5 Marks)

c) Obtain an expression for the output voltage v_o of a typical Differential amplifier in terms of its C.M.R.R., common mode gain and Differential Mode gain . (3 Marks)

d) Explain the steps and the way to arrive at "A" circuit and "β" circuit of a typical feedback amplifier in which a BJT differential stage is followed by an emitter follower. (3 Marks)

e) Sketch the Ideal Transmission Characteristics of the four major filter types and indicate how the real filter specifications of any one of them typically differ. (3 Marks)

f) A BJT is specified to have T_{Jmax} = 150°C and to be capable of dissipating maximum power as follows : 40 W at T_C = 150°C; 20 W at T_A= 25°C; Above 25 °C, the maximum power dissipation is to be de-rated linearly with θ_{JC}=3.12°C/W and θ_{JA}=64.5°C/W. Find the maximum power dissipated safely by this transistor when operated (i)in free air at T_A= 50°C . (ii)at T_A= 50°C , but with a heat sink for which θ_{CS}=0.5°C/W and θ_{SA}= 4°C/W (3 Marks)

2)

a) Sketch the transmission characteristics of a fifth-order low pass filter having all transmission zeros at infinity. Arrive at its Pole Zero pattern. Also prove that as the filter's order increases, the Magnitude response of such a Butter-worth filter approaches the ideal brick-wall type of transmission. (2+2+4=8 Marks)

b) Summarize the basic 4-steps that enable one to arrive at the Chebyshev transfer function in the realization of a given low-pass filter specifications. (2 Marks)

(Please Turn Over)

3) Using a neat Sketch of the circuit of a class B Output Stage, explain its operation and analyze to show that it cannot offer power conversion efficiency more than 78.5%. Also illustrate how cross over distortion results in a typical class B Stage. (2+2+4+2 = 10 Marks)

4)

a) A single stage CE Amplifier is measured to have a voltage gain bandwidth f_H of 5 MHz with R_L=500Ω. Assume h_{fe} = 100, g_m=100mA/V, rbb'=100Ω, $C_{b'c}$ =1pF and f_T=400 MHZ, Using approximate analysis, (a) Find the Value of the Source Resistance, R_s that will give the required Bandwidth. (b) With R_s found in part (a) find the mid band voltage gain V_o/V_s. (4+3=7 Marks)

b) Given the following BJT measurements made at I_C=5mA, V_{CE} = 10V and at room temperature (27°C) : h_{fe} = 100, h_{ie} = 600Ω, $|A_{ic}|$ =10 at 10 MHz, $C_{b'c}$=3pF. Find f_β, f_T, $C_{b'e}$, $r_{b'e}$, and $r_{bb'}$. (3 Marks)

5) A three pole feedback amplifier has a dc gain without feedback = -10^4. All three open loop poles are at f = 2 MHz. What is the maximum value of β for which the amplifier is stable? Assuming that one of the poles is shifted to f_1 =100 kHz, using the β found in (a), what is the gain margin of the modified circuit? (5+5=10 Marks)

6) Pole-zero compensation is used with an amplifier which has -10^3 dc gain and three poles at f_1 = 1MHz, f_2 =10 MHz and f_3 =200 MHz The zero of the pole-zero network is selected to cancel the 1 MHz pole of the uncompensated amplifier. Find the pole of the compensating network so that the amplifier is stable with a 45° phase margin when β = -0.1. (10 Marks)

7) Draw the Circuit of a BJT Differential amplifier employing silicon npn transistors biased by a non-ideal current source (as in a practical current mirror). Employing h-parameter model of a BJT, Analyze and obtain an expression for its common mode gain, A_c and differential mode gain, A_d. (2+4+4=10 Marks)

8) Draw a simplified internal circuit diagram of a typical four stage General Purpose Operational Amplifier IC. Identify the basic four functional stages it consists of and enumerate / describe the analysis methods to arrive at the important features of each functional stage (4+2+4=10 Marks)

9) Write a Short Notes on any TWO of the following: (5 x 2= 10 Marks)

a) Current Mirrors and Current Sources
b) Methods of Alignment in Tuned Amplifiers
c) A Comparison of the characteristics of different BJT Amplifier circuit configurations
d) Application of Composite Devices in improving Amplifier Characteristics

=====)B E S T OF L U C K(=====

VERSION A

Student Name: BITS ID No.:

BITS-Pilani Dubai Campus, Knowledge Village, Dubai

Evaluation Component : QUIZ(closed book)

EEE UC 424 / INSTR UC 313 MICROELECTRONIC CIRCUITS

Date : 15th Dec. 2005
Duration: 30 mts

Maximum Marks: 35
Weightage : 10%

Note:- 1.Respond ALL questions
2. Fill the blanks, show the working and / or indicate the **"most appropriate answer"** or **"most appropriate combination of Answers"** as required for each question.
2.Make your assumptions, if any, explicit
3.All questions carry 1 mark unless otherwise indicated

- - -

1. Identify the following signals (as either voltage or current) of the generalized signal flow diagram of a Shunt-Series feedback amplifier

X_i	X_o	X_f	X_s

2. Upon Application of Shunt-Shunt feedback to an open loop Amplifier, its input resistance will _____ (increase / decrease / remain unchanged) (0.5Mark)
3. To obtain the "A" circuit, while analyzing a feedback amplifier in which current sampling and current mixing is employed, R_{11} should be obtained by _____ (open / short) circuiting the amplifier's output. (0.5Mark)
4. Match the following configuration of feedback shown under I with the corresponding pair of the way "mixing-sampling" is accomplished as given under II …by indicating the serial no. of I in the braces: "[ ]" of II.

I	II
A. Series Series	current mixing and current sampling [ ]
B. Shunt Series	current mixing and voltage sampling [ ]
C. Shunt Shunt	voltage mixing and current sampling [ ]
D. Series Shunt	voltage mixing and voltage sampling [ ]

5. In determining the loop gain Aβ through an approach in which conceptual feed back loop is broken and a test signal (as appropriate) is applied, express Aβ in terms of Open & Short circuit transfer functions (T_{oc} & T_{sc} respectively) and also provide expressions to find T_{oc} and T_{sc}. (2 Marks)

Aβ = ; T_{sc} = ; T_{oc} = where in

____ is _____ ; ____ is _____ ;

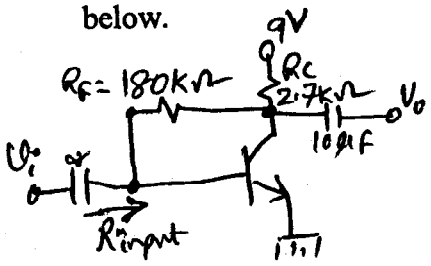
____ is _____ ; ____ is _____

6. If the two poles of a feedback amplifier are on the imaginary axis and are complex in nature then they occur as a _____ pair and the amplifier is said to have _____ response

7. The Phase margin is _____ degrees minus _____ at the frequency at which _____ is unity.
8. In Lead compensation, the amplifier or the β network's transfer function is modified so as to add a _____ (pole / zero). (0.5Mark)
9. From the general rule of thumb in ensuring Feedback amplifier's stability, at the intersection of 20log [1 / |β(jω)|] and 20log |A(jω)| the _____ should not exceed 20 dB / decade.
10. In order to obtain linear amplification, the MOSFET is biased to operate somewhere near the _____ of the _____ region of its characteristics.
11. An Alternate method of biasing instead of "fixing of V_{GS}" of a FET in amplifier applications is by the use of a Resistance in the Source. This resistance is called _____ (0.5Mark)
12. Other than the use of two bias methods namely "fixing of V_{GS}" OR "use of R_S" list / indicate two other techniques of BIASING an FET
    1. _____
    2. _____
13. A Depletion type MOSFET can be operated in both "Enhancement Mode" and "Depletion Mode". State whether this statement is TRUE of FALSE. _____. (0.5Mark)
14. Process transconductance parameter determined by the process technology used to fabricate an NMOS can be expressed as _____ and is designated as _____ (0.5Mark)
15. When biased in _____ Region of an NMOS device, can be used as a VVR and the Characteristic i_D - V_{DS} relationship is expressed as : [2Marks]

16. The characteristic equation representing the "load line" of a CS Amplifier can be mathematically expressed as a relationship between i_D, V_{DD}, R_D and v_{DS} and it is given by: (2marks)

17. Assuming that β = 200, Determine the input resistance for the feedback amplifier shown below. (2 Marks)



Input Resistance is equal to _____

18. An npn transistor has a beta cutt-off frequency of 1 MHz, emitter short circuit low frequency current gain of 200. Its unity gain cut off frequency and the alpha cut off frequency respectively are _____ and _____ (2 Marks)

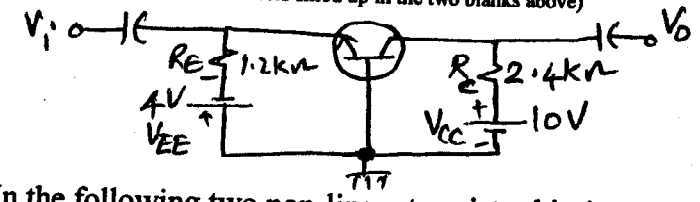
(Student is expected to show the way he/she is arriving at the answer in the space provided below, indicating major steps or formulae employed to arrive at the answers filled up in the two blanks above) (next page)

19. An amplifier has an open loop gain of 100, an input resistance of 1 KΩ, and an output resistance of 100Ω. A feedback network with a feedback factor of 0.99 is connected in a voltage series feedback mode. The new input and output resistances are _____ and _____, respectively (2 Marks)

(Student is expected to show the way he/she is arriving at the answer in the space provided below, indicating major steps or formulae employed to arrive at the answers filled up in the two blanks above)

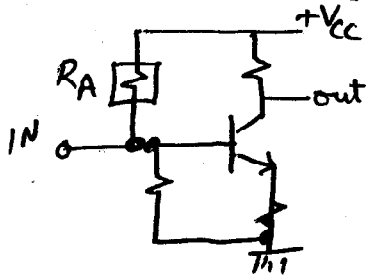
20. The V_{CB} and the current I_B for the CB-configuration of the figure shown below will be _____ and _____ respectively. Assume $\beta = 60$. (2 Marks)

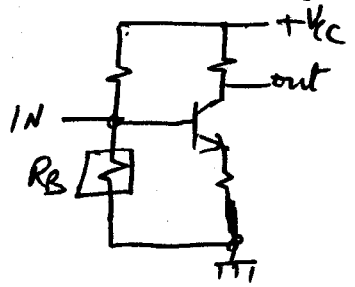
(Student is expected to show the way he/she is arriving at the answer in the space provided below, indicating major steps or formulae employed to arrive at the answers filled up in the two blanks above)



21. In the following two non-linear transistor biasing circuits, the resistors R_A and R_B are suitably employed to provide appropriate compensation against Bias Point drift, then, choose and indicate the most appropriate choice of the nature of resistors : [ ]

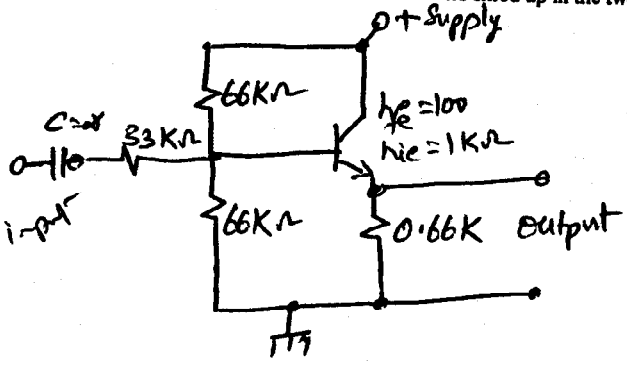
A. R_A and R_B, both have negative temperature coefficient
B. R_A and R_B, both have positive temperature coefficient
C. R_A has negative temperature coefficient and R_B has positive temperature coefficient
D. R_A has positive temperature coefficient and R_B has negative temperature coefficient





22. The voltage gain of the amplifier shown below is _____ (2 Marks)

(Student is expected to show the way he/she is arriving at the answer in the space provided below, indicating major steps or formulae employed to arrive at the answers filled up in the two blanks above)



23. A multistage amplifier has a low-pass response with three real poles at $s=-\omega_1$, $-\omega_2$, and $s=-\omega_3$. The approximate overall bandwidth B of the amplifier is given by [ ]
    A. $B = \omega_1+\omega_2+\omega_3$.
    B. $1/B = (1/\omega_1)+(1/\omega_2)+(1/\omega_3)$.
    C. $B = (\omega_1.\omega_2.\omega_3)^{1/3}$
    D. B = Square root of $(\omega_1^2+\omega_2^2+\omega_3^2)$
24. A differential amplifier is invatiably used in the input stage of all OPAMPs. This is done basically to provide the OPAMPs with a very high [ ]
    A. CMRR
    B. Bandwidth
    C. Slew Rate
    D. Open Loop Gain
25. A two stage amplifier is required to have an upper cut off frequency of 2 MHz and a lower cutoff frequency of 30 Hz. The upper and lower cutoff frequencies of the individual, but identical, stages are [ ]
    A. 4 MHz, 60 Hz
    B. 3 MHz, 20 Hz
    C. 3 MHz, 60 Hz
    D. 4 MHz, 20 Hz
26. A Class-A transformer coupled transistor power amplifier is required to deliver a power output of 10 watts. The maximum power rating of the transistor should not be less than
    A. 5 W
    B. 10 W [ ]
    C. 20 W
    D. 40 W
27. Most of the linear ICs are based on the two transistor differential amplifier because of its
    A. Input voltage dependent linear transfer characteristic [ ]
    B. High voltage gain (0.5Marks)
    C. High input resistance
    D. High CMRR
28. A source follower using an FET usually has a voltage gain which is [ ]
    A. greater than +100
    B. slightly less than unity but positive
    C. exactly unity but negative
    D. about -10
29. Class AB operation is often used in power (large signal) amplifiers in order to [ ] (0.5 Marks)
    A. Get maximum efficiency
    B. Remove even hormonics
    C. Overcome a cross-over distortion
    D. Reduce collector dissipation
30. Draw the Large-Signal Equivalent-Circuit Model of an NMOS device operating in saturation region that can be employed to analyze a practical circuit. Indicate all components of the equivalent circuit and the significant voltages and currents with most appropriate symbol notation. [2 Marks]

III B.E.(Hons.) I Semester – EEE & EIE

Course No. EEE UC 424 / INSTR UC 313 Microelectronic Circuits

Test-2 – OPEN BOOK

Date : 05-11-2005
Duration : 50 mts.

Max. Marks : 30
Weightage : 20%

Note :- 1.Answer ALL Questions
2.Make your Assumptions, if any, explicit
3.Permitted to refer Class Notes, Text Books or Reference Books
4.Students can answer in their own unused Semi-Log Graph sheets, if necessary
5.Students can answer in their own unused Graph Sheets.

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1)

a) An Amplifier employs BJT whose parameters: h_{fe} = 100, h_{ie} = 600Ω, $|A_{ie}|$ =10 at 10 MHz, $C_{b'c}$=3pF were measured at I_C=5mA, V_{CE} = 10V and at room temperature (27°C). Find f_β, f_T, $C_{b'e}$, $r_{b'e}$, and $r_{bb'}$. (5 Marks)

b) A MOSFET CS amplifier has R_{in}=2 MΩ, g_m=4 mA, r_o=100kΩ, R_D=10kΩ, C_{gs}=2pF, and C_{gd} = 0.5pF. The amplifier is fed from a voltage source with an internal resistance of 500 kΩ and is connected to a 10-kΩ load. Find (a)the overall mid band gain A_M and (b)the upper 3-dB frequency f_H. (2.5 + 2.5 = 5 Marks)

2)

a) A CE amplifier employs an n-p-n BJT having R_C = 10KΩ and is supplied input from an ac signal from a generator of 1KΩ internal resistance. A Resistance R_f = 100KΩ connects the collector to the base providing necessary negative feedback.(A)Identify the feedback topology to indicate in terms of one of the four topologies : current shunt / voltage shunt / voltage series / current series and justify your identification with pure conceptual but brief and crisp to-the-point explanation – no equations please. (B) Analyze the feedback amplifier to obtain its parameters:(i)Transfer gain (ii)Over all Voltage gain, and (iii) Input resistance (1+ 2 +2+2=7Marks)

b) An Amplifier has open loop dc gain of -10^3 with its poles located at f_1 = 1MHz, f_2 = 10 MHz and f_3 =30MHz. It is decided to employ Dominant pole compensation to this amplifier.
i) Find the location of the dominant pole so that the open-loop gain is first constant and then falls to 0dB at a rate of -20dB per decade for frequencies f ≤ 1MHz. (2 Marks)
ii) Find the maximum value of β for which this compensated amplifier is stable.
U can perform Graphical analysis on a Bode plot (2 + 1 = 3 Marks)

3) Draw the Circuit of a BJT Differential amplifier employing silicon n-p-n transistors biased by a non-ideal current source (as in a practical current mirror). Employing h-parameter model of a BJT, analyze and obtain an expression for its common mode gain, A_c and differential mode gain, A_d. (2+4+4 Marks)

=======)B E S T OF L U C K(=======

BITS, Pilani – Dubai Campus, Knowledge Village, Dubai

III B.E. (Hons.) (EEE / EIE) I-Semester

Course No.: EEE UC 424 / INSTR UC 313 Microelectronic Circuits

TEST-1 (Make-Up) – Closed Book

Date : 16-10-2005
Duration : 50 mts.

Max. Marks : 30
Weightage : 20%

NOTE :- 1.Answer ALL Questions
2.Make your Assumptions, if any, Explicit.

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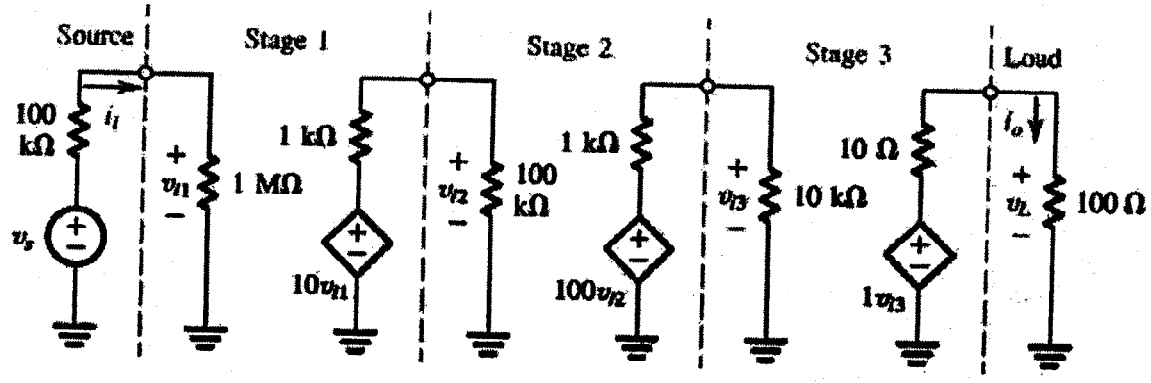
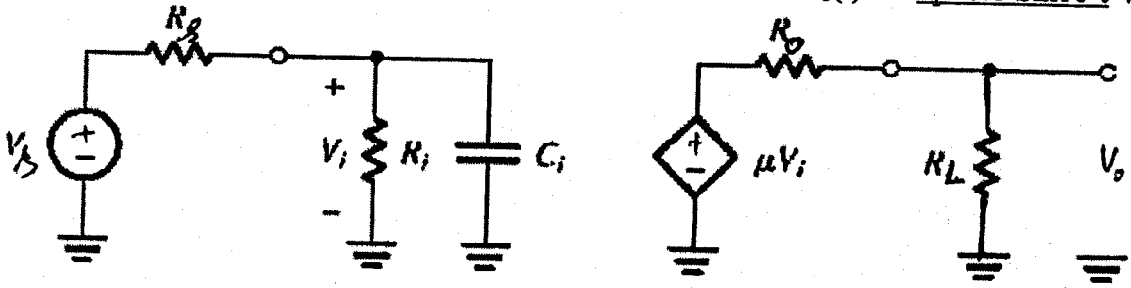
1) A transistor amplifier has the transfer characteristic $v_o = 10 - 10^{-11} e^{40v_I}$ that applies for $v_I \geq 0V$ and $v_O \geq 0.3V$. A positive input voltage signal of 1 mV superimposed on the dc bias voltage V_I. Find the corresponding signal at the output assuming that the amplifier behaves linearly around quiescent point.. **(4 Marks)**

2) For the Cascade Amplifier shown below, if v_s is 1mV, Find v_i1, v_{i2}, v_{i3} and v_L.



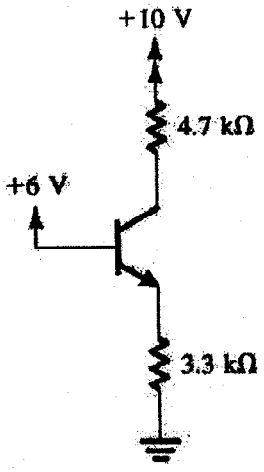
(6Marks)

3) An Voltage Amplifier has an input resistance R_i, an input capacitance C_i, Gain Factor μ and an output resistance R_o. It is fed from a voltage source, v_s, having a source resistance R_s, and a load resistance R_L is connected to the output. Find the values of the dc gain, the 3-dB frequency and the frequency at which the gain becomes 0-dB for the case R_s=20KΩ; R_i = 100KΩ, C_i=60pF, μ=144, R_o=200Ω and R_L = 1kΩ. Also find $v_o(t)$ for $v_i = 0.1\ \mathrm{Sin}10^2 t$ V



(6 Marks)

4) Perform dc Analysis on the following circuit assuming β is 100 (6 Marks)



(a)

5) Draw the Circuit of a Common Base Amplifier employing Current mirror Bias. Using a suitable model analyze for the terminal characteristics R_{in}, A_v, R_{out}, G_v, A_{is}. (8 Marks)

BITS, Pilani – Dubai Campus, Knowledge Village, Dubai

III B.E. (Hons.) (EEE / EIE) I-Semester

Course No.: EEE UC 424 / INSTR UC 313 Microelectronic Circuits

TEST-1 – Closed Book

Date : 16-10-2005
Duration : 50 mts.

Max. Marks : 30
Weightage : 20%

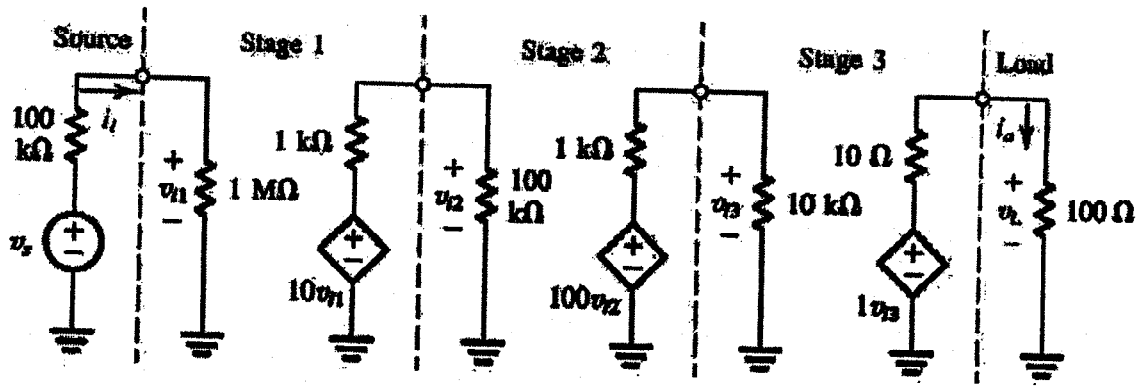
NOTE :- 1.Answer ALL Questions
2.Make your Assumptions, if any, Explicit.

1. A transistor amplifier has the transfer characteristic :

$$v_o = 10 - 10^{-11} e^{40 v_I}$$

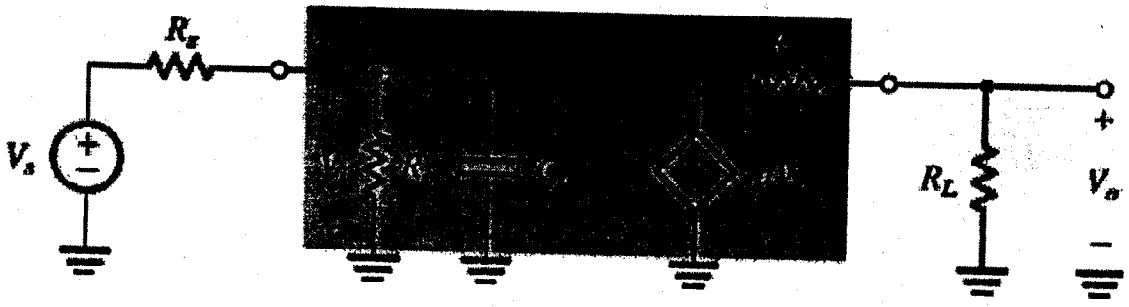
Which applies for $v_I \geq 0V$ and $v_O \geq 0.3V$. Find the negative and positive saturation limits L_- and L_+ and the corresponding values of v_I. Also find the value of the DC bias voltage V_I that result in V_o=5V and the voltage gain at the corresponding operating point **(6 Marks)**

2. What would be the overall gain of the cascade amplifier shown below without stage 3?



(4 Marks)

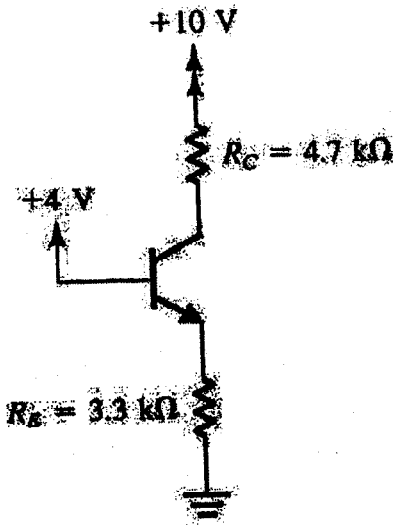
3. An Voltage Amplifier has an input resistance R_i, an input capacitance C_i, Gain Factor μ and an output resistance R_o. It is fed from a voltage source, v_s, having a source resistance R_s, and a load resistance R_L is connected to the output Derive an expression for the amplifier voltage gain Vo / Vs as a function of frequency. From this, find expressions for dc gain and the 3-dB frequency.



(6 Marks)

P.T.O

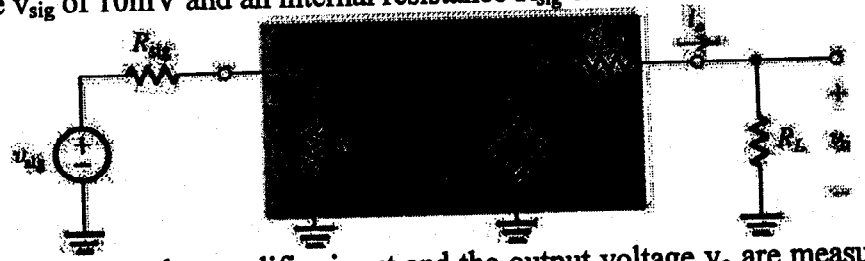
4. Perform a detailed dc Analysis on the following circuit assuming β is 100



(a)

(6 Marks)

5. A transistor amplifier, modeled as below, is fed with a signal source having an open-circuit voltage v_{sig} of 10mV and an internal resistance R_{sig} of 100kΩ.



The Voltage v_i at the amplifier input and the output voltage v_o are measured both without and with a load resistance R_L=10KΩ connected to the amplifier output. The measured results are as follows:

	v_i (mV)	v_o(mV)
Without R_L	9	90
With R_L Connected	8	70

Find ALL the characteristic parameters of this amplifier

(8 Marks)