BITS PILANI DUBAI CAMPUS
KNOWLEDGE VILLAGE, DUBAI

III Year EEE – I Semester 2005-06
COMPREHENSIVE EXAM
ELECTRONIC DEVICES AND INTEGRATED CIRCUITS

Date: 5/1/06
Max. Marks: 50

Time: 3 Hrs
Weightage: 40%

Answer All Questions

1(a) Draw the variations of the depletion region pinch off and beyond pinch off for JFET. Hoe does pinch off and saturation occur in a JFET. (3M)

(b) Draw the family of current voltage curves as V_G is varied. Mark the pinch off region. (2M)

(c) Briefly explain how an n channel MOSFET can be fabricated. (5M)

2. (a) Define the terms:
Base transport factor, Emitter injection efficiency and Current transfer ratio. (3M)
(b) Graded doping can lead to a drift component of charge transport across the base. Explain. (3M)
(c) Briefly discuss the frequency limitations of transistors. (4M)

3. (a) Why must a solar cell be operated in the fourth quadrant of the junction I-V characteristics. (3M)
(b) Why the quaternary alloy is used in fabricating LED's for fiber optics. (3M)
(c) Explain how the population inversion takes place at a junction. (4M)

4. (a) What are the advantages of integration. (3M)
(b) Explain the process of integration of the following circuit elements. Resistors, Capacitors and Contacts (4M)
(c) Explain the principle of basic charge coupled device. (3M)

5. (a) Explain the operation of a tunnel diode with the help of band diagrams (5M)
(b) Discuss the basic structure of a Shockley diode. (5M)

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III Year EEE – I Semester 2005-06
Test2 (Open Book)
ELECTRONIC DEVICES AND INTEGRATED CIRCUITS

Date:
Max. Marks: 40

Time: 50mts
Weightage: 20%

Answer ALL Questions

1. In a symmetric p-n Si junction, $N_a = N_d = 10^{17}$ cm^{-3}. If the peak electric field in the junction at breakdown is 5×10^5 V/cm, what is the reverse breakdown voltage in this junction. (10M)

2. In a p-n junction the n doping N_d is doubled. How do the following change if every thing else remain unchanged. Indicate only Increase or Decrease.

   (a) Junction capacitance
   (b) Built in potential
   (c) Breakdown voltage
   (d) Ohmic losses

   (5M)

3. Calculate V_T of a Si n channel MOSFET for an n+ poly silicon gate with gate oxide thickness of 100 $\overset{0}{A}$, $N_a = 10^{18}$ cm^{-3} and a fixed oxide charge of 5×10^{10}q C/cm^2. (10M)

4. Explain the following.
   (i) Modulation doped field effect transistor (5M)
   (ii) Base width modulation (5M)
   (iii) Emitter crowding (5M)

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III Year EEE – I Semester 2005-06
Test1
ELECTRONIC DEVICES AND INTEGRATED CIRCUITS

Date: 9/10/05
Max. Marks: 40 Time: 50mts
Weightage: 20%

Answer ALL Questions

1 (i) Show the energy band diagram of an insulator, semiconductor and metal at 0^0K (2M)

(ii) Differentiate between Direct and Indirect semiconductors. (2M)

(iii) Name 3 impurities for each of the following
(a) To create p type material
(b) To create n type material (3M)

(iv) Derive the expression to calculate the concentration of electrons in the conduction band using Fermi distribution function. (3M)

2 (a) (i) Give the experimental setup to measure the band gap energy of a semiconductor. (1M)

(ii) Explain the principle involved for the above. (2M)

(iii) Derive the expression of the intensity of light transmitted through the sample. (3M)

(b) Explain following
Cathodoluminescence, Electroluminescence. (4M)

3. Describe the following process.
(i) Thermal oxidation
(ii) Chemical vapour deposition (6M)

4(a) Explain the Zener breakdown mechanism. (4M)

(b) What are the requirements in the design of a rectifier diode. (3M)

(7M)