BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai

Year III – Semester I 2005 – 2006

Comprehensive Examination (Closed Book)

Course No.: **CS / EIE UC 391** Course Title: **DECO**

Date: January 03, 2006 Time: 3 Hours. Max. Marks = 75

Any assumptions made should be indicated clearly.

Unless otherwise mentioned assume positive logic is used throughout.

1.a) Find the value of the binary product (10110_2 x 1011_2)

b) Find the quotient of (110010_2 / 011_2) (3 x2)

2.a) Reduce: **[(AB' + ABC)' + A(B + AB')]'**

b) Simplify using Boolean Algebra

Y'Z' + W'X'Z' + W'XYZ' + WYZ'

c) Expand **A + BC' + ABD' + ABCD** to minterms and maxterms. (3 + 4 + 4)

3. There are three doors in a hall. An indicator Y has to be **Switched off (low)** when two or more doors are opened and also when none of them are open. Draw the K-map for the above case assuming inputs A, B and C for the state of each of the doors. **(open =1, closed = 0)**. Realise the simplified circuit to achieve the output Y. Identify the Prime Implicants and Essential prime Implicants. (3+3+1.5+1.5)

4. An application of PROM is to realize look-up tables for arithmetic functions. Using a PROM of appropriate size, it is required to realize the expression

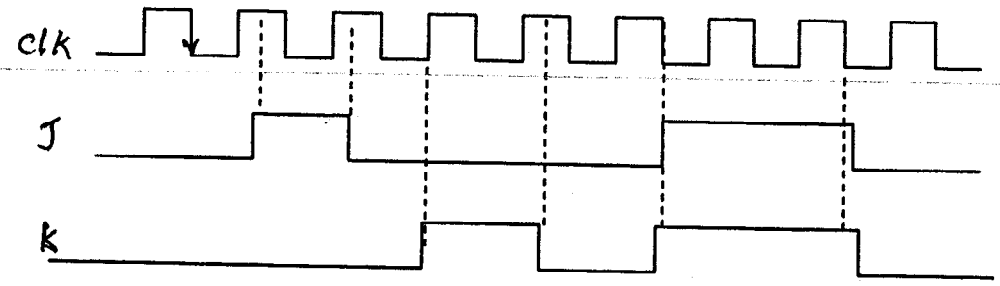
$F(x) = x + 2 \quad 0 <= x <= 3$

$= x - 1 \quad 3 < x <= 7$

Draw the **logic diagram** using PROM showing PLD notations (6)

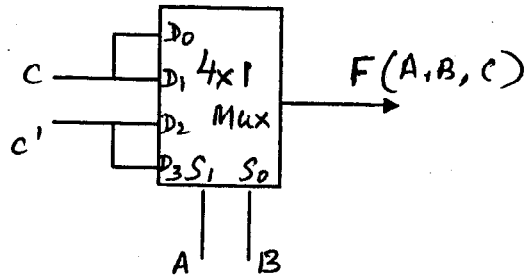
5. Design a synchronous counter with T flip-flops and logic gates to count a repeated sequence of 0, 1, 3, 7, 6, 4. The design should be self correcting. (7)

6. The waveforms shown in the figure below is applied to the J-K flip-flop. Draw the output waveform.



(6)

7. For the multiplexer circuit shown in figure shown below, Find the expression for F and implement the same using a single logic gate



(4+3)

8.a) Draw and explain the flow chart for the Non-restoration method of dividing integer numbers used in computers.

b) Illustrate the division algorithm using the numbers 1011_2 and 0011_2 (4+4)

9. Write short notes on any two of the following.
   a) Synchronous data transfer in computers
   b) IEEE 488 Bus (GPIB)
   c) The UARTs
   d) DMA

(4+4)

10. Draw the circuit and explain the operation of a Schottky TTL NAND gate. What are the merits and demerits of Schottky TTL gates? (7)

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BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester I 2005 – 2006
Test II (Closed Book) Make-up

Course No.: **CS / EIE UC 391** Course Title: **DECO**

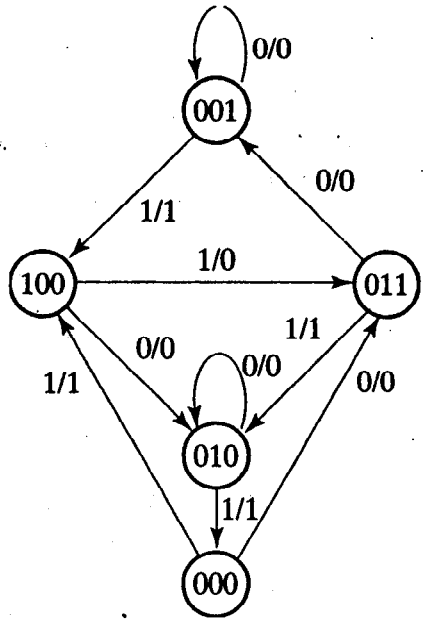
Date: December 11, 2005 Time: 50 Minutes Max. Marks = 30

(Any assumptions made should be indicated clearly. All questions carry 10 marks each.)

1. Explain the characteristic tables of D, JK and T flip flops. Design a JK flip flop using D flip flop and logic gates.

2. With a neat logic circuit diagram, explain the working of a Synchronous 4-bit binary UP-Down counter.
   Also show how a synchronous 4-bit binary counter with clear input can be modified as a BCD counter. Explain.

3. The state diagram of a sequential circuit with three flip flops, one input and one output is shown in the figure below. Design the circuit using T flip flops and logic gates assuming the unused states are don't care conditions.



BITS, PILANI – DUBAI CAMPUS

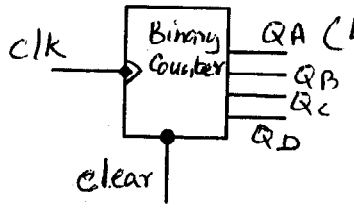
Knowledge Village, Dubai
Year III – Semester I 2005 – 2006
Test II (Closed Book)

Course No.: **CS / EIE UC 391** Course Title: **DECO**

Date: December 11, 2005 Time: 50 Minutes Max. Marks = 30

(Any assumptions made should be indicated clearly)

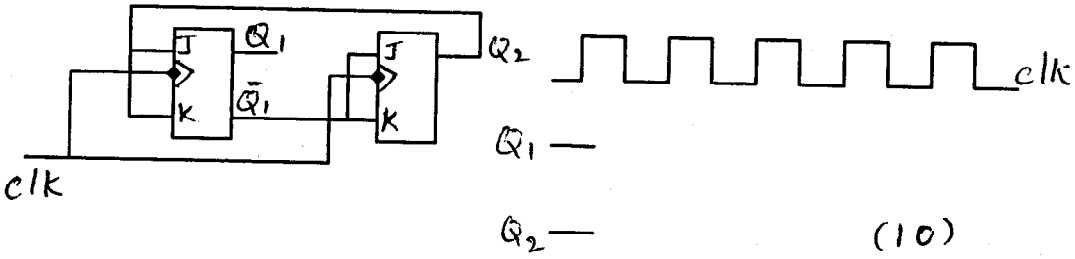
1. Design a sequential circuit that produces a logic '1' output when the input has been '1' for ten or more consecutive clock pulses. Use the counter shown below and minimum number of basic gates. Assume the input is 'x' and the output is 'y' .



Explain your circuit.

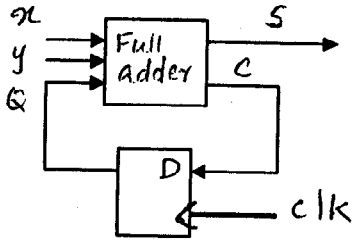
(10)

2. Given the logic diagram as below. Complete the timing diagram. Assume both Q1 and Q2 are zero initially.



(10)

3. A sequential circuit has one flip flop Q, two inputs x and y, and one output S. It consists of a full adder circuit connected to a D flip-flop as shown in the figure. Derive the state table and state diagram of the sequential circuit.



(10)

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BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
Year III – Semester I 2005 – 2006
Quiz (closed Book)

Course No.: **CS / EIE UC 391** Course Title: **DECO**

Date: October 27, 2005 Time: 30 Minutes Max. Marks = 20

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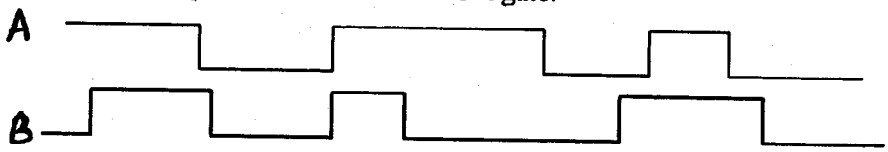
1. Represent the decimal value (-27) as 10 bit binary number in
   i) Signed Magnitude form ii) Signed One's Complement form

2. Use 2's complement arithmetic to compute $(83 - 97)_2$. Comment on your result.

3. The decimal equivalent of the binary number 1101100.01101 is _____

4. (a) In a circuit input A & B are applied to a NOR gate and to a NAND gate. The output of the two gates are then applied to an OR gate. If the inputs A & B are as shown in the figure, Draw the out put wave form of the OR gate.



5. Simplify the following function $F = B [(A + B') (B + C)]$ using Boolean algebra

6. Differentiate between a decoder and demultiplexer

7. Write a Boolean expression which will produce a high output when A > B where A & B are 4-bit binary words.

8. Which standard logic circuit (device) will you use to get the binary output corresponding to the seven segment binary inputs(a-g) ?

9. Define 'half adder' and 'full adder'

10. _____ gates outputs when tied together perform the wired-AND logic and the output of _____ gates when tied together will perform the wired-OR function.

BITS – PILANI DUBAI CAMPUS

Knowledge Village, Dubai
I semester III Year 2005-2006

Digital Electronics & Computer Organisation
C S [illegible] / INSTR UC 391
Test -1 **(Closed Book)**

23 – 10 – 05 **Time : 50min.** Max. Marks : 30 **Weightage : 15 %**

(Answer all questions. Calculators are not allowed. **Assume positive logic)**

1. Convert the hex number 3A7 to Gray code (3)

2. Create a truth table for a circuit which multiplies two 2-bit numbers (A_1A_0 and B_1B_0) (3)

3. Draw a logic diagram which represents the function F= (A'B + AD')'.C
   The available inputs are A,B,C and D. Redraw the circuit using NAND gates alone.
   How many NAND gates are required to implement the circuit (2+2+1)

4. Its desired to design a combinational logic circuit that will cause a light to go *ON* each time the decimal equivalent of 4-bit binary input is divisible by 3. It is known that the numbers 0,1,7,11 and 14 will never occur as inputs. Maps the function and simplify with K-Map and draw the logic diagram. (3+2+2+1)

5. Draw & Explain the logic diagram of a 4 x 1 Multiplexer (4)

6. How many 32 x 8 RAM chips are needed to provide a memory capacity of 256K bytes? How many address lines will be needed to address this memory bank? Show the decoding of address lines to generate the chip select signals of the memory units using a decoder. Also specify the size of the decoder.
   (1+2+3+1)

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BPDC, Knowledge Village, DUBAI

III rd yr I st Semester 2005-2006.

DECO T1 -(Make-up)

Max. Marks. 30

Time: 50 min.

I. Do the BCD addition of the decimal numbers

938 + 252 (3)

II. Show that the dual of Ex-OR is equal to its compliment (3)

III. Implement the following Boolean function F, together with the don't care conditions d, using no more than two NOR gates:

$F(A,B,C,D) = \Sigma(0,1,2,9,11)$

$d(A,B,C,D) = \Sigma(8,10,14,15)$

Assume both normal and Compliment inputs are available (5)

IV. Design a logic to examine two - 2 bit binary numbers (A_2A_1 and B_2B_1) and produce a TRUE output if the number B_2B_1 is greater than the number A_2A_1. Implement in NAND hardware, and define the variables as LT or HT so that no inverters are required. (Assume positive logic) (8)

V. Draw the logic diagram of a 2 to 4 line decoder and explain its operation. (4)

VI a) Draw the two dimensional addressing logic of a 512 x 8 memory unit.

b) Show how the memory capacity can be expanded to 2K x 8 using 512 x 8 units.

c) How many 512 x 8 memory ICs will be needed to have 2K x 8 memory bank? (3+3+1)
