

BITS PILANI DUBAI CAMPUS  
KNOWLEDGE VILLAGE

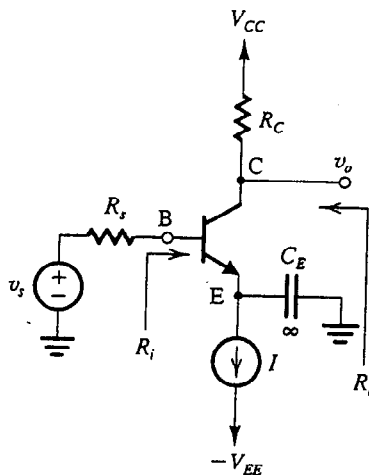
MICROELECTRONIC CIRCUITS  
TEST 1

Date: 24-10-04  
Time: 50mts

Max Marks: 20  
Weightage: 20%

Answer ALL Questions

- 1) (i) Draw the circuit models of the FOUR amplifier types. (3)  
(ii) Give the expression for the gain parameter for the above circuits. (1)  
(iii) Give the ideal value of  $R_i$  and  $R_o$ . (1)
- 2) For the amplifier shown in the figure find  $R_i$ ,  $A_v$ ,  $A_i$  and  $R_o$  given  $I=1\text{mA}$ ,  $R_C=5\text{ k}\Omega$ ,  $\beta=100$ ,  $V_A=100\text{V}$  and  $R_s=5\text{ k}\Omega$ . If the output is connected to a load resistance of  $5\text{ k}\Omega$ , find the new value of  $A_v$ . (5)



- 3) (i) Draw the high frequency hybrid  $\pi$  model of a BJT. (1)  
(ii) Derive the expression for unity gain bandwidth. (4)
- 4) (i) Show any TWO circuits for the biasing the MOSFET in discrete circuit design. (2)  
(ii) Derive the expression for the voltage gain of a common drain amplifier. (3)

BITS PILANI DUBAI CAMPUS  
KNOWLEDGE VILLAGE

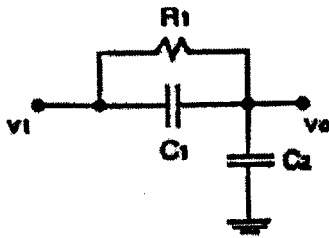
MICROELECTRONIC CIRCUITS  
TEST 2(Open Book)

Date: 12-12-04  
Time: 50mts

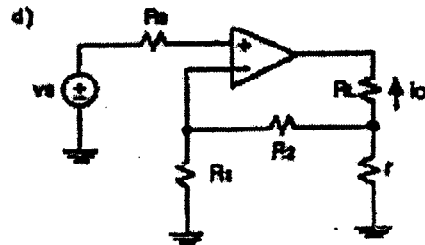
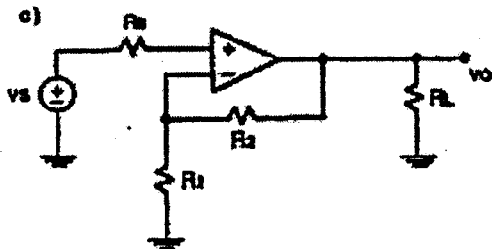
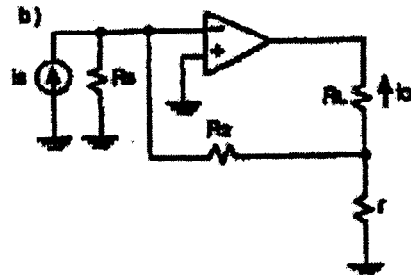
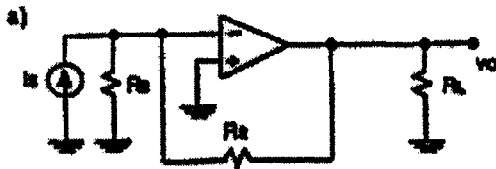
Max Marks: 20  
Weightage: 20%

Answer ALL Questions

- 1) A differential amplifier uses collector resistors of  $100\text{ k}\Omega$  and a bias source of  $200\text{ }\mu\text{A}$ . What is its differential voltage gain for outputs taken differentially. What is the differential input resistance. Emitter resistors are added to double the input resistance. What are their values. What does the differential voltage become. (5 marks)
- 2) Find the transfer function of the circuit shown. For  $C_1=0.05\text{ }\mu\text{F}$ ,  $C_2=0.5\text{ }\mu\text{F}$  and  $R_1=10\text{ k}\Omega$ , find the location of the pole(s) and zero(s). Sketch Bode plot. (5 marks)



- 3) Characterize each of the following amplifiers by feedback type. Find  $\beta$  in each case. Assume the op amp to be ideal. (5 marks)



4) The class A power amplifier using emitter follower operates from  $\pm 3\text{V}$  supplies with  $R=1.5\text{ k}\Omega$  using identical transistors. For  $V_{CE\text{ sat}}=0.3\text{ V}$  what is the largest undistorted sine wave that can be produced across a  $1\text{ k}\Omega$  load and a  $10\text{ k}\Omega$  load. For what range of load resistances is the output symmetrical. (5 marks)

BITS PILANI DUBAI CAMPUS  
KNOWLEDGE VILLAGE

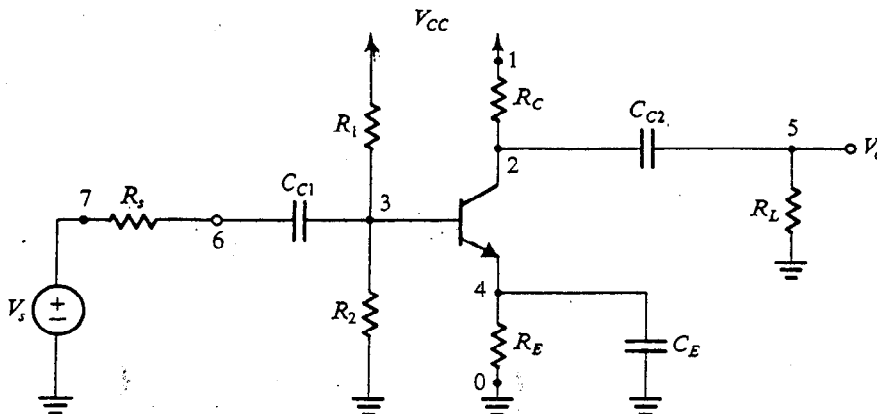
MICROELECTRONIC CIRCUITS  
Comprehensive exam

Date: 09/01/05  
Time: 3 Hours

Max Marks: 50  
Weightage : 40%

Answer ALL Questions

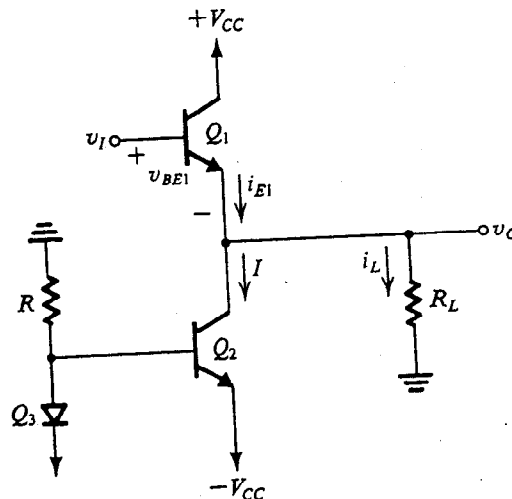
1. a) Show the circuit of a common emitter amplifier with a resistance in the emitter. Also show the equivalent circuit with BJT replaced by its T model. (1M)  
 Derive the expressions for  $R_i$ ,  $A_v$ ,  $R_o$ , and  $A_i$ . (3M)  
 Summarize the effect of  $R_e$ . (1M)
- b) A common emitter amplifier operating between a  $10\text{ k}\Omega$  source and a  $10\text{ k}\Omega$  capacitor coupled load, with a  $\pm 10\text{ V}$  supplies employs  $R_E = R_C = 10\text{ k}\Omega$ . For  $V_A = 200$  and  $\beta$  ranging from 50 to 150, what range of voltage gains  $v_o/v_s$  results. (5M)
  
2. a) Show the circuit of a differential amplifier along with currents and voltages when a small difference signal  $v_d$  is applied. (2M)  
 Derive the expressions for Collector currents, Input differential resistance, Differential voltage gain and Common mode gain. (4M)
- b) For a BJT differential pair biased at current  $I$ , both having a  $\beta$  mismatch of 10% and a source resistance mismatch of 10%. For nominal values of  $I$ ,  $\beta$  and  $R_S$  of  $100\text{ }\mu\text{A}$ , 100 and  $100\text{ k}\Omega$  respectively, what worst case input offset voltage is possible. (4M)
  
3. a) Explain the following properties of negative feedback deriving appropriate equations.  
 Gain desensitivity, Bandwidth extension, Noise reduction and Reduction in non linear distortion. (5M)
- b) The BJT common emitter amplifier shown in the figure uses  $R_S = 8.2\text{ k}\Omega$ ,  $R_1 \parallel R_2 = 40\text{ k}\Omega$ ,  $R_E = 8.2\text{ k}\Omega$ ,  $R_C = 9.1\text{ k}\Omega$  and  $V_{CC} = 5\text{ V}$ . For these conditions  $I_E = 0.15\text{ mA}$  at which  $\beta = 150$  and  $r_o = 500\text{ k}\Omega$ , coupling capacitors of value  $C_{C1} = C_{C2} = 1\text{ }\mu\text{F}$  and a bypass capacitor  $C_E = 10\text{ }\mu\text{F}$  are used. Calculate the pole and zero frequencies and the gain. (5M)



4. a) Derive the expression for power conversion efficiency of Class A and Class B power amplifiers. (5M)

b) Class A follower shown in the figure operates from  $\pm 9V$  supplies with  $I = 10 \text{ mA}$ . Ignoring the power loss in  $R$  and  $Q_3$ , find the load power, the supply power and the conversion efficiency for

- (i) The largest possible sine wave output and the smallest possible load resistance assuming  $V_{CE \text{ sat}} = 0.3V$ . (2 ½ M)
- (ii) A sine wave of half the amplitude in (i) across a load which is half the resistance of that in (i). (2 ½ M)



5. (a) Show the small signal equivalent circuit for the input stage and output stage of 741 Op amp. (2M)

(b) Show the circuit of an N bit D/A converter using a binary weighed resistive ladder network and explain its working. (4M)

(c) For the circuit in (b) which uses resistors no smaller than  $1 \text{ k}\Omega$ , what is the largest resistor required to implement an 8 bit converter. What is the largest value of switch resistance for which the associated error is at most  $\pm \frac{1}{2} \text{ LSB}$ . (4M)