BITS, PILANI - DUBAI CAMPUS

Knowledge Village

III-Year - 1st SEMESTER 2003-2004
Microelectronic Circuits (EEE UC424/INSTR UC313)
Comprehensive Exam (Closed Book)

Date: 11/1/2004
Time: 3 Hours
Max Mark: 80

Q1}

The BJT in the circuit of Fig. 1 has $\beta=100$.

a) Find the dc collector current and the dc voltage at the collector.

b) Draw the small-signal equivalent circuit of the amplifier using the T-model. Analyze the resulting circuit to determine the voltage gain v_o/v_i.

[10 M]

Q2}

For the circuit in Fig.2 let $|V_{BE}|=0.7$ V and $\beta=\infty$. Find I, V_1, V_2, V_3, V_4, and V_5, for a) R= 10 kΩ

b) R= 100 kΩ

[10 M]

Q3}

In the cascaded mirror circuit shown in Fig.3 all transistors has $V_t=1V$, $\mu_n C_{ox}=40\ \mu A/V^2$, L=5 μm, and $V_A=30V$. Widths $W_1=W_4=10\mu m$, and $W_2=W_3=200\mu m$. The reference current is 10μA and $V_{ss}=0$ V.

a) What output current results?

b) What are the voltages at the gates of Q_2 and Q_3?

c) What is the lowest voltage at the output for which the current-source operation is possible?

d) What are the values of g_m and r_o of Q_2 and Q_3?

e) What is the input and output resistance of the mirror? [12 M]

Q4}

The three stage amplifier circuit in Fig.4 has the following data:

	Q-point	g_m(mS)	r_π (kΩ)	r_o (kΩ)	β	C_{gs} , C_π	C_{gd} , C_μ	r_x (Ω)
M_1	5mA, 10.9 V	10	∞	12.2	∞	5 pF	1 pF	0
Q_2	1.67mA, 5.09V	62.8	2.39	54.2	150	39 pF	1 pF	250
Q_3	1.99mA, 8.36V	79.6	1.0	34.4	80	50 pF	1 pF	250

Use the open circuit time-constant (OCTC) and the short-circuit time constant (SCTC) techniques to estimate the upper- and lower- cutoff frequencies and the bandwidth for the given amplifier. [14 M]

Q5}

For the shunt-shunt feedback circuit in Fig.5, find the voltage gain V_o/V_s, the input resistance R_{in}, and output resistance using the feedback method. The op amp has open-loop gain $\mu=10^4$ V/V, $R_{id}=100$ kΩ and $r_o = 1$ kΩ.

[12 M]

Q6}

The circuit in Fig. 6 has the following element values: $V_{CC}=5V$, $R_L=3.3$ kΩ, $R_2=2.2$ kΩ. For all transistors, $\beta= \infty$, $V_A=20V$.

a) Compute the collector currents of Q_1, Q_2 and Q_3 and the collector voltage of Q_3.

b) Compare the maximum and minimum common-mode voltage such that Q_1, Q_2, and Q_3 are biased in the forward-active region.

c) Compute the differential-to-single-ended gain.

d) Compute the common-mode voltage gain and the CMMR. [10 M]

Q7}

A) Design a class B power amplifier that will deliver an average power of 20W to an 8Ω load. Assume that the supply voltage is larger than the peak voltage by 5V. Determine the power conversion efficiency. Also find the maximum power that each transistor can dissipate safely.

B) A power transistor is specified to have a maximum junction temperature of 130°C. When operating at this junction temperature with a heat sink, the case temperature is found to be 90°C. The case is attached to the heat sink with a bond having a thermal resistance θ_{CS} =0.5 °C/W and the thermal resistance of the heat sink θ_{SA} = 0.1 °C/W. If the ambient temperature is 30°C what is the power being dissipated in the device? What is the thermal resistance of the device θ_{JC}, from junction to case.

[12 M]

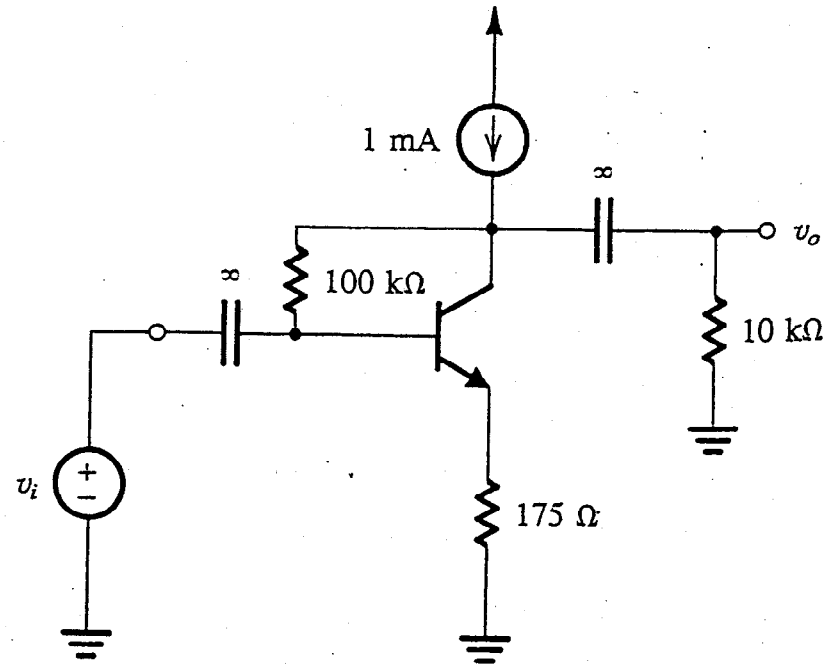

Fig. 1

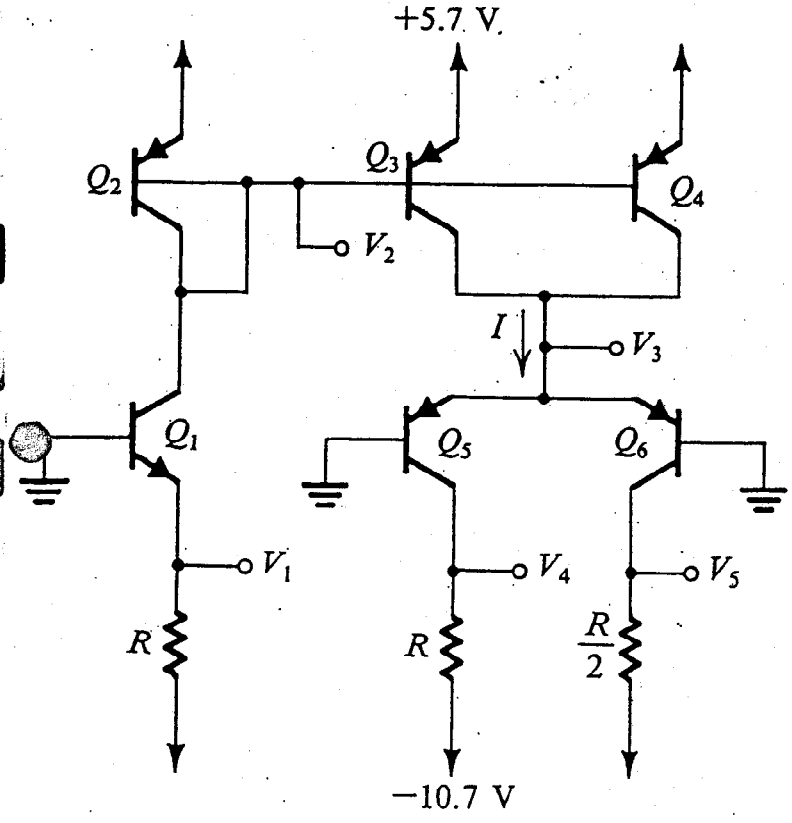

Fig. 2

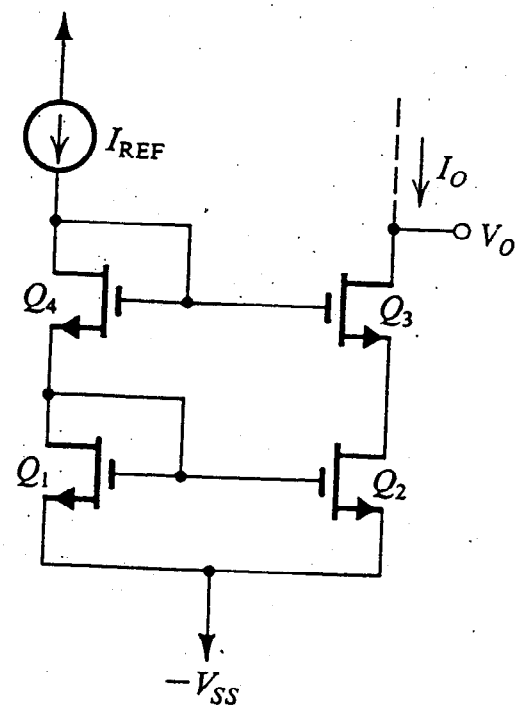

Fig. 3

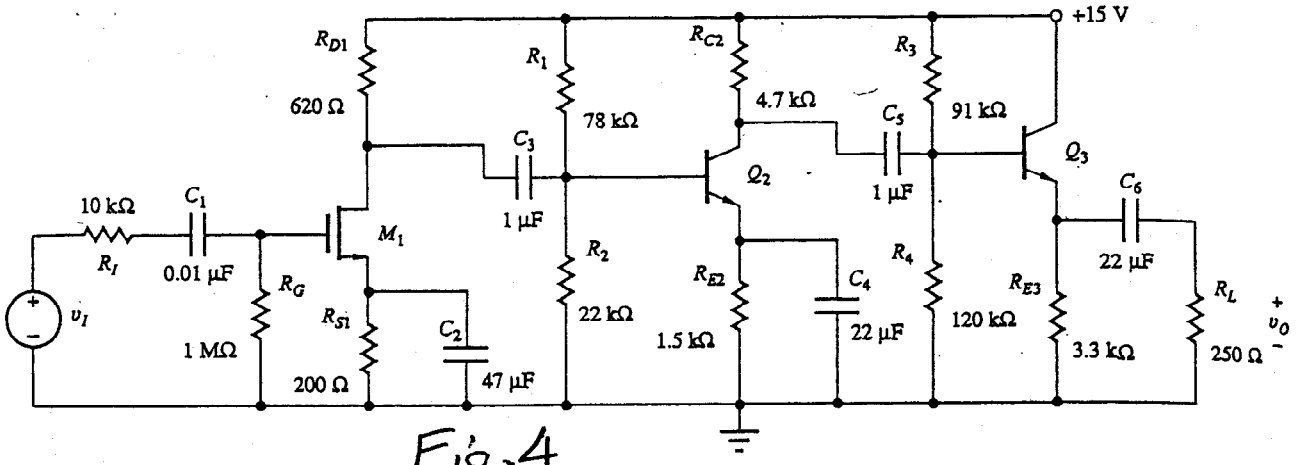

Fig. 4

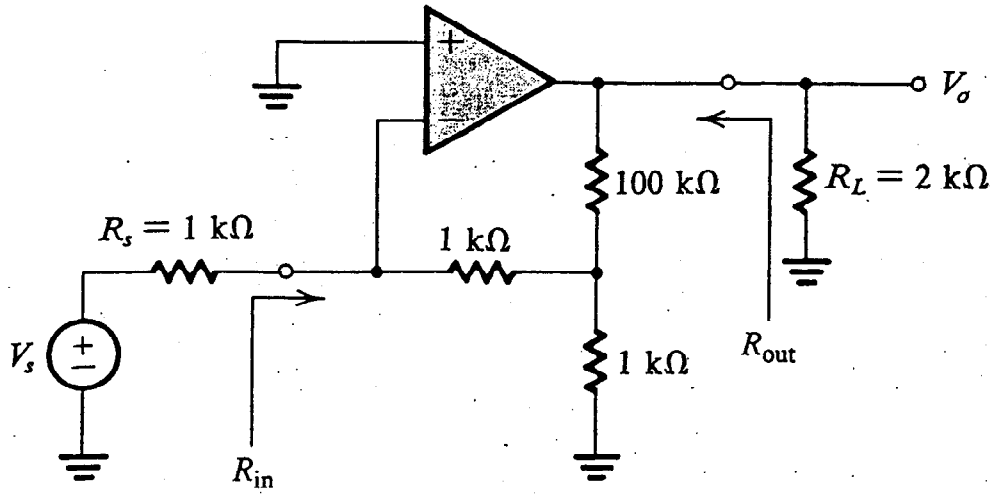

Fig. 5

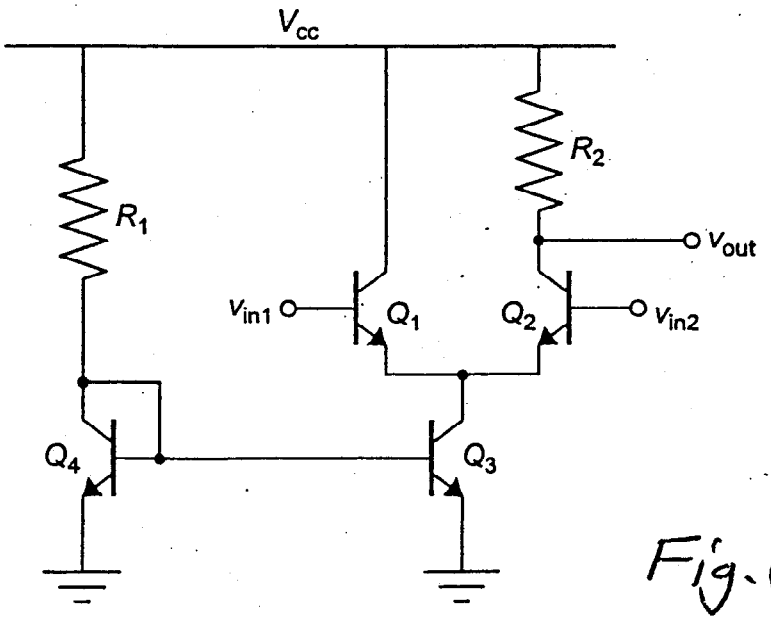

Fig. 6

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III-Year - 1st SEMESTER 2003-2004
Microelectronic Circuits (EEE UC424/INSTR UC313)
Test-I (Closed Book)

Date:2/11/2003
Time: 50 Min
Max Mark: 50

Q1}

For the circuit shown in Fig.1 find the dc emitter current. Assume that β=120. Neglecting r_o, find the input resistance R_i, the voltage gain v_o/v_s, the current gain i_o/i_i, and the output resistance R_o.

[12]

Q2}

In the circuit shown in Fig. 2 and for β=150, find v_o/v_{b2}, R_{b2}, v_{b2}/v_{b1}, R_{b1}, v_{b1}/v_s, v_o/v_s. [12]

Q3}

For the CMOS amplifier circuit shown in Fig.3, $k_n=2.5k_p = 50\ \mu A/V^2$, $|V_t|$=1v, and $|V_A|$=50V. Find I_{IREF} and (W/L) to obtain a voltage gain of -100V/V and an output resistance of 1MΩ. [9]

Q4}

Consider the circuit shown in Fig.4, find the ratio I_o/I_{REF} for each of the following cases:

a. $L_1=L_2$, $W_2=3W_1$
b. $L_1=L_2$, $W_2=10W_1$
c. $L_1=L_2$, $W_2=W_{1/2}$
d. $W_2=W_1$, $L_1=2L_2$
e. $W_2=W_1$, $L_1=10L_2$
f. $W_2=W_1$, $L_1=L_2/2$
g. $W_2=3W_1$, $L_1=3L_2$

[7]

Fig-1

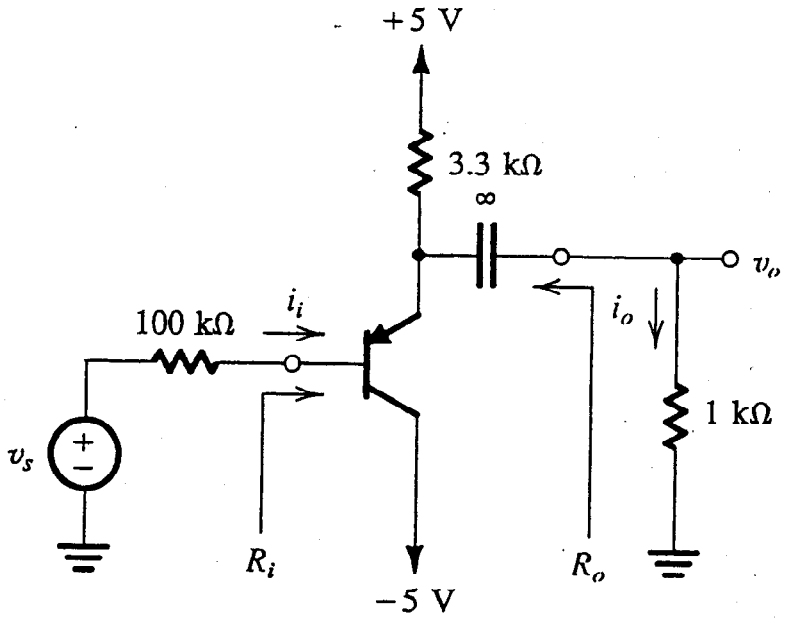
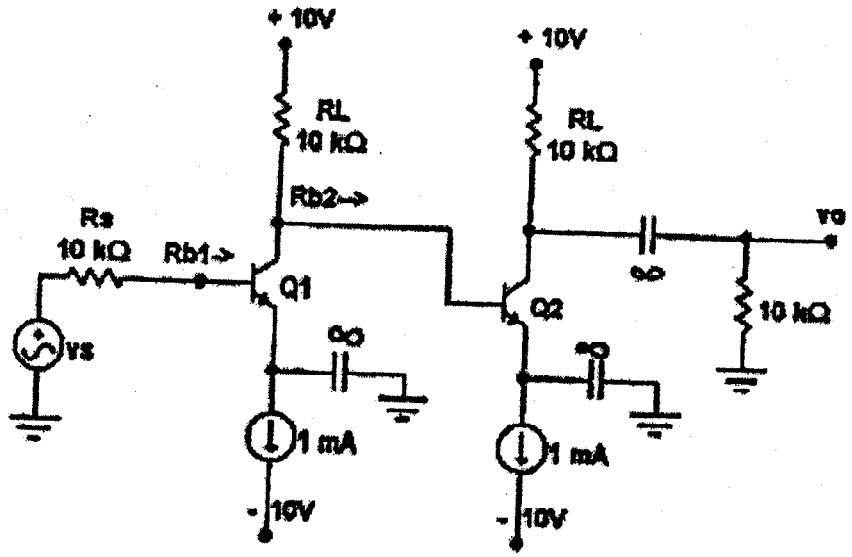


Fig-2



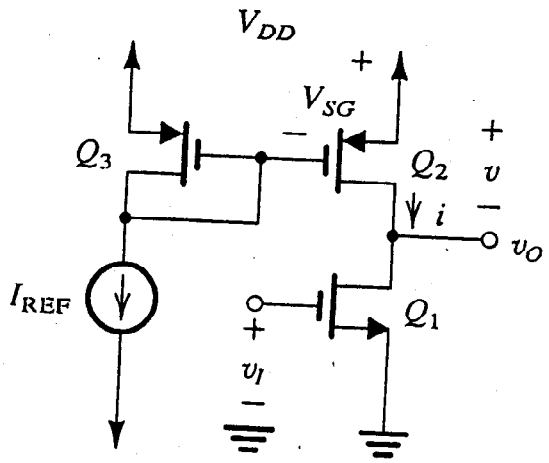


Fig-3

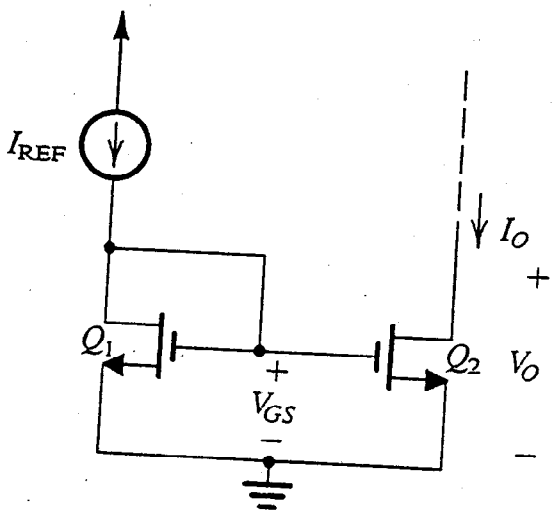


Fig-4

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Yr, 1st semester

MicroElectronic Circuits

(EEE UC424/EEE UC313)

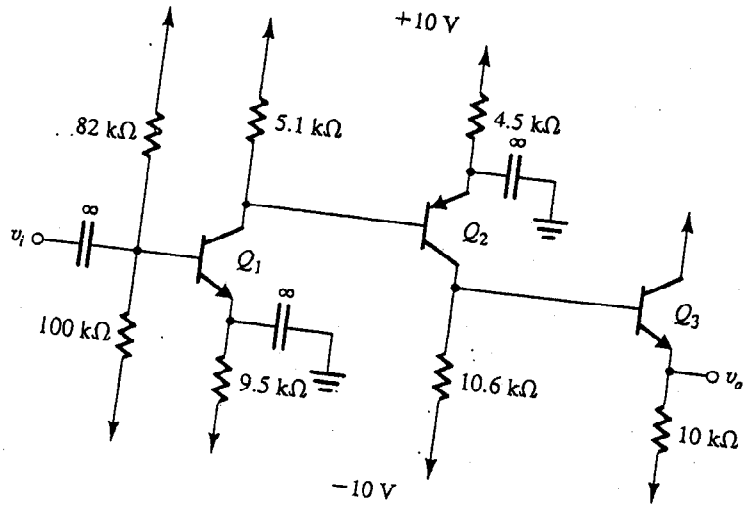
OPEN BOOK

Figure P6.121 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purposes here, we shall assume that the capacitors are sufficiently large to act as perfect short circuits at all signal frequencies of interest.

(a) Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume $|V_{BE}| = 0.7$ V, $\beta = 100$, and neglect the Early effect.

(b) Find the input resistance and the output resistance.

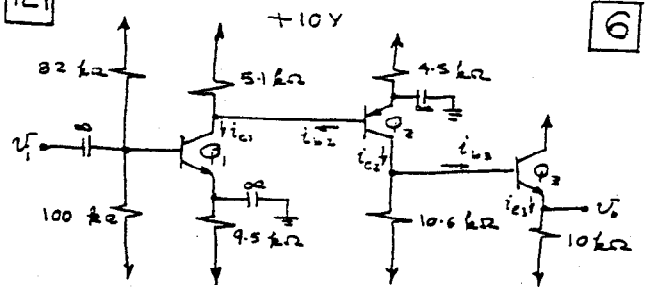
(c) Use the current-gain method to evaluate the voltage gain v_o/v_i.



Quiz solution

MicroElectronics
EEE UC424

12] 6



(a) $I_{E1} = \dfrac{\frac{20}{82+100}\times 100 - 0.7}{9.5 + \frac{(82 \,//\, 100)}{\beta+1}}$, $\beta = 100$

$= 1.03$ mA

$I_{C1} = 1.02$ mA $\quad V_{C1} \simeq 10 - 1.02 \times 5.1 = 4.8$V

$I_{E2} = \dfrac{10 - 0.7 - 4.8}{4.5}$

$= 1$ mA

$I_{C2} = 0.99$ mA

$V_{C2} \simeq 0.99 \times 10.6 - 10 = 0.5$ V

$V_{0DC} = 0.5 - 0.7 = -0.2$ V

$I_{E3} = \dfrac{-0.2 - (-10)}{10} = 0.98$ mA

$I_{C3} = 0.97$ mA

Thus all transistors are operating at $I_C \simeq 1$ mA.

(b) $R_{in} = 82 \,//\, 100 \,//\, r_{\pi 1}$

where $r_{\pi 1} = \dfrac{\beta}{g_{m1}} = \dfrac{100}{40} = 2.5\ k\Omega$

$R_{in} = 82 \,//\, 100 \,//\, 2.5 = 2.37 k\Omega$

$R_{out} = 10\ k\Omega \,//\, \left[r_{e3} + \dfrac{10.6\ k\Omega}{\beta+1} \right]$

$= 10 \,//\, \left[0.025 + \dfrac{10.6}{101} \right]$

$= 128\ \Omega$

(c) $\dfrac{i_{c1}}{v_i} = g_{m1} = 40$ mA/V

$\dfrac{i_{b2}}{i_{c1}} = \dfrac{5.1}{5.1 + r_{\pi 2}} = \dfrac{5.1}{5.1 + 2.5} = 0.671$ A/A

$\dfrac{i_{c2}}{i_{b2}} = \beta_2 = 100$ A/A

$\dfrac{i_{b3}}{i_{c2}} = \dfrac{10.6}{10.6 + (\beta+1)(r_{e3} + 10)}$

$= \dfrac{10.6}{10.6 + 101\,(0.025 + 10)} = 0.01036$ A/A

$\dfrac{i_{e3}}{i_{b3}} = \beta_3 + 1 = 101$

$v_o = i_{e3} \times 10\ k\Omega$

Thus, $\dfrac{v_o}{v_i} = 10 \times 101 \times 0.01036 \times 100 \times 0.671 \times 40$

$= 2.81 \times 10^4$ V/V

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III-Year - 1st SEMESTER 2003-2004
Microelectronic Circuits (EEE UC424/INSTR UC313)
Test-II (Open Book)

Date:14/12/2003
Time: 50 Min
Max Mark: 40

Q1}

For the circuit shown in Fig.1, find the midband gain, the frequency of high- frequency dominant pole, and estimate of f_H using the method of open-circuit time constants, and the frequency of the transfer function zero. Given that β=100, f_T=400MHz, C_μ=2pF, R_L=R_s=1kΩ. (14 Marks)

Q2}

Find the differential mode voltage gain, CMMR, input resistance and output resistance for the amplifier shown in Fig.2, if β_1= β_2= β_3= β_4=100, V_A=89V. Assume the internal resistance for the current source is 750kΩ. (14 Mark)

Q3}

For the circuit shown in Fig.3 all transistors are matched having β=150, f_T=1GHz and C_μ=o.3 pF. Each transistor operates at 150μA emitter current. The collector load resistors are 2.7kΩ. The source resistances are each 10kΩ. Find the midband gain and the upper 3dB frequency. (12 Marks)

Fig. 1

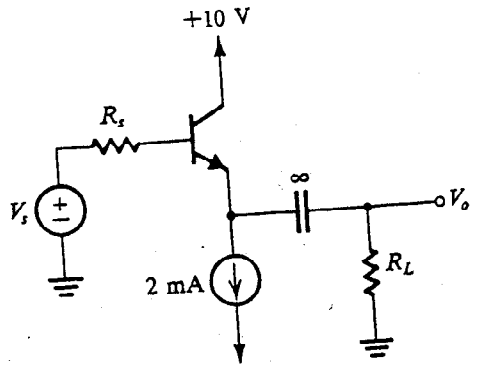


Fig. 2

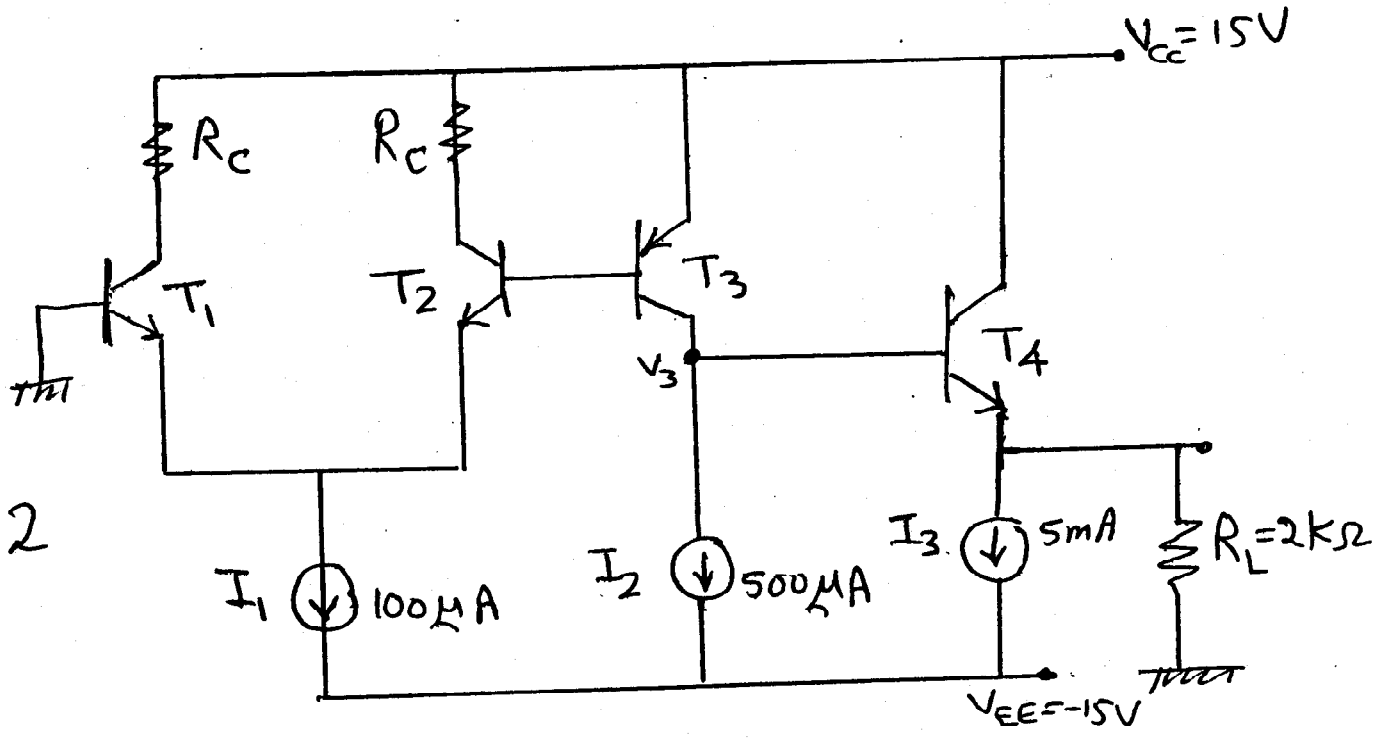
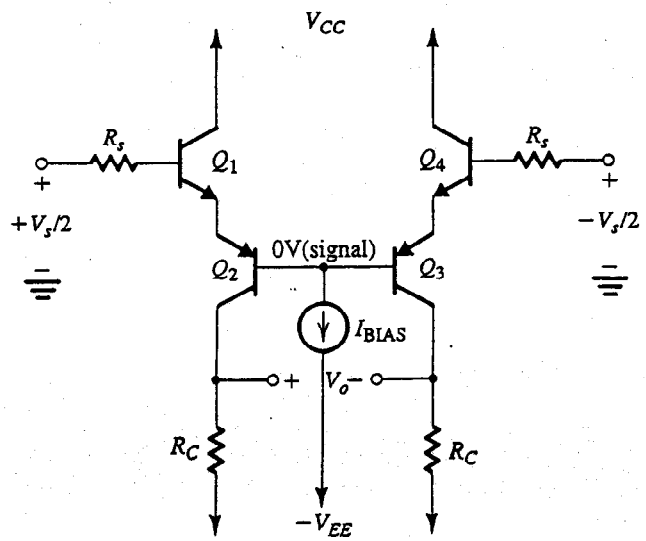


Fig. 3



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III-Year - 1st SEMESTER 2003-2004 | Date: 24/12/2003

Microelectronic Circuits (EEE UC424/INSTR UC313) | Time: 25 Min

Quiz-II | A | Max Mark: 10

A series-shunt feedback amplifier, has an A circuit for which $A = 100$ V/V, $R_i = 10$ kΩ and $R_o = 10$ Ω, and a β circuit with $\beta = 0.1$ V/V, $R_1 = 2$ kΩ and $R_2 = 18$ kΩ. When operating from a zero-impedance source and with no load, what is the overall gain and input and output resistances that result with feedback? If this feedback amplifier is connected between a 0.1 V rms source whose resistance is 10 kΩ and a load of 100 Ω, what does the output voltage become?

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III-Year - 1st SEMESTER 2003-2004

Microelectronic Circuits (EEE UC424/INSTR UC313)

Quiz-II **B**

Date: 24/12/2003

Time: 25 Min

Max Mark: 10

A feedback amplifier connected in the series-series topology uses a basic amplifier having a gain of 900 V/V, an input resistance of 20 kΩ and an output resistance of 1 kΩ, with a feedback network for which β = 50 V/A, R_{11} = 10 kΩ and R_{22} = 200Ω. The amplifier operates between a 10 kΩ source and a 1 kΩ load. Find A, A_f as well as the resistance R_{in} and R_{out} seen by the source and the load.