Max. Marks: 80

Fifth Semester-2003-04

BITS, PILANI – DUBAI CAMPUS

Course No: EEE UC381
Course Title: **Electronic Devices & Integrated Circuits**
Class: BS-III Year (EEE)

COMPREHENSIVE EXAMINATION (CLOSED BOOK)

***Duration:** Three hours*

***Date:** 15/01/04*

Note:

I. **Answer any FIVE questions. All question carry equal marks.**
II. **Question paper contains SIX questions on two pages.**
III. **Used suitable data and constant from the given sheets, otherwise assume data and constant, wherever required.**
IV. **Please return all the enclosed sheets to invigilator(s) after the exams.**
V. **Answer all the parts of the question at one place.**

Q.1 **(a)** Draw an equilibrium band diagram for an abrupt Si P-N junction with the help the data given below.

(i) Indicate fermi level position relative for the intrinsic level on each side.

(ii) Find the contact potential form the diagram .

(iii) Calculate contact potential with the analytical expression.

Given data:

P - side	N- side	
$N_a=10^{17}$ cm^{-3}	$N_d=10^{15}$	T= 300K
$\tau_n=0.1\mu s$	$\tau_p=10\mu s$	$n_i = 1.5 \times 10^{10}$ cm^{-3}
μ_p= 200 cm^2/V-s	μ_n=1300	A=10^{-4} cm^2
μ_n=700	μ_p=450	

[10]

(b) Draw the electron and hole concentration of current versus distance in a forward bias PN junction. **[4]**

(c) What do you understand by Gate Induced Drain Leakage (GIDL) in MOSFET. **[2]**

Q.2 **(a)** Assume the concentration of electron in the conduction band is

$$n_0 = N_c\, e^{-(E_C - E_F)/KT}$$

and the concentration of holes in the valance band is

$$p_0 = N_v\, e^{-(E_F - E_V)/KT},$$

Prove that intrinsic concentration is

$$n_i = (N_C * N_V)^{1/2}\, e^{-E_g/2KT}$$

[10]

(b) Draw the energy band diagram of tunnel diode for the following: (i) Forward bias (ii) Reverse bias (iii) Equilibrium condition.
Indicate clearly all the energy level in the diagram. [6]

Q.3 (a) In a P-type semiconductor the fermi level lies 0.4eV above the valance band. If the concentration of acceptor atoms is tripled, find the new position of the fermi level. Assume KT=0.03eV. Show each fermi level in the energy band diagram. [10]

(b) Discuss in brief the following ICs fabrication steps:
(i) Oxidation (ii) SiO_2 growth (iii) Diffusion [6]

Q.4 (a) Calculate the Threshold voltage of a Si MOS transistor for an n^+ - poly-silicon gate with SiO_2 thickness=50 A^0. $N_d = 10^{18}$ cm^{-3} and fixed charges of $2x\ 10^{10}q$ C/cm^2. It is an enhancement or depletion mode device? (Use ϕ_{ms}=-0.1V, $n_i = 1.5\ x10^{10}$ cm^{-3}, $\varepsilon_i=3.9x8.85x10^{-14}$ F/m, $\varepsilon_s=11.8x8.85x10^{-14}$ F/m) [10]

(b) Discuss the effect of temperature on E_G for Si and Ge. Calculate the value of E_G at room temperature. [4]

(c) Name the materials used for making solar cell. [2]

Q.5 (a) A silicon sample at T=300K contains an acceptors impurity concentration of $N_A=10^{16}cm^{-3}$. Determine the concentration of donor impurity atoms that must be added so that the silicon is N-type and the fermi energy is 0.20eV below the conduction band edge. [8]

(b) Write any four applications of LEDs. [2]

(c) Draw the following schematic diagram for N-type semiconductor;
(i) Energy band diagram (ii) Density of state
(iii) Fermi distribution function [6]

Q.6 **Write notes on *any four*.** [16]

(a) Applications of photo diode.
(b) Explain how optical fiber works?
(c) Write four differences between FET and BJT.
(d) Advantages and disadvantages of ion implantation tech.
(e) Draw the Capacitance-Voltage Characteristics of Ideal MOS.

Max. Marks: 40 Marks Obtained: *First Semester-2003-04*

BITS, PILANI – DUBAI CAMPUS

Course No: EEE UC381
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Class: BS-III Year (EEE)

CLASS TEST-I (CLOSED BOOK)

Roll No. ---------- **Name:**----------
Duration: 50 min. **Date: 26/10/03**

Note: Answer all the questions. Question paper contains *four* questions. Used suitable data and constant from annexure 1-4, otherwise assume data and constant, wherever required.

Q.1 Minority carriers are injected in to a homogeneous N-type semiconductor sample at one point. An electric field of 50V/cm is applied across the sample and the field move these minority carriers a distance of **1cm** in **100 μs.**

Find the drift velocity and the diffusivity of the minority carriers at room temperature. **(10)**

Q.2 An unknown semiconductor has E_G = **1.1 eV** and $N_c = N_v$. It is doped with 10^{15} per cm^3 donors, where the donor level is **0.2 eV** below E_G. Given that E_F is **0.25 eV** below E_C.

Calculate intrinsic concentration and the concentration of electrons and holes in the semiconductor at **300 K**. **(10)**

Q.3 (a) A silicon is doped with 10^{16} arsinic atoms/cm^3. Find the carrier concentration and the fermi level at room temperature (300K). **(7)**

(b) Draw the energy band diagram and show the each fermi-level for part-a. **(3)**

Q.4 Write the answer in brief and to the points. **(10)**

(a) Which PN junction (Si or Ge) has the higher potential barrier to the flow of majority carrier? Show its by characteristics curve. **(2.5)**

(b) Draw schematic band diagram for density of state and carrier concentration for the Intrinsic semiconductor material. **(2.5)**

(c) Draw the energy band diagram, when an electron is excited to the conduction band by optical absorption. **(2.5)**

(d) Why vertical furnace are use in diffusion process of integrated circuits fabrication of PN junction? Name two common impurity sources for diffusion in silicon for Boron. **(2.5)**

SET-I

Max. Marks: 40

First Semester-2003-04

BITS, PILANI – DUBAI CAMPUS

Course No: EEE UC381
Course Title: Electronic Devices & Integrated Circuits
Class: BS-III Year (EEE)

CLASS TEST-II(OPEN BOOK)

Roll No. ---------- **Name:**----------

Duration: 50 min. **Date: 07/12/03**

Note:

i. **Answer all the questions.**
ii. **Question paper contains *four* questions.**
iii. **Mentioned SET-I or SET-II on the front page of the answer sheet.**
iv. **Used suitable data and constants from book, otherwise assume data and constants, wherever required.**

Q.1 (a) A n^+ -p junction diode doped with $N_D=10^{17}cm^{-3}$ and $N_A=5X10^{14}cm^{-3}$. The p-side length and n^+-side length of the diode are $W_p=8\mu m$ and $W_n=50\mu m$, respectively,

(a) On which side (p or n) will be the greater part of the depletion region?
(b) What is the width of the depletion layer under reverse bias of 3V? Assume $V_o=0.7V$.
(c) If the diode has a current of 1mA under a forward bias voltage of 0.5V, what is the reverse saturation current I_o of the device?
(d) Calculate the punch-through voltage of this diode under reverse bias?

Q.2 (a) Calculate the "built in potential" for a silicon PN Junction with $N_a=10^{18}cm^{-3}$ and $N_d=10^{15}cm^{-3}$, $n_i = 9.65 \times 10^9 cm^{-3}$ at 300k. **[10]**

(b) For an ideal MOS (metal $-SiO_2$-Si) diode having $N_a=10^{17}cm^{-3}$. Calculate the maximum width of the surface depletion region at room temperature. **[5]**
$n_i = 9.65 \times 10^9 cm^{-3}$
dielectric permitivity of Si = $11.9 \times 8.85 \times 10^{-14}$F/cm. **[5]**

Q.3 (a) An N^+-P junction with a long p-region has the following properties:

$N_a=10^{16}cm^{-3}$, $D_p=13cm^2/s$,
Current density $J=7A/cm^2$, $T=300k$.

Find the Electric field in the p region far from the junction. **[5]**

(b) Calculate the ideal reverse saturation current in a Si p-n junction diode with a cross-sectional area of $2x10^{-4}cm^2$. The parameters of the diode are:

$N_A=5X10^{16}cm^{-3}$, $N_D=10^{16}cm^{-3}$, $n_i=9.65x10^9cm^{-3}$
$D_n=21cm^2/s$, $D_p=10cm^2/s$, $\tau_p=\tau_n=5x10^{-7}s$.

[5]

Q.4 Explain Why?

(a) MOS devices are generally preferred over that BJT.

(b) Minority carrier concentration on each side of PN junction varies with applied bias.

(c) GaAs is used in place of Si in MESFET.

(d) Why transistor can not be used at MW frequency.

(e) Electron diffusion current is quite large with forward bias.

[10]

Max. Marks: 40 *SET-II*

First Semester-2003-04

BITS, PILANI – DUBAI CAMPUS

Course No: EEE UC381
Course Title: **Electronic Devices & Integrated Circuits**
Class: BS-III Year (EEE)

CLASS TEST-II(OPEN BOOK)

Roll No. ---------- **Name:**----------

Duration: 50 min. **Date: 07/12/03**

Note:

v. **Answer all the questions.**
vi. **Question paper contains *four* questions.**
vii. **Mentioned SET-I or SET-II on the front page of the answer sheet.**
viii. **Used suitable data and constants from book, otherwise assume data and constants, wherever required.**

Q.1 (a) Calculate the "built in potential" for a silicon PN Junction with $N_a = 10^{18} cm^{-3}$ and $N_d = 10^{15} cm^{-3}$, $n_i = 9.65 \times 10^9 cm^{-3}$ at 300k. **[5]**

(b) For an ideal MOS (metal $-SiO_2$-Si) diode having $N_a = 10^{17} cm^{-3}$. Calculate the maximum width of the surface depletion region at room temperature.
$n_i = 9.65 \times 10^9 cm^{-3}$
dielectric permitivity of Si = $12.0 \times 8.85 \times 10^{-14} F/cm$.

Q.2(a) An N^+-P junction with a long p-region has the following properties: **[5]**

$N_a = 10^{16} cm^{-3}$, $D_p = 15 cm^2/s$,
Current density $J = 7 A/cm^2$, T=300k.
Find the Electric field in the p region far from the junction. **[5]**

(b) Calculate the ideal reverse saturation current in a Si p-n junction diode with a cross-sectional area of $2 \times 10^{-4} cm^2$. The parameters of the diode are:

$N_A = 5 \times 10^{16} cm^{-3}$, $N_D = 10^{16} cm^{-3}$, $n_i = 9.65 \times 10^9 cm^{-3}$
$D_n = 21 cm^2/s$, $D_p = 12 cm^2/s$, $\tau_p = \tau_n = 5 \times 10^{-7} s$.

[5]

Q.3 A n^+ -p junction diode doped with $N_D=10^{17}cm^{-3}$ and $N_A=5X10^{14}cm^{-3}$. The p-side length and n^+-side length of the diode are $W_p=10\mu m$ and $W_n=50\mu m$, respectively,

(a) On which side (p or n) will be the greater part of the depletion region?

(b) What is the width of the depletion layer under reverse bias of 3V? Assume $V_o=0.7V$.

(c) If the diode has a current of 1mA under a forward bias voltage of 0.5V, what is the reverse saturation current I_o of the device?

(d) Calculate the punch-through voltage of this diode under reverse bias?

[10]

Q.4 Explain Why?

(a) GaAs is used in place of Si in MESFET.

(b) Electron diffusion current is quite large with forward bias.

(c) Minority carrier concentration on each side of PN junction varies with applied bias.

(d) Why transistor can not be used at MW frequency.

(e) MOS devices are generally preferred over that BJT.

[10]

Max. Marks: 20 Marks Obtained: *First Semester-2003-04*

BITS, PILANI – DUBAI CAMPUS

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QUIZ TEST-I (CLOSED BOOK-)

Roll No. ---------- **Name:**----------

Duration: 15 min. **Date: 28/10/03**

Note: Answer all the questions. Question paper contain *thirteen* questions.

Fill the blanks with appropriate/suitable words. **Marks**

Q.1 The number of distinct energy levels in atomic orbits depends on ---------- **1**

Q.2 Absorption of photons in the visible and IR regions called----------. **1**

Q. 3. What happens to energy gap when atomic spacing decreases? **1**

Q.4 The colour of the light emitted by a phosphors depends upon the----------. **1**

Q.5 Indicate the approximate range of temperature for thermal oxidation of Si to SiO_2 Process. **1**

Q.6 Diffusion current in SC is proportional to-------- **1**
