BITS, PILANI – DUBAI

International Academic City, Dubai
Year III – Semester I 2008 – 2009
Test I (Closed Book)

Course No.: **CS / INSTR C391** Course Title: **DECO**

Date: October 09, 2008 Time: 50 Minutes Max. Marks = 25

(Answer all questions. Calculators are not allowed.)

1. a) Using 2's complement arithmetic perform the operation $(27-63)_{10}$ and explain the result. Use 8 bits binary representation.

   b) Represent the mixed fractional number – 6 *5/8* (neg six and 5/8) in signed binary format

   c) Define the four most important parameters of a digital IC which characterize the logic family. (2 + 1 + 2)

2 The four people in a director board are **A**li, **B**ob, **C**harles and **D**ev. The director board's decision will be made based on the following rule.
If Ali and any one more member vote YES, the decision of the board should be YES. Or if any three of the board members vote YES also the final decision is made YES.

   a) Write the binary truth table showing the possibility of a decision being YES depending on the inputs from the board members. (Assume positive binary logic)

   b) Design a **simplified product of sum expression** for the logic circuit to be implemented to give the decision output **using Boolean algebra.** (2 + 3)

3. a) What is a full adder? Write the truth table of a full adder. Draw the block diagram level representation of a full adder circuit **using two half adders and basic logic gates.**

   b) Design and explain **four bit binary Adder / Subtractor circuit** using four bit binary adder circuit and external logic gates (Use Block diagram representation of four bit binary adder). (3+ 2)

4. a) Prove the following using Boolean algebra

   ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C = A + B'C

   b) Implement the following function along with the don't care conditions, **using no more than two NOR gates.**

   $F(w,x,y,z) = \sum (0,1,2,9,11)$; $d(w,x,y,z) = (8,10,14,15)$; (1.5 + 3.5)

5. Given a Boolean function $Y(A,B,C,D) = \sum (0,2,4,5,6,7,8,10,13,15)$;

   (a) Find all the Prime Implicants for the Boolean function and determine the Essential Prime Implicants

   b) Find the simplified SOP expression for the function.

   c) Realise the simplified SOP expression using NAND gates alone. Assume only true inputs are available. (2 + 1.5 + 1.5)

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BITS, PILANI – DUBAI

International Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: CS C 391/ INSTR C 391 TEST II (Open Book) Course Title: DECO

Date: November 09, 2008 Time: 50 Minutes Max. Marks = 25

(Only text book Morris Mano and handwritten notes are allowed.)

1. Design a decimal to BCD encoder using four OR gates. Switches S0 to S9 indicate the 9 decimal numbers, when an operator presses a push button similar to a switch a high signal will enter the OR gate and produce a BCD number at the output which is the binary equivalent of the decimal number of the switch pressed. (3M)

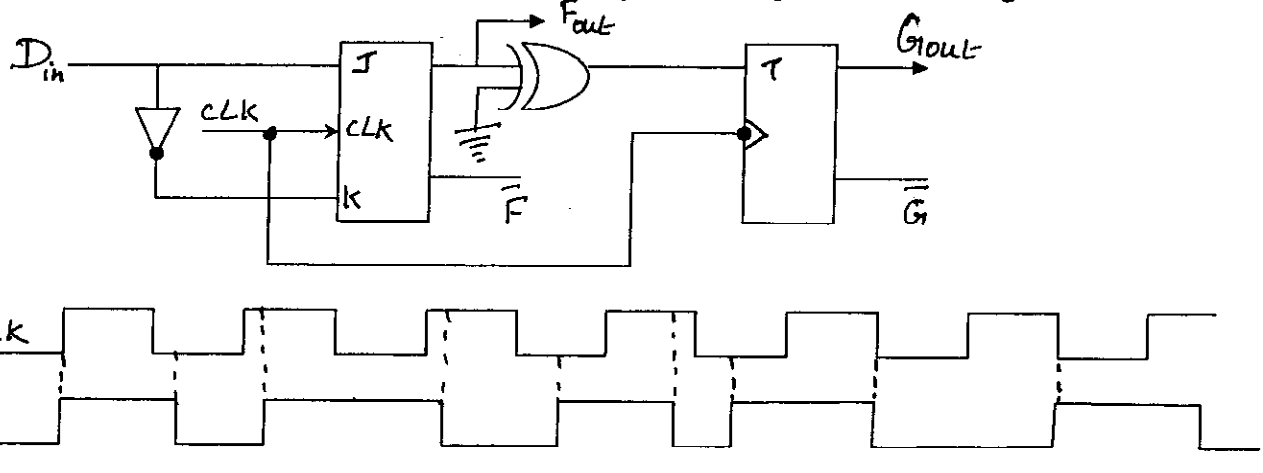
2. Design a comparator , which compares the magnitude of two numbers X and Y , each consisting of two bits and giving three outputs F1, F2, F3 such that :

   F1 = 1, if X > Y otherwise F1 = 0
   F2 = 1, if X = Y otherwise F2 = 0
   F3 = 1, if X < Y otherwise F3 = 0

   a. Draw the block diagram of the above comparator. (1M)
   b. Obtain the expression for F1 using K- Map (3M)

3. Construct a 5-to-32- line decoder with four 3-to8-line decoders with enable and a 2-to-4-line decoder. Use block diagrams for the 3 x 8 decoder. Clearly mark each of the decoder signals. (3M)

4. Given below is a sequential circuit. Draw the out put waveforms for both the flip flops F_{out} and G_{out} for the input waveform shown in the figure with respect to the clock signal.



5. A sequential circuit has two D flip flops A and B and one input x and one output y. The circuit is described by the following next state and output equations.

   $A(t+1) = AB + A'x$; and $B(t+1) = A'B + B'x$ $y = Ax + B'$

   i) Draw the sequential circuit
   ii) Write the state table of the circuit
   iii) Draw the state diagram of the circuit
   iv) What will be the output sequence if the following input sequence (01101001011) is applied to the circuit starting from the state '00'. (2 + 2 + 3 + 3)

QUIZ – 1

Date : 11/9/08 DECO CS C391/ INSTR C391 Weightage : 5%

Name : _____ ID No : _____

1. Convert $(216.321)_{10}$ to octal 1M

2. Convert $(147.C)_{16}$ to binary 0.5M

3. What is the significance of gray code 0.5M

4. Give the 8421 and 84-2-1 code for digits from 2 to 7. 1M

5. Find the complement of the given expression XY' + X' Y 1M

6. Given the Boolean function F= xy+x'y'+y'z implement the function using and , or and inverter gates. 1M

BITS, PILANI – DUBAI

SET A

Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **INSTR C 391** Quiz I Course Title: **DECO**

Date: September 16, 2008 Time: 30 Minutes Max. Marks = 10

All the question carry two marks each

1. Do the following conversion $(7654.123)_{10}$ = (----------)$_2$ = (----------)$_8$
2. Perform the following BCD addition and show the steps 268 + 457
3. Using the two's compliment arithmetic perform the following operation on the given decimal number and prove your answer 52 – 71
4. Find the 9's and 2's compliment of the hexadecimal number 79C0
5. Determine the base of the number for the following operation to be correct 24 + 17 = 40

BITS, PILANI – DUBAI

SET B

Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **INSTR C 391** Quiz I Course Title: **DECO**

Date: September 16, 2008 Time: 30 Minutes Max. Marks = 10

All the question carry two marks each

1. Do the following conversion $(1234.567)_{10}$ = (----------)$_2$ = (----------)$_8$
2. Perform the following BCD addition and show the steps 467 + 258
3. Using the two's compliment arithmetic to perform the following operation on the given decimal number and prove your answer 72 – 91
4. Find the 9's and 2's compliment of the hexadecimal number 70C9
5. Determine the base of the number for the following operation to be correct 24 + 17 = 40

BITS, PILANI – DUBAI

SET C

Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **INSTR C 391** Quiz I Course Title: **DECO**

Date: September 16, 2008 Time: 30 Minutes Max. Marks = 10

All the question carry two marks each

1. Do the following conversion $(1234.765)_{10}$ = (----------)$_2$ = (----------)$_8$
2. Perform the following BCD addition and show the steps 367 + 358
3. Using the two's compliment arithmetic to perform the following operation on the given decimal number and prove your answer 62 – 81
4. Find the 9's and 2's compliment of the hexadecimal number 7C09
5. Determine the base of the number for the following operation to be correct 24 + 17 = 40

Name: _____

ID No: _____

BITS, PILANI – DUBAI

SET A

Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **CS / INSTR C 391** Quiz II Course Title: **DECO**

Date: September 27, 2008 Time: 30 Minutes Max. Marks = 10

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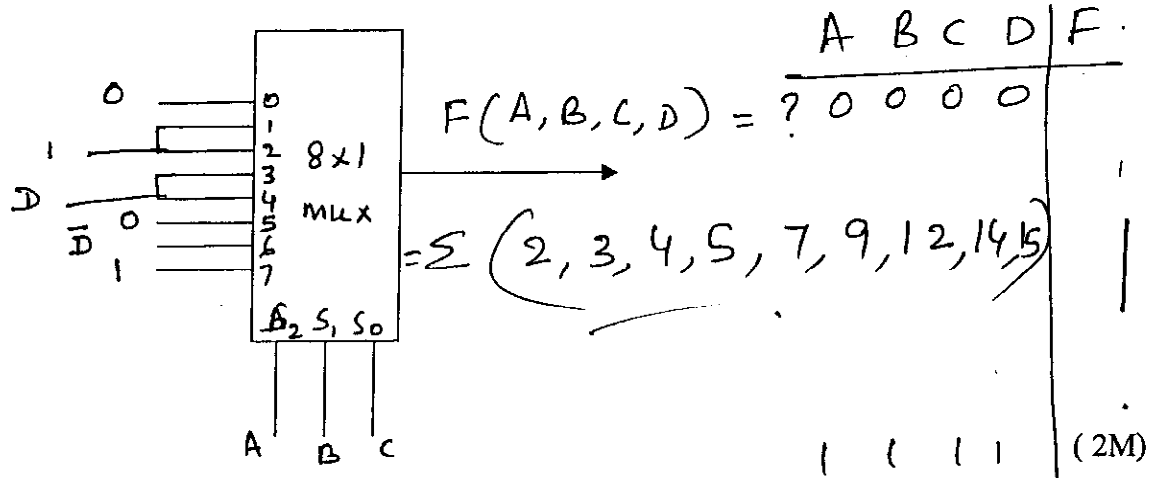
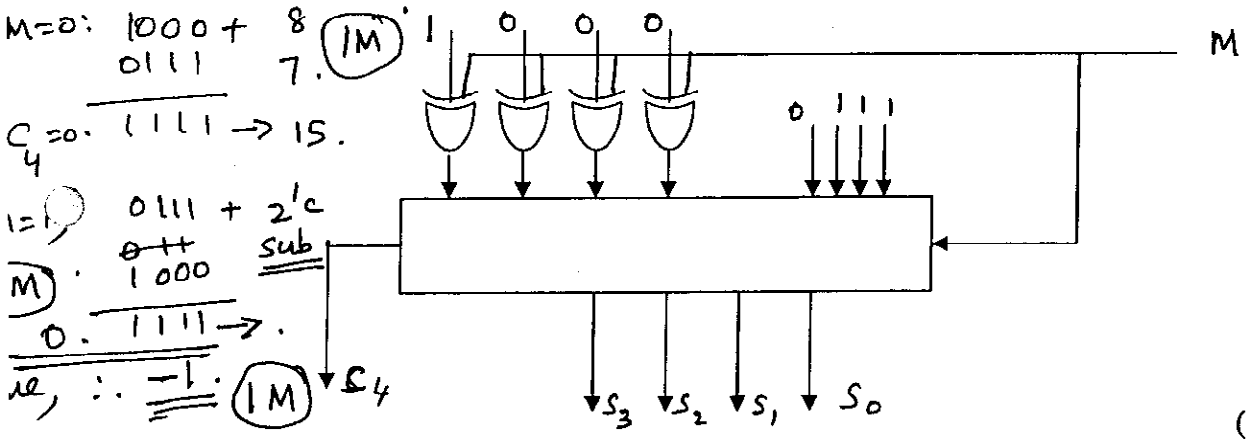
1. Using a 3 x 8 decoder (active low) and minimum number of two input external logic gates implement the following function F(x,y,z) = xy + yz (2M)

2. Find the logic function implemented using the circuit shown below.



(2M)

3. What will be the result of the following circuit operations? Verify your answer in equivalent decimals with Mode bit i) M= 0 ii) M=1 Justify the answers.

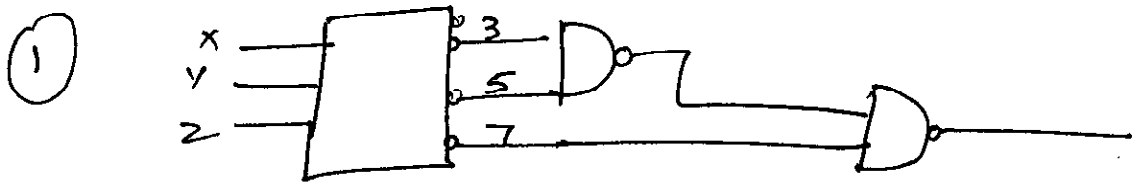


(3M)

4. Write the Boolean expression for a three bit binary word comparator output to be high for the binary word A > B (1.5M)

5. Draw the circuit diagram of a SR flip-flop using NAND gates (1.5M)

********** GOOD LUCK **********



Name: _____

ID No: _____

BITS, PILANI – DUBAI **SET A**

Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **CS / INSTR C 391** Quiz II Course Title: **DECO**

Date: September 27, 2008 Time: 30 Minutes Max. Marks = 10

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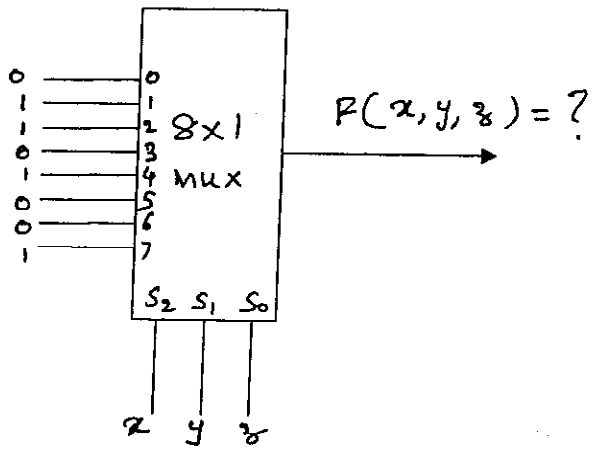
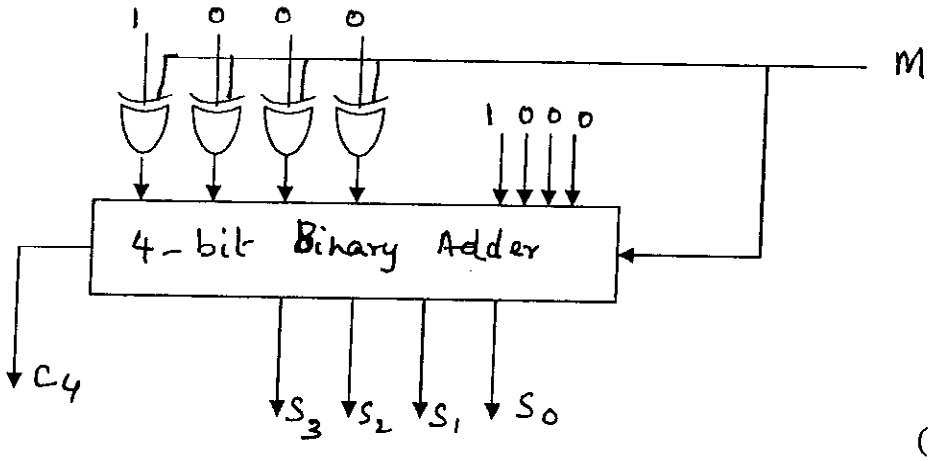
1. Using a 3 x 8 decoder (active low) and minimum number of two input external logic gates implement the following function F(x,y,z) = xz + y'z (2M)
2. Find the logic function implemented using the circuit shown below.



(2M)

3. What will be the result of the following circuit operations? Verify your answer in equivalent decimals with Mode bit i) M= 0 ii) M=1 Justify the answers.



(3M)

4. Write the Boolean expression for a three bit binary word comparator output to be high for the binary word A < B (1.5M)
5. Draw the circuit diagram of a SR flip-flop using NOR gates (1.5M)

********** GOOD LUCK **********

Name :

ID No :

BITS, PILANI – DUBAI

SET C

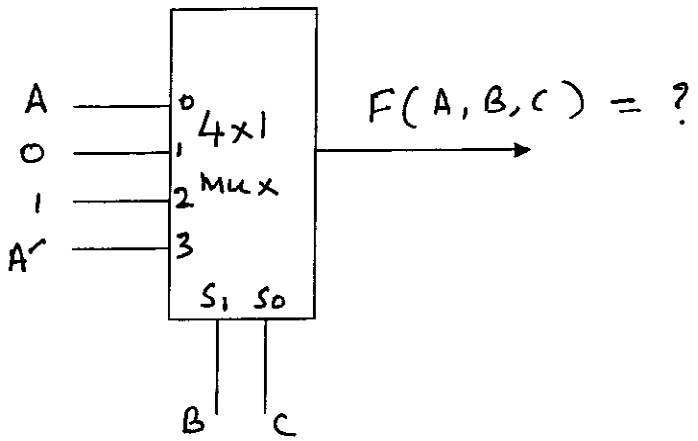
Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **CS / INSTR C 391** Quiz II Course Title: **DECO**

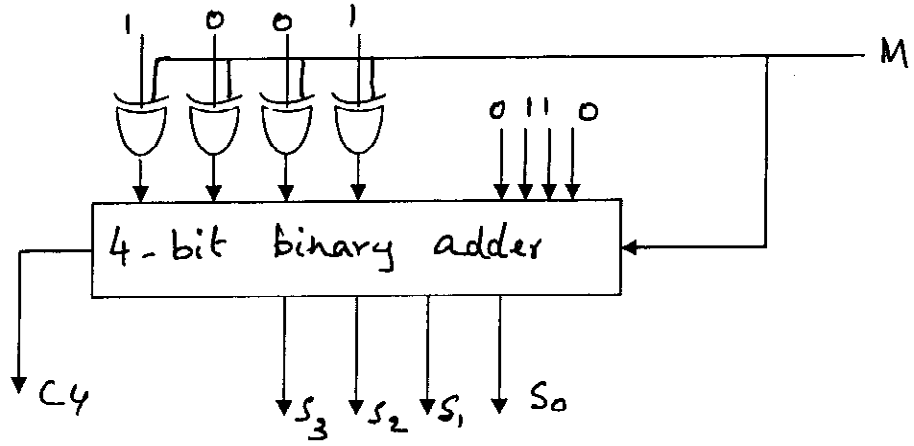
Date: September 27, 2008 Time: 30 Minutes Max. Marks = 10

1. Using a 3 x 8 decoder (active low) and minimum number of two input external logic gates implement the following function F(x,y,z) = xy' + yz' (2M)
2. Find the logic function implemented using the circuit shown below.



(2M)

3. What will be the result of the following circuit operations? Verify your answer in equivalent decimals with Mode bit i) M= 0 ii) M=1 Justify the answers.



(3M)

4. Write the Boolean expression for a three bit binary word comparator output to be high for the binary word A = B (1.5M)
5. Draw the circuit diagram of a D flip-flop using NOR gates (1.5M)

********** GOOD LUCK **********

BITS, PILANI – DUBAI

SET A

Academic City, Dubai

Year III – Semester I 2008– 2009

Course No.: **INSTR C 391** Quiz III Course Title: **DECO**

Date: November 25, 2008 Time: 30 Minutes Max. Marks = 10

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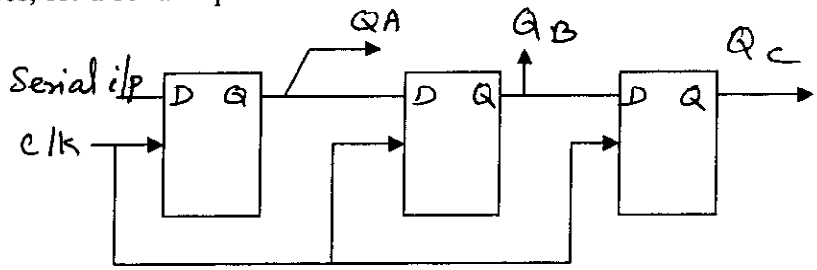
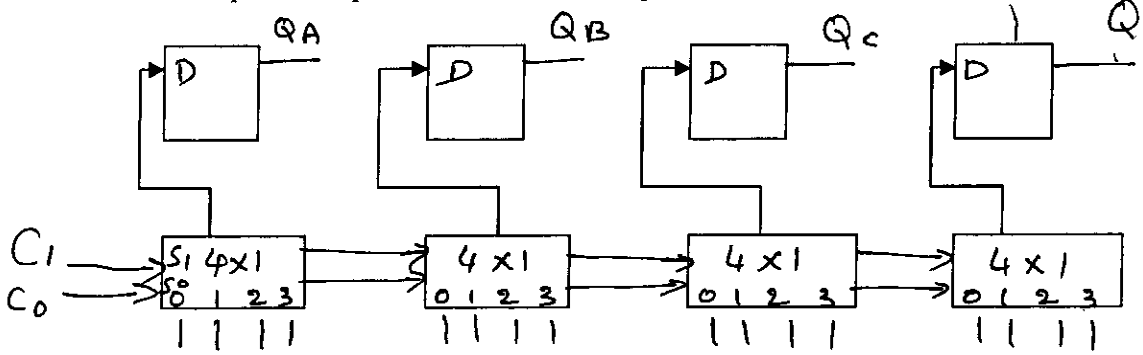
1. Draw the out put wave forms of the shift register shown below with respect to the clock pulses, for a serial input of 1101



2. For the following universal shift register, draw the missing connections at the input of the multiplexer to perform the functions given in the table.



Function table	
C_1 C_0	Fn.
0 0	A → D
0 1	D → A
1 0	clear i/p
1 1	load i/p

3. Design a ROM to implement the function $F(x) = 2x + 3$ where x is a binary 3 bit input and F(x) is given out in binary.

BITS PILANI – DUBAI

DIAC, Dubai

Year III – Semester I 2008– 2009

COMPREHENSIVE EXAMINATION (Closed Book)

Course No.: **CS C 391 / INSTR C 391** Course Title: **DECO**

Date: 23rd December, 2008 Time: 3 hrs Max. Marks = 80

Clearly indicate the assumptions made if any

Answer questions Part A and Part B separately

Calculators are not allowed

PART A

1. i) Write the Boolean expression for the digital logic diagram given in figure 1 below. Also find the simplified expression using Boolean algebra.

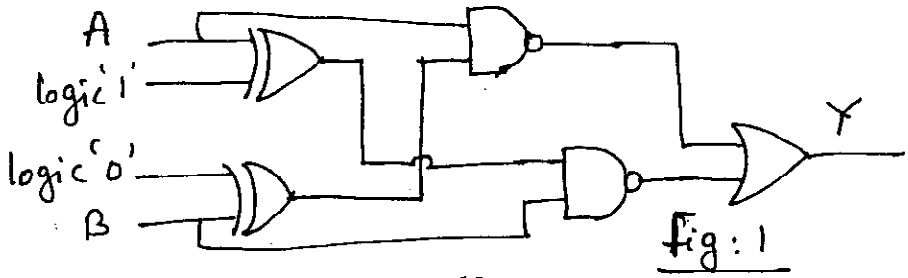


Fig: 1 (1+2M)

ii) Represent the number $-19\frac{13}{16}$ using signed binary number format (2M)

iii) Write the 2's compliment representation of the decimal number -32 using 8-bits (2M)

2. a) Given Boolean function F (w, x, y, z) = Σ (0,2,3,4,7,10,15) and don't care terms d (w, x, y, z) = (6,9,11,13) Using K-Map,

i)) Identify the Prime Implicants

ii) Identify the Essential Prime Implicants

iii) Find the reduced expression in the SOP form

iv) Implement the function using NOR gates alone

(Assume only true inputs are available) (1·5+1·5+2+3 M)

b) A combinational circuit is divided into two sub networks N1 and N2 as shown in figure2.. Network N1 is described by the truth table given in table 1. Redesign each of these sub networks N1 and N2 using minimum number of two input NAND gates

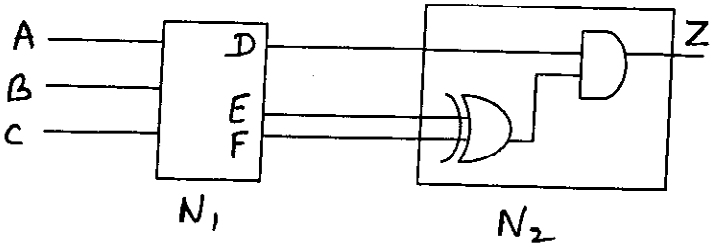


Fig: 2

Table: 1.

A	B	C	D	E	F
0	0	0	0	1	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	1	1
1	1	0	0	1	1
1	1	1	1	0	1

(5M)

3.a) Design a Full Subtractor circuit with three inputs x, y, z and two outputs 'D' the difference and 'B' the borrow. Assume the circuit does x-y-z. 5M

b) A combinational circuit using an 8 x 1 multiplexer is given in figure below. Sketch the outputs Y0 – Y7 for the given conditions of A,B,C. (Note: output of the Demultiplexer is 1 when not selected.

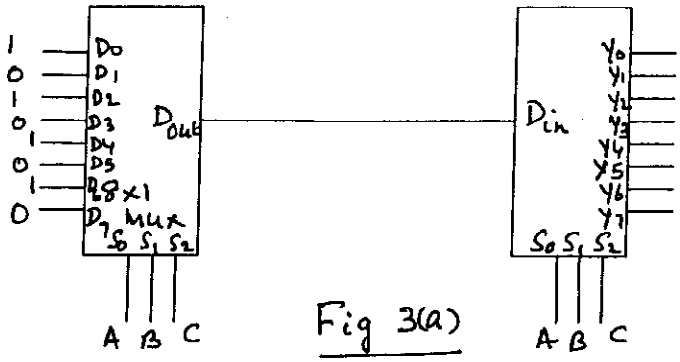
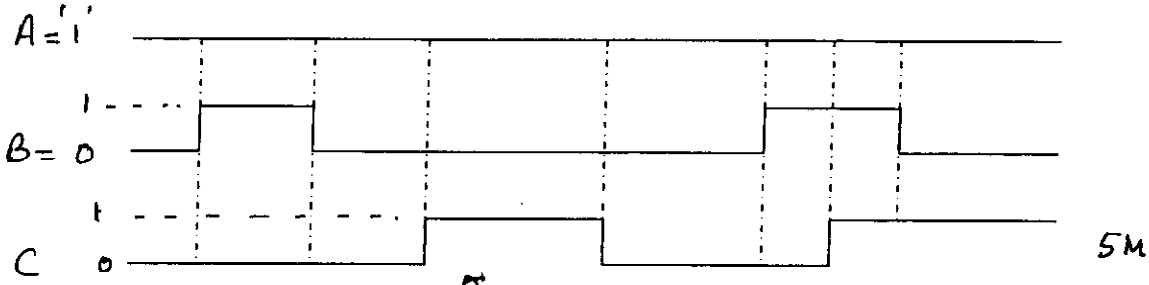


Fig 3(a)



5M

Fig 3(b)

4. a) List the PLA programming table for the BCD to excess-3 code converter. Optimize the no. of product terms for true outputs. 5M

b) The specification of a 7400 IC is given below. Find the Fan-out, Power dissipation, Propagation delay and Noise Margin of the IC

I_{OH} = 1 mA; I_{OL} = 20mA; I_{IH} = 0.05 mA; I_{IL} = 2 mA;
I_{CCH} = 10mA; I_{CCL} = 20 mA; t_{PHL} = 3ns; t_{PLH} = 4ns;
V_{CC} = 5 V; V_{OH} = 2.7 V; V_{OL} = 0.5V; V_{IH} = 2V; V_{IL} = 0.8 V 5M

PART B

5. a. Perform the operation -10 x 9 using Booth's algorithm. Verify your answer. 5M

b. Explain the hardware implementation of the restoration method for division of integers. Show the step by step working of the division operation 13 ÷ 3. 5M

c. Draw the block diagram of a 2 x 4 decoder using NAND gates with an enable pin and give its HDL description. 5M

6. a. Briefly explain the following terms. 3M
   i) Locality of reference with reference to memory.
   ii) Memory Paging.
   iii) UART

b. Explain the different techniques involved in bus arbitration. 2M

7. a. Draw a four bit MOD – 16 binary ripple up counter using JK flip flops, explain its working. Show the timing diagram of this counter. Assume this flip flop is initially in state 0. 5M

b. Design a synchronous counter which counts states 0,1,3,4,6,7 using T flip flops. Assign don't care values for the unused states. 5M

8.a) Determine the functional behavior of the given circuit . Assume that initially a clear signal is given to both the flip flops

i) Draw the state table and plot the waveforms for Q0 and Q1 for 5 cycles. 3M

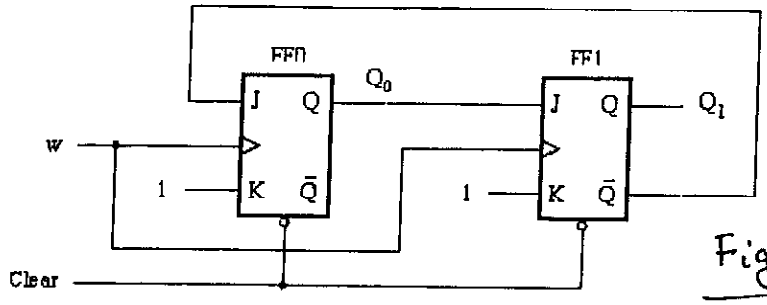


Fig. 4

b) Given the following state table of a Mealy model sequential circuit with one input, one output and four states, develop the following:

a) State diagram
b) Flip Flop input equations (assume that the state memory uses D flip-flops)
c) Output equation
d) Logic diagram

7M

Table : 2

S(t)	S(t+1),z	
	x = 0	x = 1
A	B,0	A,0
B	B,0	C,0
C	D,0	A,0
D	B,0	C,1