BITS PILANI DUBAI CAMPUS
DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI
II SEMESTER 2012-2013
COMPREHENSIVE EXAMINATION

COURSE NO	: **CS / ECE/ EEE/ INSTR F241**	DURATION : 3 HOURS
COURSE NAME	: **Microprocessors and Interfacing**	**II Years**
WEIGHTAGE	: 40% (80 Marks)	
Date	: **04-06-2013** FN	

Calculators are not allowed.
Answer Part A, Part B and Part C in separate answer sheets.

PART-A

1. Write a procedure that multiplies DI by SI and then divides the result by 100H.Make sure that the result is left in AX upon returning from the procedure. This procedure may not change any register except AX. [4M]

2. Suppose that DS=1200H, BX=0100H, and SI=0250H. Determine the address accessed by each of the following instructions, assuming real mode operation
   a) MOV [100H],DL
   b) MOV [SI+100H], EAX
   c) MOV DL,[BX+100H] [3M]

3. Draw the Programming Model of 8086 through the Core 2 microprocessors including 64-bit extensions. Which Flag bit controls the INTR pin on the microprocessors. Mention the states of the flag when INTR pin is enabled and disabled. [4M]

4. Convert the following
   a) Binary 11101.11101 to decimal
   b) Octal (521.7) to decimal
   c) Decimal .057986 to hexadecimal [1.5M]

5. Explain why the following assembly language constructs are incorrect. [2.5M]

   a) MOV CX, #4
   b) POP CS
   c) MOV ES, 1234H
   d) MOV ES, DS
   e) MOV BX, DL

6. Express the following sequence of instructions in assembly language. [5M]
   a) Copies CX into AX
   b) Copies 0000H into SI
   c) Copies the byte contents of the data segment memory location addressed by the sum of BX, DI and 20H into DH
   d) Removes a quad word from the stack and places it into the RAX register
   e) Copies the word contents of the data segment memory location addressed by BX on to the stack

7. Write an assembly language program to reverse the bits of a byte. [5M]

PART-B

1. a. Expand the following macro. [3M]

```
MyMacro   MACRO  p1, p2, p3
          MOV AX, p1
          MOV BX, p2
          MOV CX, p3
ENDM
MyMacro   1, 2, 3
MyMacro   4, 5, DX
RET
```

   b. Write an assembly program using macro to display the string "DUBAI" on the monitor. Display one character a time using DOS interrupt function. [4M]

2. a. Why do we need to demultiplex the buses in 8086 processors? [1M]

   b. If the crystal oscillator is operating at 24MHz, What will be the CLK and PCLK output of 8284A (Clock generator). [2M]

   c. Explain with diagram Demultiplexing of 8086 microprocessor. [4M]

3. a. Write an assembly program to find the highest among 5 grades and write it in DL. [5M]

   b. If AX = 5, multiply AX by 63 without using MUL or loop instruction. [2M]

   c. Develop a sequence of instructions that clear bits 0 and 1; set bits 6 and 7 and invert bit 5 of AX. [2M]

4. Draw the block diagram of 8254 (Programmable Interval Timer) and mention the different modes of operation. [4M]

5. Write the sequence of events that occur when one or more interrupt request lines go high in 8259 (Programmable Interrupt Controller). [3M]

PART-C

1. Draw the generalized block diagram for the memory device 2764 EPROM of size 8Kbytes showing address, data and control selections. [2 M]

2. Show how simple NAND gate decoder is used to select 16K EPROM. [2 M]

3. Draw the pin-out and truth table of the 74LS139, dual 2-to-4 line decoder. [3 M]

4. Write any two differences between static RAM and dynamic RAM. [2 M]

5. How is the memory banks selected in the 8086 processors. [2M]

6. The interfacing for connecting eight EPROM in parallel on a common address bus and common data bus in a certain system is done as follows:

   Address bits A13, A14, and A15 of 8086 are connected to A, B and C of 74LS138 (3X 8 decoder).
   A12 address bit is connected to $\overline{G2A}$ of 74LS138. $\overline{RD}$ control signal is connected to $\overline{G2B}$ of 74LS138. A19, A18, A17, A16 are all connected to G1 of 74LS138 through AND gate.
   Remaining address bits i.e. A0-A11 of 8086 are directly connected to each EPROM.

   Draw the schematic of the interfacing and prepare the address decoder worksheet showing address decoding for the eight EPROMS. [6 M]

7. Write an assembly language program to transfer 10 bytes of data from location DATA1 to DATA2 using string instruction. [4 M]

8. Explain with neat diagram the operation of the 8257 DMA controller. [2 M]

9. What are the modes and input-output configurations for PORT A, B, and C of an 8255 PPI after its control word register is loaded with 80H? [2 M]

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COURSE NAME	: **Microprocessors and Interfacing**	**II Years**
WEIGHTAGE	: 40% (80 Marks)	
Date	: **04-05-2013** FN	

Answering Scheme. Part - A

1. Progarm 4M

2. a) DSX10H+100=12000+100=12100 3X1=3M
   b) SI+100=0250+100=0350 = 12.000 + 0350 = 12.350
   c) DSx10+BX+100=12000+0100+100=12200

3. Drawing 2M
   The Interupt I FLAG 1M
   I=1, INTR pin is enabled ,I=0, INTR pin is disabled 1M

4. a) 39.906 1.5M
   b) 337.875
   c) (0.0ED6C)

5. a) MOV CX, #4 #is not used 2.5M
   b) POP CS not allowed. Next address partially changing.
   c) direct data cannot be moved to ES
   d) MOV ES, DS segment to segment not allowed
   e) Mixed sizes not allowed

6. a) MOV AX,CX 5M
   b) MOV SI,0
   c) MOV DH, [BX+DI+20H]
   d) POP RAX
   e) PUSH WORD PTR[BX]

7. mov cx,1 ;will move and shift 1 bytes 5M
   reverse_next_byte:

```
mov bl,al        ;move low AX byte to low BX byte
shl bx,8         ;shift low BX byte to next high position
shr ax,8         ;place next high EAX byte in low position
loop reverse_next_byte
mov bl,al        ;move the highest AX byte into low BX byte
mov ax,bx        ;return the result to EAX
```

Part-B

Q: a)

```
mov   AX,  0001H
mov   BX,  0002H
mov   CX,  0003H
mov   AX,  0004H
mov   BX,  0005H
mov   CX,  DX
```

(4M)

b)

```
.model small
.code
disp  macro  var
      mov    dl, var
      mov    ah, 6
      int    21h
endm
.startup
      disp   'D'
      disp   'U'
      disp   'B'
      disp   'A'
      disp   'I'
.exit
end
```

(4M)

2. a.

Memory and I/o require that the address remains valid and stable throughout a read or write cycle. If the buses are multiplexed, the address changes at the memory and I/o, which causes them to read or write data in the wrong locations. (1M)

b. 24 MHz

$$CLK = \frac{24}{3} = 8 \text{ MHz}$$

$$PCLK = \frac{24}{6} = 4 \text{ MHz}.$$

(2M)

c. 8086 MP with demultiplexed address bus

Diagram

(4M)

3.a.

```
.model small
.data
data db 51, 44, 99, 88, 80

mov cx, 5
mov bx, offset data
sub al, al

again : cmp al, [bx]
        ja next
        mov al, [bx]

next : inc bx
       loop again
       mov dl, al

.exit
end
```

5M

(4)

3. b. (2M)

```
MOV   BX, AX
SHL   AX, 6
SUB   AX, BX
```

5. c. (3M)

```
AND   CX, 0FCH
OR    CX, 0C0H
XOR   CX, 020H
```

4. Block diagram of 8254 (2M)

Different modes of operation (1M)

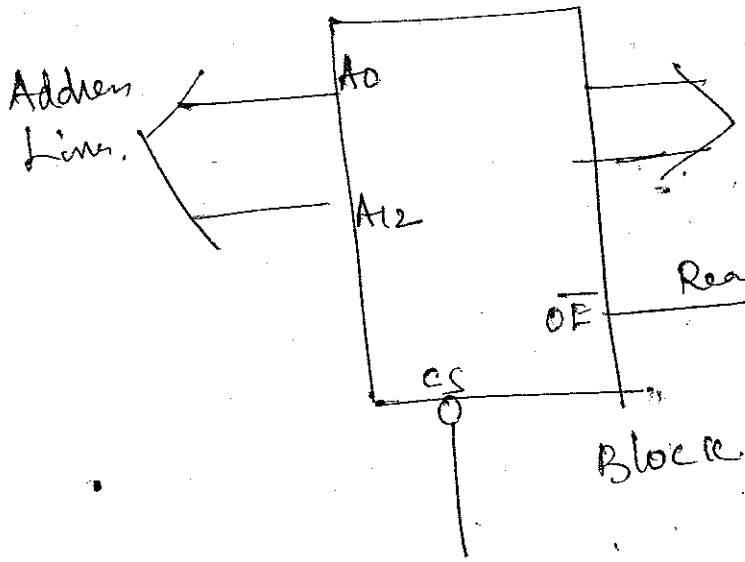
5. Sequence of events that occur when 1/more interrupt request lines go high in 8259 (2M)

Part-C

(1)

8 K bytes = $2^3 \cdot 2^{10}$ = 13 address Lines

$A_0 - A_{12}$

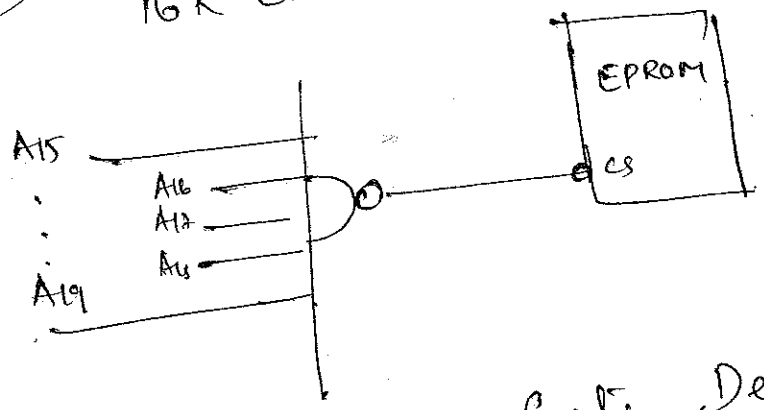


(2M)

Block diagram of Memory device

(2)

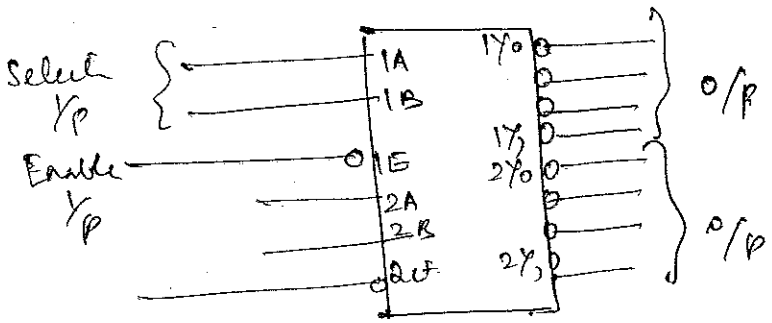
16 K EPROM = 14 address Lines,



[2M]

Simple Nand Gate Decoder to select 16 K EPROM.

(3) Pinout of 74LS139.



[1.5 M]

E	A	B	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0
1	X	X	1	1	1	1

[1.5 M]

[2 M]

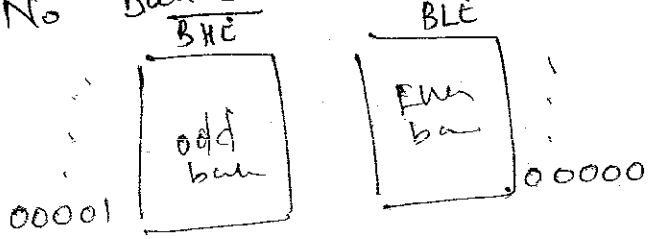
(4)

S. Ram	D. Ram
Volatile Memory. → temporary data	Retains data 2 or 4 ms
smaller size.	Larger size.

[2 M]

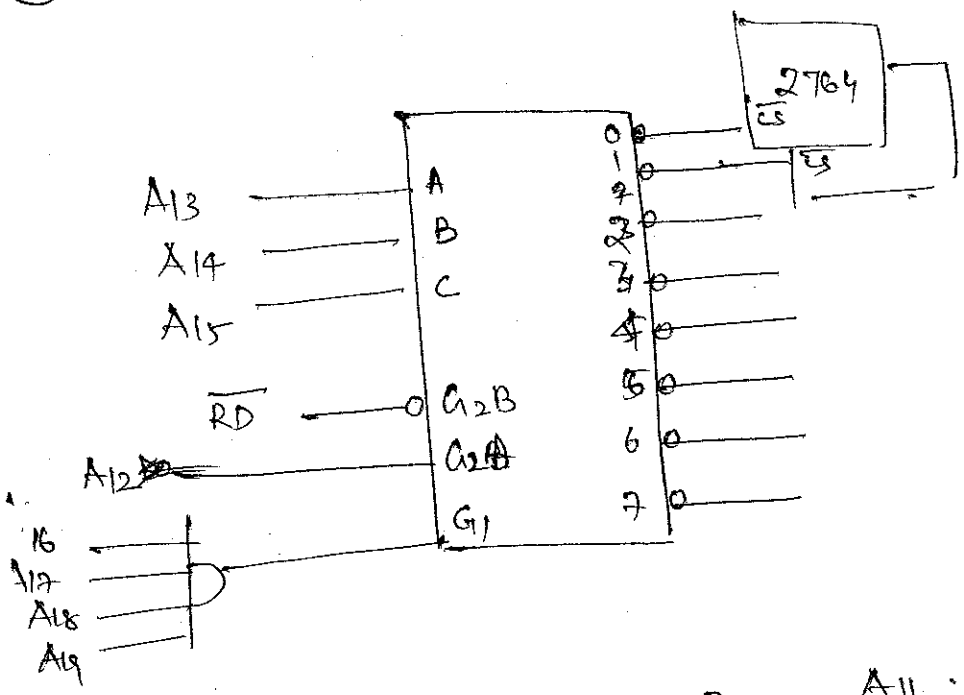
(5)

$\overline{BHE}$	$\overline{BLE}$	
0	0	Both banks enabled
0	1	High Bank "
1	0	Low "
1	1	No bank "



(6)

[6M]



A19 ... A16	A15	A14	A13	A12	A11 ... A0	
1 1 1 1	0	0	0	0		
	0	0	1	0	F0000 — F0FFF	
	0	1	0	0	F2000 — F2FFF	
	0	1	1	0	F4000 — F4FFF	
	1	0	0	0	F5000 — F5FFF	
					F8000 — F8FFF	Address Ranges
					FA000 — FAFFF	
					FC000 — FCFFF	
					FE000 — FEFFF	

A15 A14 A13 A12

0 0 0 0 = 0
0 0 1 0 = 2
0 1 0 0 → 4
0 1 1 0 → 5
1 0 0 0 → 8
1 0 1 0 → A
1 1 0 0 → C
1 1 1 0 → E

(7)

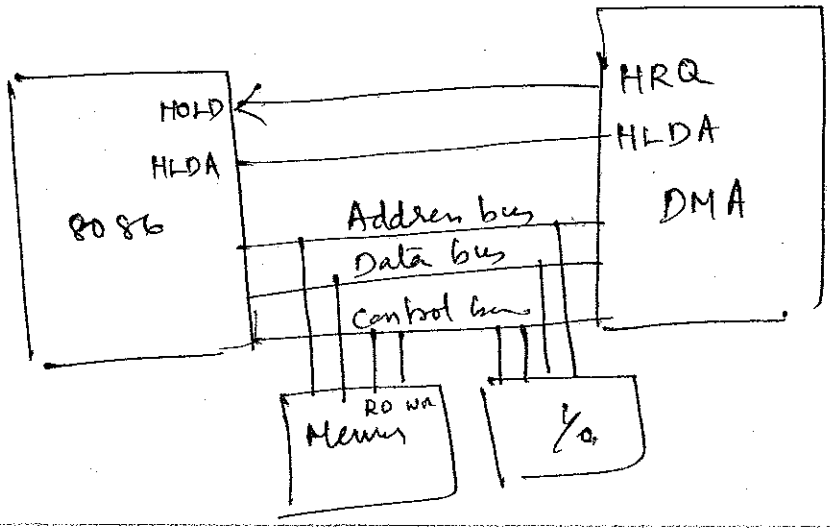
```
MOV   SI, OFFSET DATA1
MOV   DI, OFFSET DATA2
CLD
MOV   CX, 10
REP   MOVSB
```

[4M]

(8)

8257 DMA Controller

[2M]



(9)

[2M]

8255 PPI

Control word 80

1 000 | 0000

all port A, B, and C as output ports

→ parallel Input output mode.

(not BSR)

BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai
Year II – Semester II 2012– 2013
Test II Open Book

Course No.: **EEE/ECE/CS/INSTR F 241** Course Title: Microprocessors and Interfacing
Date: 29.04.13 Time: 50 Minutes Max. Marks = 40

(Answer all questions.)

1. Compare macro and procedure. (Any 4 differences in tabular column) [4M]

2. Write an assembly program using procedure to move a block of data of size 10 bytes from the memory location **SOURCE** to memory location **DEST** using string instruction. [8M]

3. Explain what **SBB [DI-4], DX** Instruction accomplishes [3M]

4. Where is the least significant 32 bits of the product stored for the Instruction given below. Mention the total width of the result.
   MUL EDI [2M]

5. Develop a sequence of instructions that scans through 500H –byte section of memory called BEST, located in the data segment, searching for a 55H, also write the code for number of occurrences of 55H in the specified memory section and store the count at the end of 500H-byte. [8M]

P.T.O

6. Write the instructions that will invert leftmost 6 bits and rightmost 6 bits of the register DX. Every step must be shown. [3M]

7. Implement the following Pseudocode in assembly language. [6M]

```
If (bx <= cx)
{
ax=5;
dx=6;
}
```

8. Write a program to Replace the number in AX by its absolute value.
[Hint: absolute value of -5 = 5] [6M]

Test-2

Marking Scheme

Microprocessor & Interfacing

Marks: 40.

1. Macro : procedure.

→ No call statement.

→ No return address.

→ Codes b'cause lengthy.

→ Less Time.

2. MOV SI, offset SOURCE

MOV DI, offset DEST.

CLD

MOV CX, 10

MOVSB.

3. [DI − 4] + DS. → DX Substracted from this.

(4) EDX – EAX.

(5). MOV AX, 55H.

MOV the offset of BEST to SI.

Scan Using SCASB instruct whenever feild match, increment the count.

XOR → to invert

(6)

7. CMP bX, CX.

JZ
MOV AX, 5
Mov dx, 6.

8. CMP & AX, 0
if less than 0, xply by –1

BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai
Year II – Semester II 2012– 2013
Test I

Course No.: **EEE/ECE/CS/INSTR F 241** Course Title: Microprocessors and Interfacing

Date: 11.03.13 **Time: 50 Minutes** **Max. Marks = 40**

(Answer all questions. Calculators are not allowed.)

1. Convert the following to decimal (3 * 2 = 6 Marks)

   a) Binary 101011.010

   b) octal 767.0

   c) Hexadecimal AC.D

2. Convert the following binary –coded Hexadecimal numbers to Hexadecimal

   100101011111110 . 1100001 (2 Marks)

3. Draw the conceptual view of microprocessors 80486 and Pentium 4. (2 Marks)

4. In the real mode, show the starting and ending addresses of each segment located by the segment register values: (2 * 2.5 = 5 Marks)

   a. CABDH
   b. DACFH

5. Determine the memory location addressed by the following real mode 80286 register combinations: (2 * 2.5 = 5 Marks)

   a. SS = 3900H, SP = 2B00H, IP = 2000H
   b. CS = 2A50H, SP = 2B00H, IP = 354FH

6. What flag bits will be affected when you perform 8EH+ DCH? Show the detailed working. (5 Marks)

7. Identify the type of jump, for the following set of instructions. (3 Marks)

JMP 10H
JMP 2000H
JMP WORD PTR [DI]

8. Write a assembly program, to add alternate elements of an array TABLE of size 6. (6 Marks)

9. Write the machine code for the instruction given below using 16 bit instruction mode for Pentium4 microprocessor. [Refer to the tables given below for the same]
MOV WORD PTR [EBX+20], 8765H (6 Marks)

Code	*W=0 (Byte)*	*W=1 (Word)*	*W=1 (Doubleword)*
000	AL	AX	EAX
001	CL	CX	ECX
010	DL	DX	EDX
011	BL	BX	EBX
100	AH	SP	ESP
101	CH	BP	EBP
110	DH	SI	ESI
111	BH	DI	EDI

R/M Code	*Function*
000	DS:[EAX]
001	DS:[ECX[
010	DS:[EDX]
011	DS:[EBX]
100	Uses scaled-index byte
101	SS:[EBP]*
110	DS:[ESI]
111	DS:[EDI]

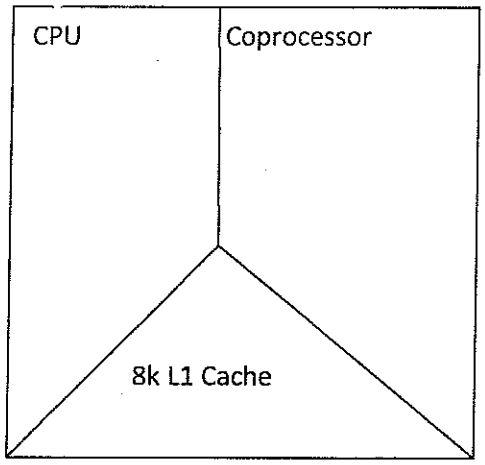
Course No : **EEE/ECE/CS/INSTR F 241** Course Title: **Microprocessors and Interfacing**

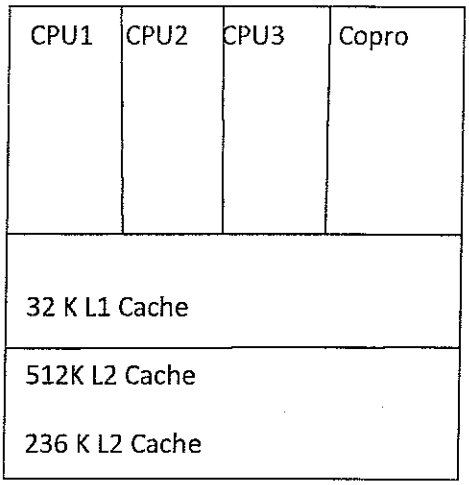
Answering Scheme for TEST 1

1. a) 43.25
   b) 503.0
   c) 172.06

2. 4AFE. C4

3.





4. (2 * 2.5 = 5 Marks)

   a. CABDH

      Starting address = CABD0H 1M

      Ending address = DABCFH 1.5M

   b. DACFH

      Starting address = DACF0H 1M

      Ending address = E9CEFH 1.5M

5. (2 * 2.5 = 5 Marks)

a. SS = 3900H, SP = 2B00H, IP = 2000H

SS:SP

SS*10 + SP 1M

= 39000 + 2B00
= 3BB00H 1.5M

b. CS = 2A50H, SP = 2B00H, IP = 354FH

CS:IP
CS*10 + IP 1M
= 2A500 + 354F
= 2DA4FH 1.5M

6. (5 Marks)

8E 1000 1110

DC 1101 1100

0110 0010 (carry = 1) 2.5 M

7. a) short jmp 3M

b) Near jmp
c) Indirect jmp

8. Array declaration with name and size. [1 M]
Use Base plus Index addressing mode [1 M]
Change Index register to add alternate elements [2 M]
Logic to Add [2 M]

9. 66 67 C7 43 20 65 87 6 M

ID NO: ---------- SEC----------

NAME: ----------

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Dubai International Academic City, Dubai

Year II – Semester II 2012– 2013

QUIZ I

SET A

Course No.: **EEE/ECE/CS/INSTR F 241** Course Title: **Microprocessors and Interfacing**

Date: 25.03.13 **Time: 20 Minutes** **Max. Marks = 10**

1. Initialize the stack memory from address 9000h: 1000h [1 Mark]

2. Save data of register AX, BX, CX, DX into stack memory and transfer back the data from stack memory into corresponding registers [2 Mark]

3. The default segment of memory for DI is ----------and for SI is ---------- [1 Mark]

4. What will be the content of SS and SP after executing the instruction? LSS SP, [BX] when BX= 1000 and DS=1000 and data present in data segment memory is as shown in fig. [2 Mark]

data	address
30	11004
00	11003
12	11002
7A	11001
55	11000

5. If the value of EAX register is 12345678H, what will be its value after executing the instruction BSWAP EAX? [1 Mark]

6. What will be stored in AX register, when the instruction MOVSX AX, AL is executed? Initially AL = 9CH. [1 Mark]

7. Write an instruction that adds the word contents of the data segment memory location addressed by TEMP plus ESI from DI and stores the sum in DI. [1 Mark]

8. Write the operands involved in MOVS instruction. [1 Mark]

ID NO: ---------- SEC----------

NAME: ----------

BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai

Year II – Semester II 2012– 2013

QUIZ I

SET A

Course No.: **EEE/ECE/CS/INSTR F 241** Course Title: **Microprocessors and Interfacing**

Date: 25.03.13 **Time: 20 Minutes** **Max. Marks = 10**

1. Initialize the stack memory from address 9000h: 1000h [1 Mark]

```
MOV AX, 9000
MOV SS, AX
MOV SP, 1000
```

2. Save data of register AX, BX, CX, DX into stack memory and transfer back the data from stack memory into corresponding registers [2 Mark]

```
PUSH AX        POP DX
PUSH BX        POP CX
PUSH CX        POP BX
PUSH DX        POP AX
```

3. The default segment of memory for DI is ---------- Extra ----------and for SI is ---------- Data ---------- [1 Mark]

4. What will be the content of SS and SP after executing the instruction? LSS SP, [BX] when BX= 1000 and DS=1000 and data present in data segment memory is as shown in fig. [2 Mark]

data	address
30	11004
00	11003
12	11002
7A	11001
55	11000

SP : 7A 55

SS : 00 12

1000 ∪
100

5. If the value of EAX register is 12345678H, what will be its value after executing the instruction BSWAP EAX? [1 Mark]

78 56 34 12

6. What will be stored in AX register, when the instruction MOVSX AX, AL is executed? Initially AL = 9CH. [1 Mark]

AX : 009C

7. Write an instruction that adds the word contents of the data segment memory location addressed by TEMP plus ESI from DI and stores the sum in DI. [1 Mark]

← TEMP[ESI] + DI

ADD DI, Temp[ESI]

8. Write the operands involved in MOVS instruction. [1 Mark]

SI & DI