BIRLA INSTITIUE OF TECHNOLOGY AND SCIENCE PILANI, DUBAI

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

SECOND SEMESTER 2012-2013

Course No: **EEE F244 ECE F244 INSTR F244**	Course Name: **MICROELECTRONIC CIRCUITS**
Evaluation component: **COMPREHENISVE EXAMINATION**	Date & Time: 10TH JULY 2013, WEDNESDAY 12:30 PM – 03:30 PM
Weightage : **40%**	Max marks :**80**
Duration: **3 HOURS** **ANSWER PART A & PART B IN SEPARATE ANSWER BOOK**	Note : ***Answer all the question, assume any missing data suitably***

PART A

Q.1 [5+(1+1)+3=10M]

It is required to couple a voltage source V_s with a resistance R_s to a load R_L via a capacitor ***C.***

A. Derive an expression for the transfer function from source to load (i.e., V_L/V_S).

B. Offering a Justification, Identify which Single Time Constant (STC) i.e., either a highpass or a lowpass type is this expression?

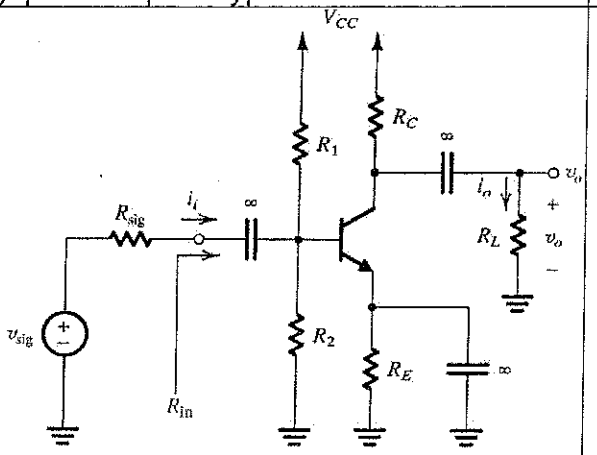
C. For R_s = *15* kΩ and R_L = 60 kΩ, find the (smallest/largest) coupling capacitor that will result in a 3-dB cut-off frequency no (greater/lesser) than 500 Hz, depending on whether the transfer function is, respectively, highpass/lowpass type.

Q.2 [3+3=6M]

For the common-emitter amplifier shown below, let V_{cc} = ***10V***, R_1 = ***33 kΩ***, R_2= 20 k***Ω*** ,R_E= ***1.5 kΩ***, and R_C = 2.7 k***Ω***. The transistor has β = 150 and V_A = 125 V.

A. Calculate the dc bias current I_E.

B. Assuming R_{sig}= 15 k***Ω*** and R_L= 1.5 k***Ω*** , draw the small signal ac equivalent Circuit by replacing the device with its hybrid-π: model.



Q.3 [6+2+3+(2+1)=14M]

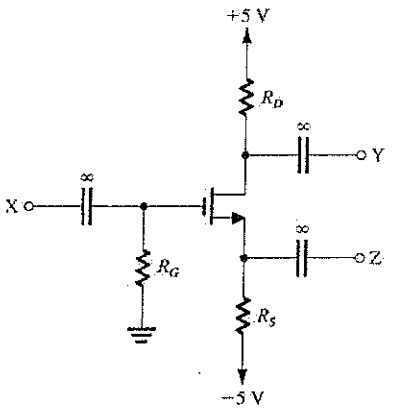
The MOSFET in the circuit of Fig. below has V_t =1.5 V, k'_nW/L = 0.6 mA/V^2 , and V_A= 30V. Find

A. the values of R_s, R_D, and R_G so that I_D = 0.2 mA; if the circuit conditions are: (i)the largest possible value for R_D is used while (ii) a maximum signal swing at the drain of ±1.5 V is possible, and (iii)the input resistance at the gate is 9 MΩ.

B. the values of g_m and r_o at the bias point.

C. the voltage gain from signal source to load; if the circuit conditions are: (i)terminal Z is grounded, (ii)terminal X is connected to a signal source whose internal resistance is 0.8MΩ, and (iii)terminal Y is connected to a load resistance of 30 kΩ,.

D. The voltage gain from X to Z with Z open-circuited and also its output resistance assuming terminal Y is grounded? – Also identify Configuration of this Amplifier circuit.



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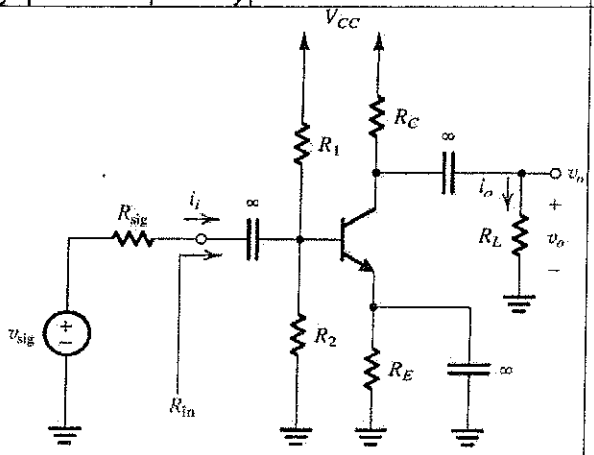

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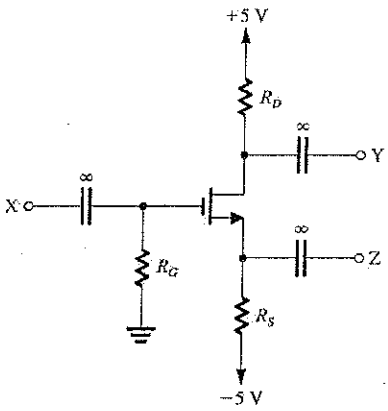

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PART B

Q.1 Draw the circuit diagram of MOS differential amplifier with a common mode input voltage v_{CM}. Derive an expression for V_{OV} and V_{GS}. [10M]

Let $V_{DD}=V_{SS}=1.5V$, $k'_n(W/L)=4mA/V^2$, $V_t=0.5V$, $I=0.4mA$ and $R_D=2.5k\Omega$.

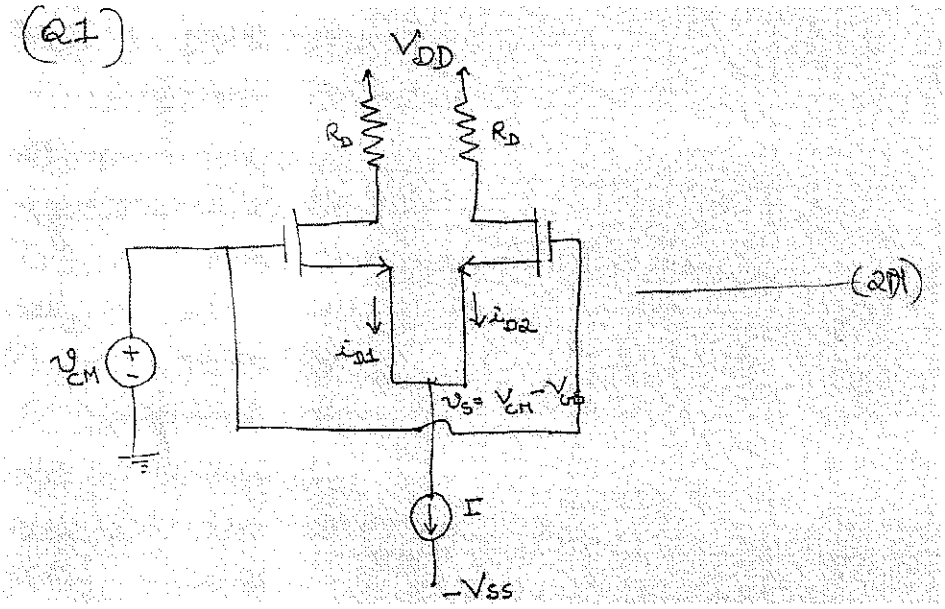
Find the following for MOS differential amplifier with common mode input

a) V_{OV} and V_{GS}

b) For $V_{CM}=0$, find v_S(voltage at source), i_{D1},i_{D2}, v_{D1},v_{D2}

c) For $V_{CM}=+1V$, find v_S(voltage at source), i_{D1},i_{D2}, v_{D1},v_{D2}

(Q1)



$$V_{OV}=\sqrt{\frac{I}{k'_n(W/L)}} \quad \text{(1M)}$$

$$V_{GS}=V_t+V_{OV} \quad \text{(1M)}$$

(a) $V_{OV}=0.316V$ (1M)

$V_{GS}=0.82V$ (1M)

(b) $v_s = -0.82V$
$i_{D1} = 0.2mA$
$i_{D2} = 0.2mA$
$v_{D1} = +1V$
$v_{D2} = +1V$ (2M)

(c) $v_s = 0.18V$
$i_{D1} = 0.2mA$
$i_{D2} = 0.2mA$
$v_{D1} = +1V$
$v_{D2} = +1V$ (2M)

Q.2 Draw the neat circuit diagram of bipolar Op-Amp and briefly explain each stage in this multistage amplifier. [10M]

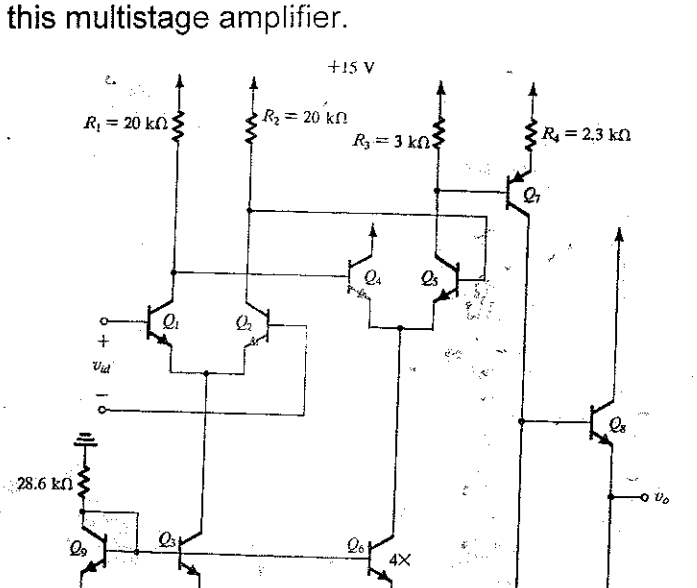


FIGURE 7.43 A four-stage bipolar op amp.

Q.3 With the use of a general structure of the feedback amplifier, derive an expression for closed loop gain and prove the folowing properties of negative feed back [10M]

a) Gain Desensitivity
b) Bandwidth Extention
c) Noise Reduction
d) Reduction in Nonlinear Distortion

8.1 THE GENERAL FEEDBACK STRUCTURE

Figure 8.1 shows the basic structure of a feedback amplifier. Rather than showing voltages and currents, Fig. 8.1 is a **signal-flow diagram,** where each of the quantities x can represent either a voltage or a current signal. The *open-loop* amplifier has a gain A; thus its output x_o is related to the input x_i by

$$x_o = Ax_i \qquad (8.1)$$

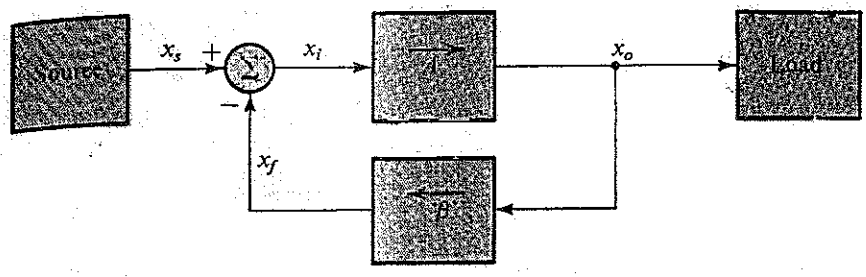


FIGURE 8.1 General structure of the feedback amplifier. This is a signal-flow diagram, and the quantities x represent either voltage or current signals.

The output x_o is fed to the load as well as to a feedback network, which produces a sample of the output. This sample x_f is related to x_o by the **feedback factor** β,

$$x_f = \beta x_o \tag{8.2}$$

The feedback signal x_f is *subtracted* from the source signal x_s, which is the input to the complete feedback amplifier,[1] to produce the signal x_i, which is the input to the basic amplifier,

$$x_i = x_s - x_f \tag{8.3}$$

Here we note that it is this subtraction that makes the feedback negative. In essence, negative feedback reduces the signal that appears at the input of the basic amplifier.

Implicit in the description above is that the source, the load, and the feedback network *do not* load the basic amplifier. That is, the gain A does not depend on any of these three networks. In practice this will not be the case, and we shall have to find a method for casting a real circuit into the ideal structure depicted in Fig. 8.1. Figure 8.1 also implies that the forward transmission occurs entirely through the basic amplifier and the reverse transmission occurs entirely through the feedback network.

The gain of the feedback amplifier can be obtained by combining Eqs. (8.1) through (8.3):

$$A_f \equiv \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \tag{8.4}$$

The quantity $A\beta$ is called the loop gain, a name that follows from Fig. 8.1. For the feedback to be negative, the loop gain $A\beta$ should be positive; that is, the feedback signal x_f should have the same sign as x_s, thus resulting in a smaller difference signal x_i. Equation (8.4) indicates that for positive $A\beta$ the gain-with-feedback A_f will be smaller than the open-loop gain A by the quantity $1 + A\beta$, which is called the **amount of feedback.**

If, as is the case in many circuits, the loop gain $A\beta$ is large, $A\beta \gg 1$, then from Eq. (8.4) it follows that $A_f \simeq 1/\beta$, which is a very interesting result: *The gain of the feedback amplifier is almost entirely determined by the feedback network.* Since the feedback network usually consists of passive components, which usually can be chosen to be as accurate as one wishes, the advantage of negative feedback in obtaining accurate, predictable, and stable

8.2.1 Gain Desensitivity

The effect of negative feedback on desensitizing the closed-loop gain was demonstrated in Exercise 8.1, where we saw that a 20% reduction in the gain of the basic amplifier gave rise to only a 0.02% reduction in the gain of the closed-loop amplifier. This sensitivity-reduction property can be analytically established as follows:

Assume that β is constant. Taking differentials of both sides of Eq. (8.4) results in

$$dA_f = \frac{dA}{(1+A\beta)^2} \tag{8.7}$$

Dividing Eq. (8.7) by Eq. (8.4) yields

$$\frac{dA_f}{A_f} = \frac{1}{(1+A\beta)} \frac{dA}{A} \tag{8.8}$$

which says that the percentage change in A_f (due to variations in some circuit parameter) is smaller than the percentage change in A by the amount of feedback. For this reason the amount of feedback, $1+A\beta$, is also known as the **desensitivity factor.**

8.2.2 Bandwidth Extension

Consider an amplifier whose high-frequency response is characterized by a single pole. Its gain at mid and high frequencies can be expressed as

$$A(s) = \frac{A_M}{1+s/\omega_H} \tag{8.9}$$

where A_M denotes the midband gain and ω_H is the upper 3-dB frequency. Application of negative feedback, with a frequency-independent factor β, around this amplifier results in a closed-loop gain $A_f(s)$ given by

$$A_f(s) = \frac{A(s)}{1+\beta A(s)}$$

Substituting for $A(s)$ from Eq. (8.9) results, after a little manipulation, in

$$A_f(s) = \frac{A_M/(1+A_M\beta)}{1+s/\omega_H(1+A_M\beta)} \tag{8.10}$$

Thus the feedback amplifier will have a midband gain of $A_M/(1+A_M\beta)$ and an upper 3-dB frequency ω_{Hf} given by

$$\omega_{Hf} = \omega_H(1+A_M\beta) \tag{8.11}$$

It follows that the upper 3-dB frequency is increased by a factor equal to the amount of feedback.

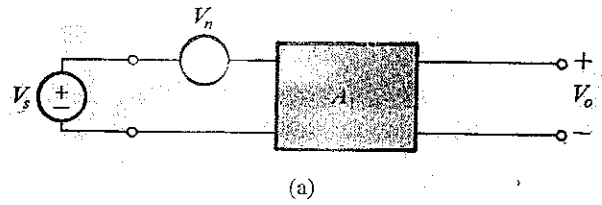
Similarly, it can be shown that if the open-loop gain is characterized by a dominant low-frequency pole giving rise to a lower 3-dB frequency ω_L, then the feedback amplifier will have a lower 3-dB frequency ω_{Lf},

$$\omega_{Lf} = \frac{\omega_L}{1+A_M\beta} \tag{8.12}$$

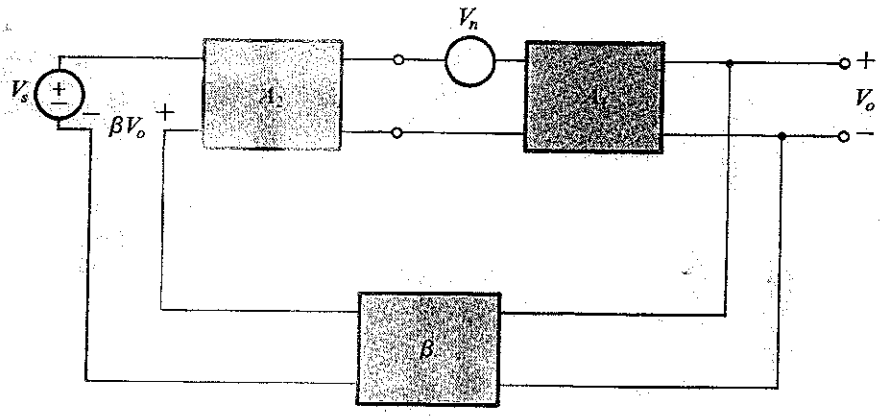
Note that the amplifier bandwidth is increased by the same factor by which its midband gain is decreased, *maintaining the gain–bandwidth product at a constant value.*

8.2.3 Noise Reduction

Negative feedback can be employed to reduce the noise or interference in an amplifier or, more precisely, to increase the ratio of signal to noise. However, as we shall now explain, this noise-reduction process is possible only under certain conditions. Consider the situation illustrated in Fig. 8.2. Figure 8.2(a) shows an amplifier with gain A_1, an input signal V_s, and noise, or interference, V_n. It is assumed that for some reason this amplifier suffers from noise and that the noise can be assumed to be introduced at the input of the amplifier. The



(a)



(b)

signal-to-noise ratio for this amplifier is

$$S/N = V_s/V_n \tag{8.13}$$

Consider next the circuit in Fig. 8.2(b). Here we assume that it is possible to build another amplifier stage with gain A_2 that does not suffer from the noise problem. If this is the case, then we may precede our original amplifier A_1 by the *clean* amplifier A_2 and apply negative feedback around the overall cascade of such an amount as to keep the overall gain constant. The output voltage of the circuit in Fig. 8.2(b) can be found by superposition:

$$V_o = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta} \tag{8.14}$$

Thus the signal-to-noise ratio at the output becomes

$$\frac{S}{N} = \frac{V_s}{V_n} A_2 \tag{8.15}$$

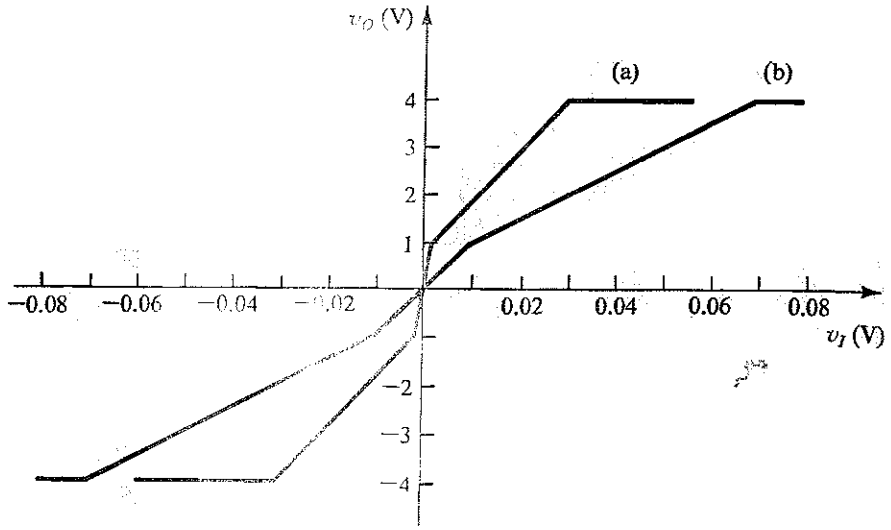
which is A_2 times higher than in the original case.

We emphasize once more that the improvement in signal-to-noise ratio by the application of feedback is possible only if one can precede the noisy stage by a (relatively) noise-free stage. This situation, however, is not uncommon in practice. The best example is found in the output power-amplifier stage of an audio amplifier. Such a stage usually suffers from a problem known as **power-supply hum.** The problem arises because of the large currents that this stage draws from the power supply and the difficulty in providing adequate power-supply filtering inexpensively. The power-output stage is required to provide large power gain but little or no voltage gain. We may therefore precede the power-output stage by a small-signal amplifier that provides large voltage gain, and apply a large amount of negative feedback, thus restoring the voltage gain to its original value. Since the small-signal amplifier can be fed from another, less hefty (and hence better regulated) power supply, it will not suffer from the hum problem. The hum at the output will then be reduced by the amount of the voltage gain of this added preamplifier.

8.2.4 Reduction in Nonlinear Distortion

Curve (a) in Fig. 8.3 shows the transfer characteristic of an amplifier. As indicated, the characteristic is piecewise linear, with the voltage gain changing from 1000 to 100 and then to 0. This nonlinear transfer characteristic will result in this amplifier generating a large amount of nonlinear distortion.

The amplifier transfer characteristic can be considerably **linearized** (i.e., made less nonlinear) through the application of negative feedback. That this is possible should not be too surprising, since we have already seen that negative feedback reduces the dependence of the overall closed-loop amplifier gain on the open-loop gain of the basic amplifier. Thus large



To illustrate, let us apply negative feedback with $\beta = 0.01$ to the amplifier whose open-loop voltage transfer characteristic is depicted in Fig. 8.3. The resulting transfer characteristic of the closed-loop amplifier is shown in Fig. 8.3 as curve (b). Here the slope of the steepest segment is given by

$$A_{f1} = \frac{1000}{1 + 1000 \times 0.01} = 90.9$$

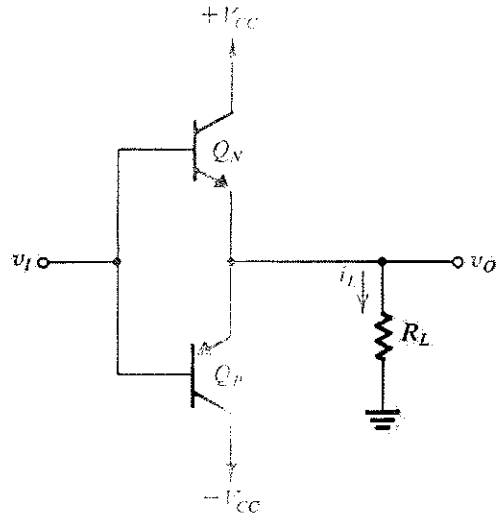
and the slope of the next segment is given by

$$A_{f2} = \frac{100}{1 + 100 \times 0.01} = 50$$

Thus the order-of-magnitude change in slope has been considerably reduced. The price paid, of course, is a reduction in voltage gain. Thus if the overall gain has to be restored, then a preamplifier should be added. This preamplifier should not present a severe nonlinear-distortion problem, since it will be dealing with smaller signals.

Finally, it should be noted that negative feedback can do nothing at all about amplifier saturation, since in saturation the gain is very small (almost zero) and hence the amount of feedback is also very small (almost zero).

Q.4	a) Draw the circuit diagram of Class B output stage amplifier and derive the expression for Power conversion efficiency.	[5+5=10M]



- Complementary Pair (an npn, Q_N and a pnp, Q_P)
- PUSH PULL Operation - Only one conducts at a time – Q_N pushes (sources) into load Q_P pulls (sinks) from load
- Biased at zero current active devices conduct only when signal is present

$$\eta = \left(\frac{1}{2}\frac{V_{o-peak}^2}{R_L}\right) \div \left(\frac{2}{\pi}\frac{V_{o-peak}}{R_L}V_{CC}\right)$$

$$= \frac{\pi}{4}\frac{V_{o-peak}}{V_{CC}} \Rightarrow \eta_{max} = 78.5\%$$

$$P_{Dmax} = \frac{2}{\pi^2}\frac{V_{CC}^2}{R_L}$$

b) A BJT is specified to have a maximum power dissipation P_{D0} of 3W at an ambient temperature T_{A0} OF 25°C , and maximum junction temperature T_{Jmax}=200°C. Find the following

i. The thermal resistance θ_{JA}

ii. The maximum power that can be safely dissipated at an ambient temperature of 60°C

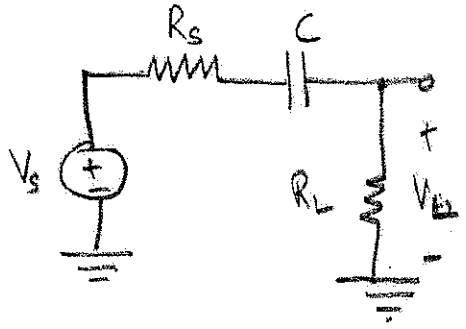
iii. The junction temperature if the device is operating at T_A=30°C and is dissipating 0.5W of power.

$$i)\ \theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{D0}} = \frac{200-25}{3} = 58.33^\circ C/W$$

$$ii)\ P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}} = \frac{200-60}{58.33} = 2.4W$$

$$iii)\ T_J = T_A + \theta_{JA}P_D = 30 + 58.33x0.5 = 59.16^\circ C$$

Q1) Using the voltage divider rule.



$$\frac{V_o}{V_s} = \frac{R_L}{R_L + R_s + \frac{1}{sC}}$$

$$= \frac{R_L}{R_L + R_s} \cdot \frac{s}{s + \frac{1}{C(R_L + R_s)}}$$

Which is T.F. of the high pass STC type (see Table 1.2 of Text book)

$$K = \frac{R_L}{R_L + R_s} \quad ; \omega_o = \frac{1}{C(R_L + R_s)}$$

For $f_o \leq 500$ Hz.

$$\frac{1}{2\pi C(R_L + R_s)} \leq 500$$

$$\frac{1}{2\pi C(60+15)\times 10^3} \leq 500$$

$$C \geq \frac{1}{2\pi \times 500 \times (60+15\times 10^3}$$

$$C \geq 4.244 \times 10^{-9} F$$

min value of C = 4.244 nF.

Q2) $V_{CC} = 10V$; $R_1 = 33K\Omega$; $R_2 = 20K\Omega$ $R_E = 1.5K\Omega$ $R_C = 2.7K\Omega$

$B = 150$, $V_A = 125V$

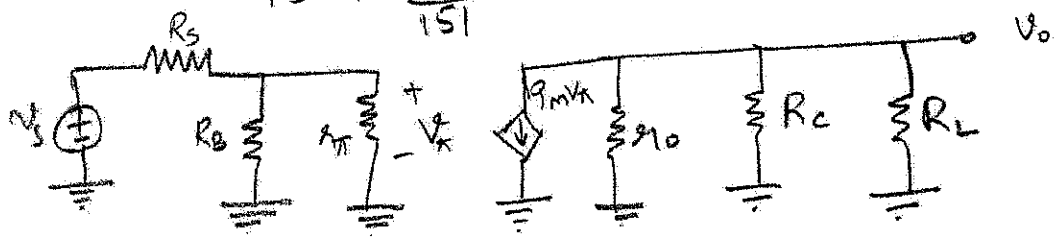
$R_{sig} = 15K\Omega$ $R_L = 1.5K\Omega$.

a) $I_E = \dfrac{V_{BB} - V_{BE}}{R_E + R_B/(B+1)}$

where $V_{BB} = V_{CC} \cdot \dfrac{R_2}{R_1 + R_2} = 10 \cdot \dfrac{20K}{33K+20K} = 3.77V$

$R_B = R_1 \| R_2 = 33 \| 20 = 12.45K\Omega$

Thus $I_E = \dfrac{3.77 - 0.7}{1.5K + \frac{12.45K}{151}} = 1.94mA$.



$g_m = \dfrac{I_C}{V_T} = \dfrac{\alpha I_E}{V_T} = \dfrac{0.99 \times 1.94}{0.025} \simeq 76.8 \dfrac{mA}{V}$

$r_\pi = \dfrac{B}{g_m} = \dfrac{150}{76.8 \times 10^{-3}} = 1.953K\Omega$

$r_o = \dfrac{V_A}{I_C} = \dfrac{125}{0.99 \times 1.94 \times 10^{-3}} = 65.08 \times 10^3 \Omega$

Q3) $V_t = 1.5V$ $K_n' W/L = 0.6 mA/V^2$ $V_A = 30V$

a) $I_D = 0.2 \times 10^{-3} = \frac{1}{2} \times 0.6 \times 10^{-3} \times V_{ov}^2 \Rightarrow V_{ov} = 0.816V$

$V_{GS} = 1.5 + 0.816 = 2.316V$

$V_G = 0 \Rightarrow V_S = -2.316V$

$R_S = \frac{-2.316 - (-5)}{0.2} = 13.42K\Omega$

$V_{DS} = 5 - R_D$

Largest possible R_D is achieved for $V_{DS\,min}$

$V_{DS} \geq V_{GS} - V_t \Rightarrow V_{DS\,min} - V_{ov} \Rightarrow V_{DS} - 1 = V_{ov}$

$\Rightarrow V_{DS} = 1.5 + 0.816 = 2.316V \Rightarrow R_D = \frac{5 - 2.316}{0.2} = 13.42K\Omega$

$R_G = 10M\Omega$

b) $g_m = \frac{2I_D}{V_{ov}} = \frac{2 \times 0.2}{0.816} = 0.49\ mA/V$; $R_o = \frac{V_A}{I_D} = \frac{30}{0.2} = 150K\Omega$

c) If z is grounded then the ckt becomes a common-source config.

The voltage gain according to Eq 4.82.

$G_v = \frac{-R_G}{R_G + R_{sig}} g_m (r_o \| R_D \| R_L) = \frac{9^M}{9^M + 0.8^M} \times 0.49 \times 10^{-3} (150^K \| 13.42^K \| 30^K)$

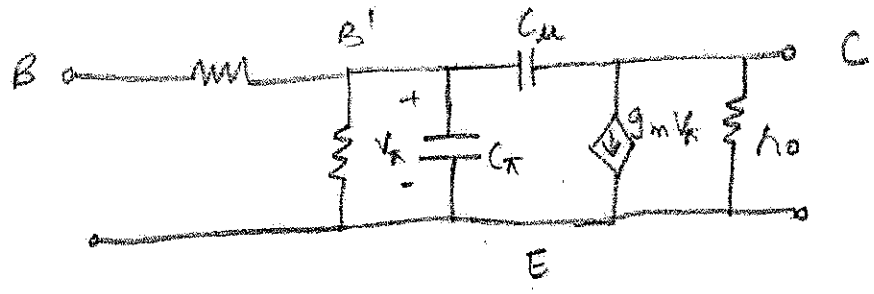
$= 3.92\ V/V$

d) If y is grounded, then the ckt becomes a source follower config

Eq 4.103 $A_{vo} = \frac{r_o}{r_o + \frac{1}{g_m}} = \frac{150}{150 + \frac{1}{0.49}} = 0.986\ V/V$

$R_{out} = \frac{1}{g_m} \| r_o = \frac{1}{0.49} \| 150 = 2.013\ K\Omega$.

Q4)



$$g_m = \frac{I_C}{V_T} = \frac{0.75mA}{25mV} = 30\ mA/V$$

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{30\times10^{-3}} = 6.67\ K\Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{75V}{0.75mA} = 100\ K\Omega$$

$$C_\mu = \frac{C_{\mu o}}{\left(1+\frac{V_{CB}}{V_{oc}}\right)^{0.5}} = \frac{45fF}{\left(1+\frac{2.5}{0.6}\right)^{0.5}} = 19.79fF$$

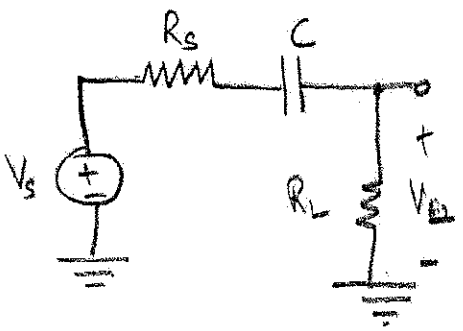
$$C_{je} \simeq 2C_{jeo} = 2\times15 = 30fF$$

$$C_{de} = \tau_F g_m = 25\times10^{-12}\times30\times10^{-3} = 750\ fF$$

$$C_\pi = C_{je} + C_{de} = 30+750 = 0.78\ pF$$

$$f_T = \frac{g_m}{2\pi(C_\pi+C_\mu)} = \frac{30\times10^{-3}}{2\pi(0.78+0.020)\times10^{-12}} = 5.9698\times10^{9}\ Hz.$$

Q1) Using the voltage divider rule.



$$\frac{V_o}{V_s} = \frac{R_L}{R_L + R_s + \frac{1}{sC}}$$

$$= \frac{R_L}{R_L + R_s} \cdot \frac{s}{s + \frac{1}{C(R_L + R_s)}}$$

Which is T.F. of the high pass STC type (see Table 1.2 of Text book)

$$K = \frac{R_L}{R_L + R_s} \quad ; \omega_o = \frac{1}{C(R_L + R_s)}$$

For $f_o \leq 500$ Hz.

$$\frac{1}{2\pi C(R_L + R_s)} \leq 500$$

$$\frac{1}{2\pi C(60+15)\times 10^3} \leq 500$$

$$C \geq \frac{1}{2\pi \times 500 \times (60+15\times 10^3}$$

$$C \geq 4.244 \times 10^{-9} F$$

min value of C = 4.24 nF.

Q2). $V_{CC} = 10V$; $R_1 = 33K\Omega$; $R_2 = 20K\Omega$ $R_E = 1.5K\Omega$ $R_C = 2.7K\Omega$

$\beta = 150$, $V_A = 125V$

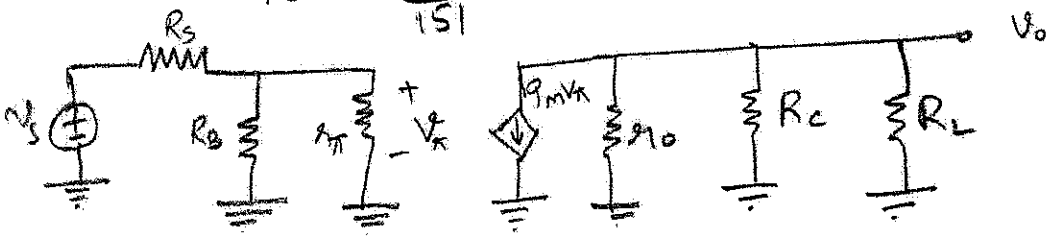
$R_{sig} = 15K\Omega$ $R_L = 1.5K\Omega$.

a) $I_E = \dfrac{V_{BB} - V_{BE}}{R_E + R_B/(\beta+1)}$

where $V_{BB} = V_{CC} \cdot \dfrac{R_2}{R_1+R_2} = 10 \cdot \dfrac{20K}{33K+20K} = 3.77V$

$R_B = R_1 \| R_2 = 33 \| 20 = 12.45K\Omega$

Thus $I_E = \dfrac{3.77 - 0.7}{1.5K + \frac{12.45K}{151}} = 1.94mA$.



$g_m = \dfrac{I_C}{V_T} = \dfrac{\alpha I_E}{V_T} = \dfrac{0.99 \times 1.94}{0.025} \simeq 76.8 \dfrac{mA}{V}$

$r_\pi = \dfrac{\beta}{g_m} = \dfrac{150}{76.8 \times 10^{-3}} = 1.953K\Omega$

$r_o = \dfrac{V_A}{I_C} = \dfrac{125}{0.99 \times 1.94 \times 10^{-3}} = 65.08 \times 10^3 \Omega$

Q3) $V_t = 1.5V$ $\quad K_n' W/L = 0.6 mA/V^2$ $\quad V_A = 30V$

a) $I_D = 0.2 \times 10^{-3} = \frac{1}{2} \times 0.6 \times 10^{-3} \times V_{ov}^2 \Rightarrow V_{ov} = 0.816V$ ∴

$V_{GS} = 1.5 + 0.816 = 2.316V$

$V_G = 0 \Rightarrow V_S = -2.316V$

$R_S = \frac{-2.316 - (-5)}{0.2} = 13.42K\Omega$

$V_{DS} = 5 - R_D$

Largest possible R_D is achieved for $V_{DS\,min}$

$V_{DS} \geq V_{GS} - V_t \Rightarrow V_{DS\,min} - V_{ov} \Rightarrow V_{DS} - 1 = V_{ov}$

$\Rightarrow V_{DS} = 1.5 + 0.816 = 2.316\,V \Rightarrow R_D = \frac{5 - 2.316}{0.2} = 13.42K\Omega$

$R_G = 10M\Omega$

b) $g_m = \frac{2I_D}{V_{ov}} = \frac{2 \times 0.2}{0.816} = 0.49\ mA/V$; $r_o = \frac{V_A}{I_D} = \frac{30}{0.2} = 150K\Omega$

c) If z is grounded then the ckt becomes a common-source config.

The voltage gain according to Eq 4.82.

$G_v = \frac{-R_G}{R_G + R_{sig}} g_m (r_o \| R_D \| R_L) = \frac{9^M}{9^M + 0.8^M} \times 0.49 \times 10^{-3} (150^K \| 1342^K \| 30^K)$

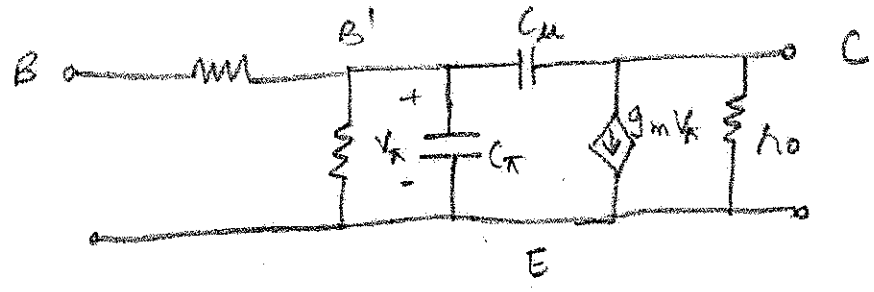
$= 3.92\ V/V$

d) If y is grounded, then the ckt becomes a source follower config

Eq 4.103 $A_{vo} = \frac{r_o}{r_o + \frac{1}{g_m}} = \frac{150}{150 + \frac{1}{0.49}} = 0.986\ V/V$

$R_{out} = \frac{1}{g_m} \| r_o = \frac{1}{0.49} \| 150 = 2.013\ K\Omega$.

94)



$$g_m = \frac{I_C}{V_T} = \frac{0.75mA}{25mV} = 30\ mA/V$$

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{30\times10^{-3}} = 6.67\ K\Omega$$

$$r_o = \frac{V_A}{I_C} = \frac{75V}{0.75mA} = 100K\Omega$$

$$C_\mu = \frac{C_{\mu o}}{\left(1+\frac{V_{CB}}{V_{oc}}\right)^{0.5}} = \frac{45fF}{\left(1+\frac{2.5}{0.6}\right)^{0.5}} = 19.79fF$$

$$C_{je} \simeq 2C_{jeo} = 2\times15 = 30fF$$

$$C_{de} = \tau_F g_m = 25\times10^{-12}\times30\times10^{-3} = 750\ fF$$

$$C_\pi = C_{je} + C_{de} = 30+750 = 0.78\ pF$$

$$f_T = \frac{g_m}{2\pi(C_\pi+C_\mu)} = \frac{30\times10^{-3}}{2\pi(0.78+0.020)\times10^{-12}} = 5.9698\times10^9\ Hz.$$

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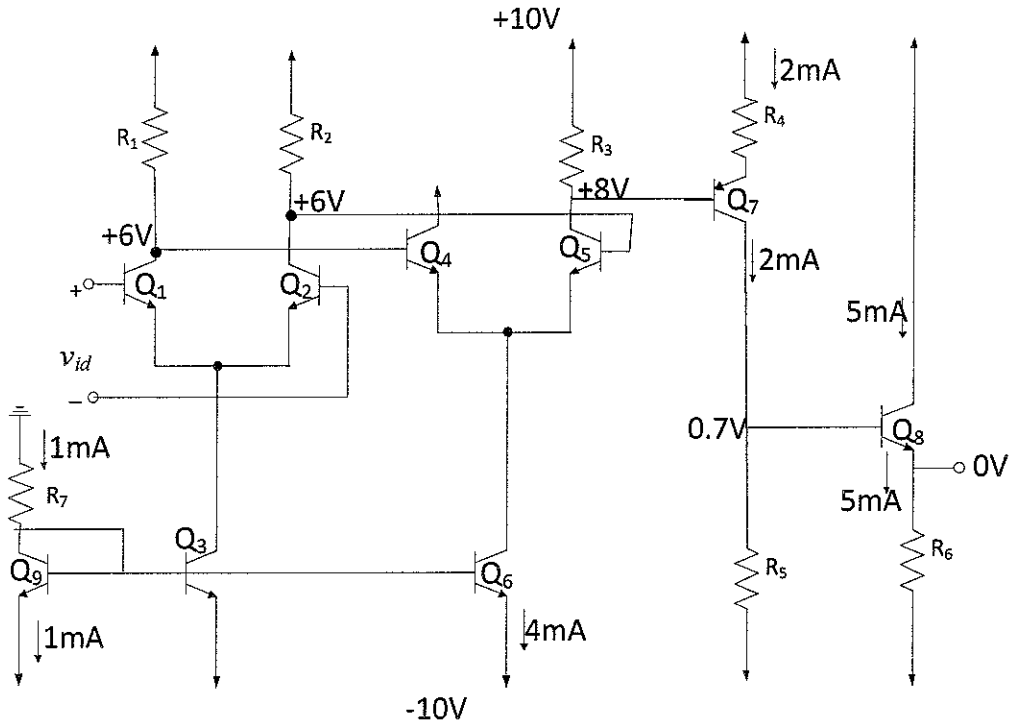
SECOND SEMESTER 2012-2013

Course No: **EEE F244 ECE F244 INSTR F244**	Course Name: **MICROELECTRONIC CIRCUITS**
Evaluation component: **TEST-2 (OPEN BOOK)**	Date & Time: **12-05-2013, SUNDAY, 10:15AM TO 11:20 AM**
Weightage : **20%**	Max marks :**40**
Duration: **50 Minutes** **ANSWER PART A & PART B IN SEPARATE ANSWER BOOK**	Note : ***Answer all the question, assume any missing data suitably***

PART A

Q.1 An overdrive voltage for an NMOS differential amplifier is 0.4V and has a W/L ration of 60, $\mu_n C_{ox}=200\mu A/V^2$, $V_A=10V$ and $R_D=5k\Omega$, Find bias current (I), Transconductance (g_m), output resistance (r_o) and differential gain (A_d). 2.5x2+2x2=9M

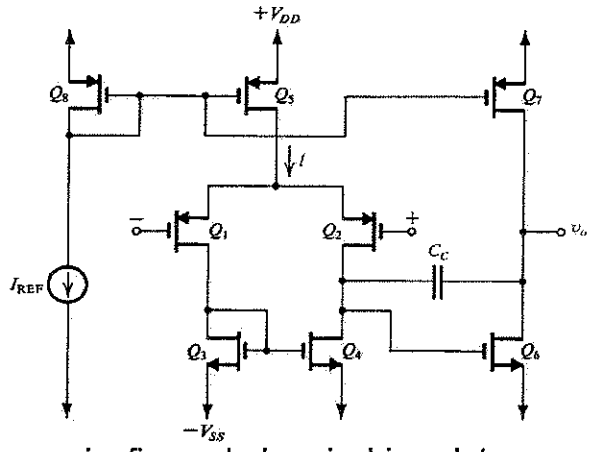
Q.2 Find the values of resistance R_1 to R_7 for the following BJT op-amp circuit shown below 1.5x6+2=11M



PART B

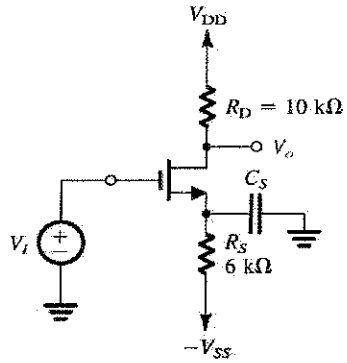
Q.1 The basic 2-stage CMOS OP-AMP, shown in figure below, is fabricated in a process for which $V'_{An}=|V'_{Ap}|<15V/\mu m$. If all the devices are of 1.25μm long; $V_{OV1}=0.3V$; and $V_{OV6}=0.6V$ Find: 2+2+4=8M

i. both individual stage gains and the overall gain.
ii. the OPAMP output resistance obtained when the second stage is biased at 0.6mA
iii. the value of C_C that results in unity-gain frequency, $f_t=120MHz$ assuming: (i)a 250Ω resistance is included in series with Cc and (ii)trans-conductance of 1st and 2nd stages, respectively are: 1.5mA/V and 2.5mA/V.



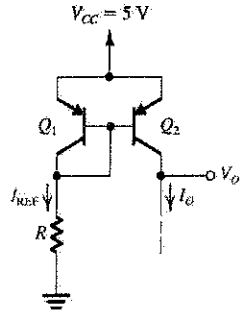
Q.2 The amplifier shown in figure below is biased to operate at I_D=2mA; and g_m=2mA/V. Neglecting r_o, find 2+3+3=8M

a) the mid-band gain and
b) the value of C_S that places f_L at 20Hz.
c) the amplifier's f_H, assuming an R_L=10KΩ is connected at the output. Assume "reasonable/most appropriate" values for the MOSFET parameters including internal capacitances by explicitly indicating needed values assumed.



Q.3 The current source circuit shown in Fig. below utilizes a pair of matched pnp transistors having $I_S=10^{-15}$ A, β=75 and $|V_A|$=45V. It is required to design the circuit to provide an output current I_O=1.5mA at V_O=3V. 2+1+1=4M

i. What values of I_{REF} and R are needed?
ii. What is the maximum allowed value of V_O while the current source continues to operate properly?
iii. What change occurs in I_O corresponding to V_O changing from the maximum positive value of -5V?



PART-A

Q1 Given $V_{OV} = 0.4V$; $\frac{W}{L} = 60$; $\mu_n C_{ox} = 200\mu A/V^2$

$R_D = 5k\Omega$; $V_A = 10V$

Bias current

$$V_{OV} = \sqrt{\frac{I}{k_n'\left(\frac{W}{L}\right)}} \; ; \; 0.4V = \sqrt{\frac{I}{k_n'(60)}}$$

$$0.4V = \sqrt{\frac{I}{200\mu A/V^2 \times 60}} \; ; \; 0.16 = \frac{I}{200\mu A \times 60}$$

$$I = 0.16 \times 12 \times 10^{-3} = 1.92mA \simeq \underline{2mA} \quad \text{——— 2.5}$$

output resistance

$$g_m = \frac{I}{V_{OV}} \; ; \; r_o = \frac{V_A}{I/2} = \frac{10}{1mA} = \underline{10k\Omega} \quad \text{——— 2}$$

Transconductance

$$g_m = \frac{2mA}{0.4V} = \underline{5mA/V} \quad \text{——— 2}$$

Differential Gain

$$A_d = g_m\left(R_D \| r_o\right) = 5mA/V \left(\frac{5k\Omega \times 10k\Omega}{5k\Omega + 10k\Omega}\right)$$

$$= \frac{5 \times 50}{15} = \underline{16.66}$$

$$A_d = 20\log_{10}(16.66) = \underline{24.43dB} \quad \text{——— 2.5}$$

Q2 From the circuit diagram, the current through collector of Q_3 is 1 mA, the currents through Resistor R_1 and R_2 is 0.5mA.

at Q_1, (from KVL)

$$-10 + R_1 \times 0.5\text{mA} + 6 = 0$$

$$0.5\text{mA} \times R_1 = 4$$

$$R_1 = \frac{4}{0.5\text{mA}} = \underline{8\text{k}\Omega} \quad \text{——— 1.5M}$$

In Similar way the value of the resistance $R_2 = \underline{8\text{k}\Omega}$ ——— 1.5M

Since the current through Q_6 is 4mA, current through R_3 is 2mA.

at Q_5 (from KVL)

$$-10 + 2\text{mA} \times R_3 + 8 = 0$$

$$2\text{mA} \times R_3 = 2$$

$$R_3 = \frac{2}{2\text{mA}} = \underline{1\text{k}\Omega} \quad \text{——— 1.5M}$$

Voltage at the emitter of Q_7 is 8.7V

at Q_7, we have (from KVL)

$$-10 + 2\text{mA}\, R_4 + 8.7 = 0$$

$$R_4 = \frac{1.3}{2\text{m}} = 0.65\text{k}\Omega = \underline{650\,\Omega} \quad \text{——— 2M}$$

Voltage at the base of Q_8 is 0.7
at the base of Q_8 from KVL, we get

$$-0.7 + 1\,mA \times R_5 - 10 = 0$$

$$R_5 = 10.7\ k\Omega \quad //$$ ——— 1.5M

Similarly at Q_8, from KVL, we get

$$-0 + 5\,mA \times R_6 - 10 = 0$$

$$R_6 = \frac{10}{5\,mA} = 2\ k\Omega$$ ——— 1.5M

at Q_9, applying KVL, we get

$$1\,mA \times R_7 + 0.7 - 10 = 0$$

$$R_7 = \frac{9.3}{1\,mA} = 9.3\ k\Omega$$ ——— 1.5M

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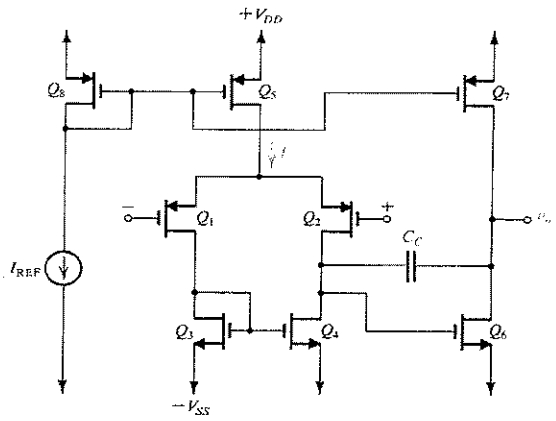
SECOND SEMESTER 2012-2013

Course No: **EEE F244 ECE F244 INSTR F244**	Course Name: **MICROELECTRONIC CIRCUITS**
Evaluation component: **TEST-2 (OPEN BOOK)**	Date & Time: **12-05-2013, SUNDAY, 10:15AM TO 11:20 AM**

PART B

Solution for Q. No.1:

The basic 2-stage CMOS OP-AMP The basic 2-stage CMOS OP-AMP, shown in figure below, is fabricated in a process for which $V'_{An} = |V'_{Ap}| < 15$ V/μm. If all the devices are of 1.25μm long; V_{OV1}=0.3V; and V_{OV6}=0.6V



Find:

a) both individual stage gains and the overall gain can be computed employing the given data and using the relations in Eqn Nos.9.11, 9.12 and 9.13 of the prescribed Text Book:

$A_1=-g_{m1}(r_{o2}||r_{o4}) = -2/V_{A1}/\{(1/|V_{A2}|) + (1/|V_{A4}|)\}$;

$A_2=-g_{m6}(r_{o6}||r_{o7}) = -2/V_{A1}/\{(1/|V_{A6}|) + (1/|V_{A7}|)\}$

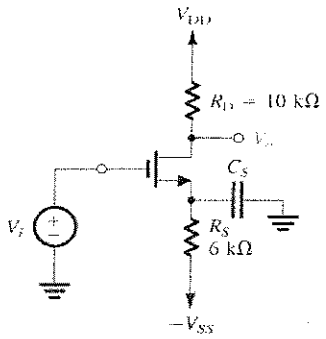
and overall gain is A_1*A_2.

b) when the second stage is biased at i.e., I_{D6}=0.6mA, the OPAMP output resistance can be obtained using the relation as in Eqn. No.9.16 of the prescribed text book; which is: $r_{o6}=|V_{A6}|/I_{D6}$.

c) Using the relations in Eqn. 9.16; 9.27 and 9.37 of the prescribed Text book, the value of C_C that results in unity-gain frequency, f_t=120MHz assuming: (i)a 250Ω resistance is included in series with Cc and (ii)trans-conductance of 1st and 2nd stages, respectively are: 1.5mA/V and 2.5mA/V;

Solution for Q. No.2:

The amplifier shown in figure below is biased to operate at I_D=2mA; and g_m=2mA/V. Neglecting r_o,



a) the mid-band gain and

Given that: I_D=2 mA; g_m=2mA/V;

Prescribed Book page No.311 Eqn. No.4.89 is:

$$A_M = -\frac{g_m R_D}{1+g_m R_S} = -\frac{2x10}{1+2x6} = 1.5384\ V/V$$

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Course No: **EEE F244 ECE F244 INSTR F244**	Course Name: **MICROELECTRONIC CIRCUITS**
Evaluation component: **TEST-2 (OPEN BOOK)**	Date & Time: **12-05-2013, SUNDAY, 10:15AM TO 11:20 AM**

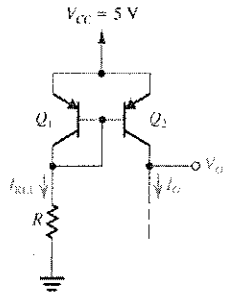
b) the value of C_S that places f_L at 20Hz.

Assuming that C_{c1} or C_{c2} are infinity and thus the low frequency is response is only due to R_S and C_S: $f_L = \frac{1}{2\pi(\frac{1}{g_m}||R_S)C_S} = 20Hz$

Here the R contributing to the high frequency pole is: $R_{eq} = R_S||R_{out}$, in which $R_{out}=r_0||(1/g_m)$ following the Eqn.4.105 on page 318 and/or using Fig.4.51 of prescribed text. Student can assume $r_0=\infty$ i.e., an ideal MOS, Cs can be found using above eqn.

c) Assuming an R_L=10KΩ is connected at the output and the by using the values of MOSFET parameters of the prescribed text Example No. 4.12 on page 331-332, the amplifier's f_H,can be determined using the expression for the same (as on page 332 of prescribed text: $f_H = \frac{1}{2\pi(R_{sig}||R_G)C_{in}} = \frac{1}{2\pi(C_{gs}+[1+g_m\{R_D||R_L||r_0\}C_{gd}])R_{sig}||R_G}$

Solution for Q. No.3



Matched pnp transistors of the circuit shown in Fig. has: $I_S=10^{-15}$ A, β=75 and $|V_A|$=45V. To design the circuit such that its output current I_0=1.5mA at V_0=3V:

a) I_{REF} can be computed using $I_0 = \frac{I_{REF}}{1+\frac{2}{\beta}}$; the needed can be computed from the relations: $R=\frac{V_C}{I_{REF}} = \frac{V_{CC}-V_{C/B}}{I_{REF}}$ in which: $V_B = V_{BE} = V_T \ln \frac{I_0}{I_S\{1+\frac{V_{CE}}{V_A}\}}$

b) the maximum allowed value of V_O while the current source continues to operate properly

V_{0min} occurs when Q_2 is on the edge of saturation or V_{CC}=0.3V. Therefore, V_{0max} is 5 - V_{CEsat} = 5 - 0.3 = 4.7V.

c) Change that occurs in I_O corresponding to V_O changing from the maximum positive value of $-V_{CC}$(=-5V) can be computed by solving the relationship: $r_0=\frac{V_A}{I_0} = \frac{\Delta v_0}{\Delta I_0} = \frac{v_{0max}-(-V_{CC})}{\Delta I_0}$ compute from it the value of: $\frac{\Delta I_0}{I_0} \times 100$.

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SECOND SEMESTER 2012-2013

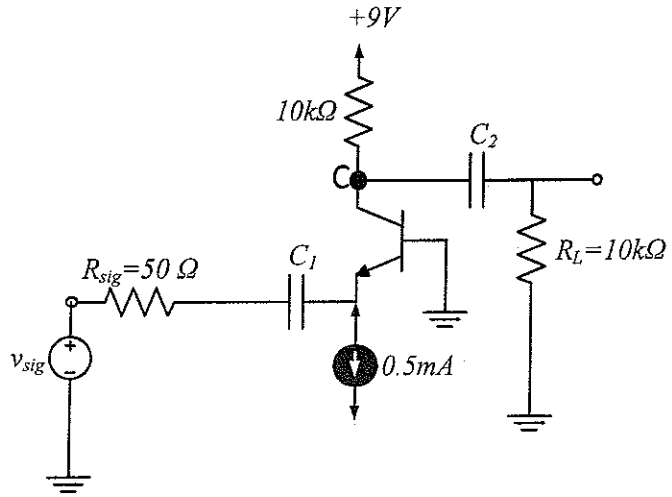
Course No: **EEE F244 ECE F244 INSTR F244**	Course Name: **MICROELECTRONIC CIRCUITS**
Evaluation component: **TEST-1**	Date & Time: **21-03-2013, THURSDAY , 11:15AM TO 12:05 PM**
Weightage : **25%**	Max marks :**50**
Duration: **50 Minutes** **ANSWER PART A & PART B IN SEPARATE ANSWER BOOK**	Note : ***Answer all the question, assume any missing data suitably***

PART A

Q.1 Draw the circuit diagram of the single stage CE BJT amplifier and using its small signal equivalent model derive an expression for the following [1.5+1.5+2x6=15M]

I. Input resistance
II. Output resistance
III. Voltage gain
IV. Open circuit voltage gain
V. Overall voltage gain
VI. Short circuit current gain

Q.2 For the circuit shown below, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT (α=0.99), Your circuit should show the values of all components, including the model parameters. What is the input resistance R_{in} ? Calculate the overall voltage gain? [3+3+2+2=10M]



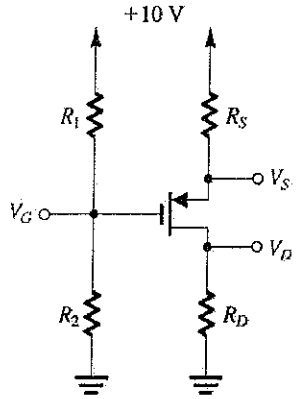
PART B

Q.1 Sketch the complete hybrid-π model (valid at high-frequencies also) of an *npn* transistor. Compute the values of C_π and C_μ. [3+2.5x2=8M]

Assume: the npn transistor is operated at I_C = 0.5 mA and V_{CB} =2 V and has (i)low-frequency value of β (β_0) = 100, (ii)Early Voltage, V_A = 40 V, (iii)Forward base-transit time, τ_F = 25 ps, (iv)Base -Emitter Junction (EBJ) Capacitance at zero voltage, C_{je0} = 15 fF, (v)Collector Base Junction (CBJ) Capacitance at zero voltage, $C_{\mu 0}$ =25 fF, (vi)Collector-Base Junction (CBJ) built-in Voltage, V_{0c} = 0.7 V, (vii)grading coefficient, m_{CBJ} = 0.5, and (viii)Base spreading resistance, r_x = 110Ω.

Q.2 By employing a 10A current in the voltage divider of the circuit of Fig. shown, in order to operate the MOS transistor in saturation with V_D biased 1 V from the edge of the triode region, with I_D=*I mA* and V_D = 3 V, find the values of all the resistors and voltages indicated in the figure. [1x4+1x3=7M]

Assume: $|V_t| = 1\ V$ *and* $k'_pW/L = 0.6\ mA/V^2$.



Q.3 The source follower of Circuit shown in Fig. employs a MOSFET biased to have g_m = 5 mA/V and r_0=20 kΩ. [1+3+2x3=10M]

I. Draw the small signal equivalent model

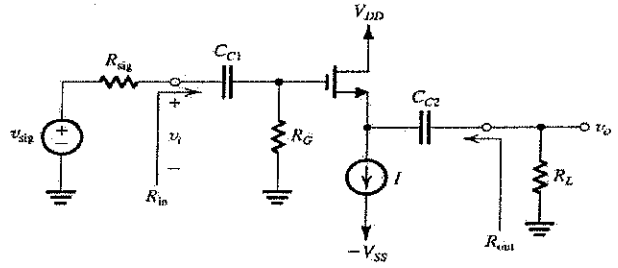
II. Derive the expression for overall voltage gain

III. Find

a. the open circuit voltage gain,A_{v0}

b. the output resistance (R_{out}).

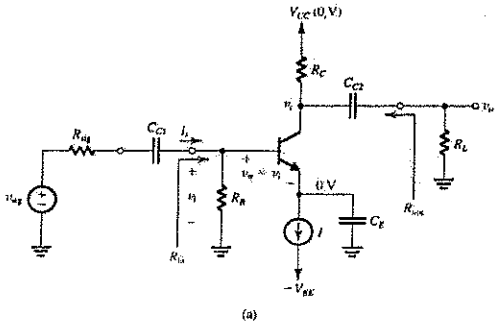
c. the voltage gain if R_L = 1.5 kΩ



(a)

Q1

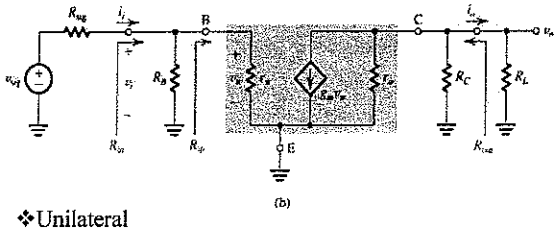
PART-A



(a)

1.5

Let us determine Input resistance , voltage gain and output resistance by replacing the BJT with its hybrid π small signal model.



(b)

- Unilateral
- $R_{in}=R_i$ and $R_{out}=R_o$

1.5

At the amplifier input we have

$$R_{in} \equiv \frac{v_i}{i_i} = R_B \| R_{ib}$$

where R_{ib} is the input resistance looking into the base. Since the emitter is grounded,

$$R_{ib} = r_\pi$$

Normally, we select $R_B \gg r_\pi$, with the result that

$$R_{in} \cong r_\pi$$

(2)

The fraction of source signal v_{sig} that appears across the input terminals of the amplifier proper can be found from

$$v_i = v_{sig}\frac{R_{in}}{R_{in}+R_{sig}} = v_{sig}\frac{(R_B \| r_\pi)}{(R_B \| r_\pi)+R_{sig}}$$

which for $R_B \gg r_\pi$ becomes

$$v_i \cong v_{sig}\frac{r_\pi}{r_\pi + R_{sig}}$$

we note that $v_\pi = v_i$

At the output of the amplifier we have

$$v_o = -g_m v_\pi (r_o \| R_C \| R_L)$$

Replacing v_π by v_i we can write for the voltage gain of the amplifier proper; that is, the voltage gain from base to collector,

$$A_v = -g_m(r_o \| R_C \| R_L)$$

(2)

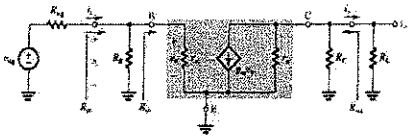
The open-circuit voltage gain A_{vo} can be obtained by setting $R_L = \infty$

$$A_{vo} = -g_m(r_o \| R_C)$$

since typically $r_o \gg R_C$, resulting in

$$A_{vo} \cong -g_m R_C$$

(2)



The output resistance R_{out} can be found from the equivalent circuit by looking back into the output terminal while short-circuiting the source v_{sig}.

Since this will result in $v_\pi = 0$, we see that

$$R_{out} = R_C \| r_o$$

(2)

PART A

$r_o \gg R_C$

$R_{out} \cong R_C$

unilateral amplifier $R_o = R_{out}$,

voltage gain A_v corresponding to any particular R_L,

$$A_v = A_{vo}\frac{R_L}{R_L + R_o}$$

The overall voltage gain from source to load, G_v, can be obtained by multiplying (v_i/v_{sig}) by A_v

$$G_v = \frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{sig}} g_m (r_o \parallel R_C \parallel R_L)$$

For the case $R_B \gg r_\pi$, this expression simplifies to

$$G_v \cong -\frac{\beta(R_C \parallel R_L \parallel r_o)}{r_\pi + R_{sig}} \quad (2)$$

if $R_{sig} \gg r_\pi$, the overall gain will be highly dependent on β.

This is not a desirable property since β varies considerably between units of the same transistor type.

if $R_{sig} \ll r_\pi$, we see that the expression for the overall voltage gain reduces to

$G_v \cong -g_m(R_C \parallel R_L \parallel r_o)$

which is the gain A_v;

in other words, when R_{sig} is small, the overall voltage gain is almost equal to the gain of the CE circuit proper, which is independent of β.

short-circuit current gain, A_{is}

This can be easily done by referring to the amplifier equivalent circuit

R_L is short circuited, the current through it will be equal to $-g_m v_\pi$,

$i_{os} = -g_m v_\pi$

Since v_π is related to i_i by

$v_\pi = v_i = i_i R_{in}$

the short-circuit current gain can be found as

$$A_{is} \equiv \frac{i_{os}}{i_i} = -g_m R_{in} \quad (2)$$

$R_{in} = R_B \parallel r_\pi \qquad R_B \gg r_\pi$,

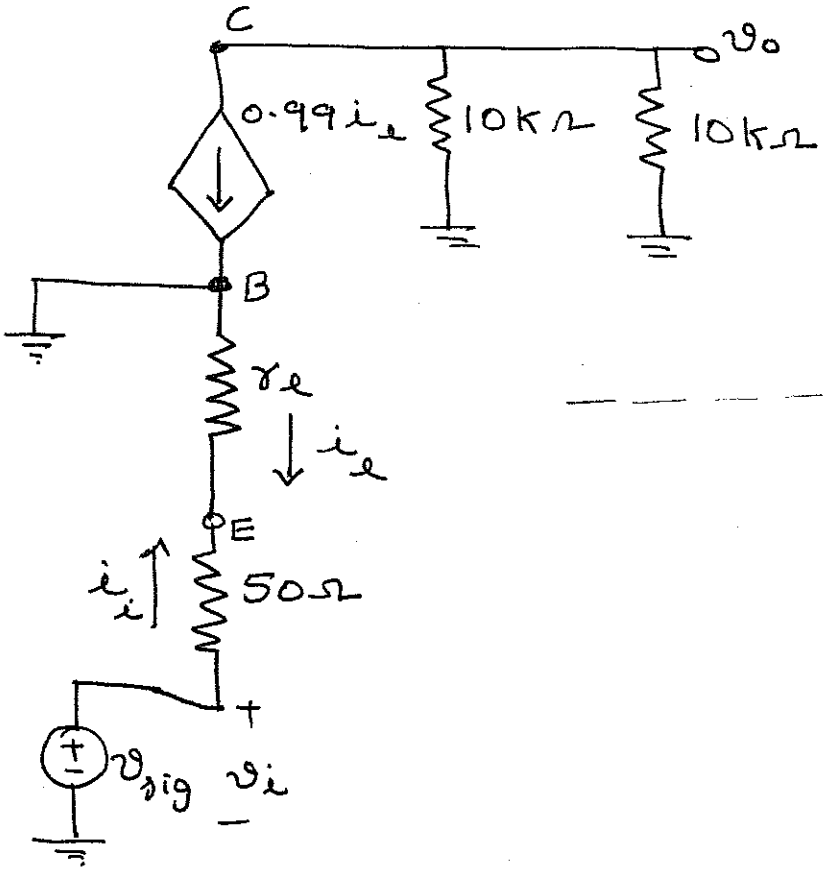
$|A_{is}|$ reduces to β, by definition,

the short-circuit current gain of the common-emitter configuration.

PART-A

Q2: Given $\alpha = 0.99$

Small signal equivalent circuit using - T model is



3M

$$r_e = \frac{V_T}{I_E} = \frac{25mV}{0.5mA} = \underline{\underline{50\Omega}}$$ ---------- 3M

$$R_{in} = r_e = \underline{\underline{50\Omega}}$$ ---------- 1M

$$i_e = \frac{-v_{sig}}{R_s + R_e} = \frac{-v_{sig}}{100}$$ ---------- 1M

$$v_o = -0.99 i_e \times \frac{10K\Omega \times 10K\Omega}{10+10} = \underline{\underline{5K\Omega}}$$ ---------- 1M

Substituting i_e, we get

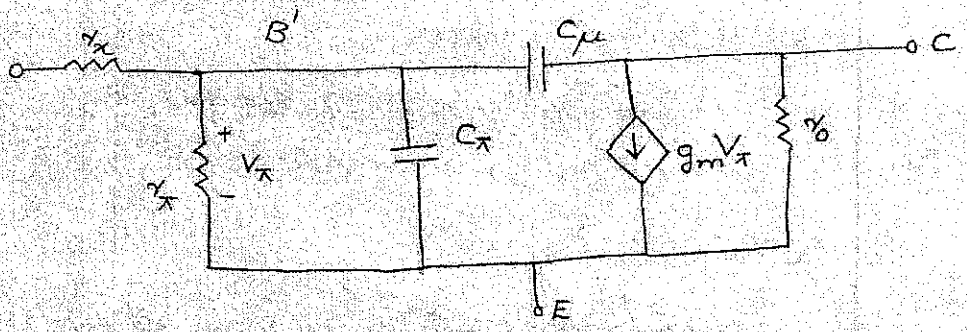
$$\frac{v_o}{v_{sig}} = \frac{+0.99 \times 5K\Omega}{100} = \underline{\underline{49.5}}$$ {overall voltage gain} ---------- 1M

TEST - 1

Microelectronic Circuits

Answer key for PART B

Q.1 High frequency hybrid-π model



Emitter-base capacitance, $C_\pi = C_{de} + C_{je}$

$$C_{de} = \tau_F g_m = \tau_F \frac{I_C}{V_T}$$

Given, $\tau_F = 25ps$, $I_C = 0.5mA$ and $V_T = 25mV$ (at room temp)

$$C_{de} = \frac{25 \times 10^{-12} \times 0.5 \times 10^{-3}}{25 \times 10^{-3}} = \underline{0.5\,pF}, \quad C_{je} = 2C_{je0} = \underline{30fF}$$

$$\therefore C_\pi = 0.5pF + 0.003pF = \underline{0.503pF}$$

$$C_\mu = \frac{C_{\mu 0}}{\left[1 + \frac{V_{CB}}{V_{0c}}\right]^m}$$

Given $C_{\mu 0} = 25fF$, $V_{CB} = 2V$, $V_{0c} = 0.7V$, $m = 0.5$

$$\therefore C_\mu = \frac{25 \times 10^{-15}}{\left[1 + \frac{2}{0.7}\right]^{0.5}}$$

Q.2. Given $I_D = 1\,mA$, $V_D = 3V$

$$\therefore R_D = \frac{V_D}{I_D} = 3k\Omega$$

10A current in voltage divider,

$$R_1 + R_2 = \frac{10V}{10A} = 1\Omega$$

To operate MOS transistor in saturation, biasing V_D 1V from the edge of triode region,

$$V_{DS} = V_{GS} - V_t - 1 \quad (\text{Given } V_D = 3V)$$

Given $|V_t| = 1V$ & $k_p'(W/L) = 0.6 mA/V^2$,

$$I_D = \frac{1}{2} k_p'\left(\frac{W}{L}\right)(V_{GS}+1)^2$$

$$1 = \frac{0.5}{2} \times 0.6 \times (V_{GS}+1)^2 = \frac{1}{2} \times 0.6 \times (V_{GS}+1)^2$$

$$\therefore V_{GS} = -3V$$

$$\therefore V_{DS} = V_{GS} - V_t - 1 = -3 + 1 - 1 = -3V$$

$V_D = 3V$, $\therefore V_S = 6V$, $V_G = 3V$

$$R_S = \frac{V_{DD} - V_S}{I_D} = \frac{10 - 6}{1 \times 10^{-3}} = 4k\Omega$$

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

$$3 = 10 \times \frac{R_2}{R_1 + R_2}$$

$$\frac{R_2}{R_1 + R_2} = \frac{3}{10} \quad (R_1 + R_2 = 1)$$

$$R_2 = 0.3\Omega \qquad R_1 = 0.7\Omega$$

$$I_D = \frac{1}{2} \times 0.6 \times (V_{GS}+1)^2$$

$$(V_{GS}+1)^2 = 2/0.6 = 3.33$$

$$V_{GS} + 1 = 1.82$$

$$V_{GS} = -0.82V$$

$$\therefore V_{DS} = V_{GS} - V_t - 1 = -0.82 + 1 - 1 = -0.82V$$

$V_D = 3V$ $\therefore V_S = 3.82V$,

$\therefore V_G = 3V$.

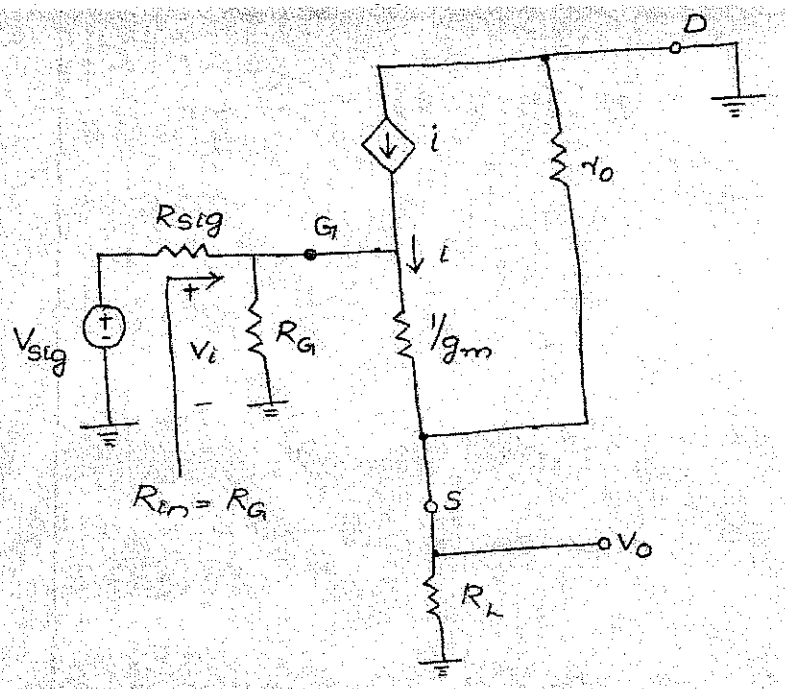
$$R_S = \frac{V_{DD} - V_S}{I_D} = \frac{10 - 3.82}{1 \times 10^{-3}}$$

$$= 6.18\,k\Omega$$

~~$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$~~

Q 3.

I.



II. Input resistance, $R_{in} = R_G$

Thus $$V_i = V_{sig} \cdot \frac{R_{in}}{R_{in} + R_{sig}} = V_{sig} \cdot \frac{R_G}{R_G + R_{sig}} \quad — (1)$$

$R_G >> R_{sig}$, $V_i \cong V_{sig}$

Output voltage, $$V_o = V_i \frac{R_L // r_o}{(R_L // r_o) + 1/g_m} \quad — (2)$$

Voltage gain, $$A_V = \frac{R_L // r_o}{(R_L // r_o) + 1/g_m} \quad — (3)$$

Open-circuit voltage gain, $$A_{Vo} = \frac{r_o}{r_o + 1/g_m} \quad — (4)$$

For $r_o >> R_L$, $$A_V \cong \frac{R_L}{R_L + 1/g_m} \quad — (5)$$

Overall voltage gain, G_V can be found by combining (1) and (3)

$$\therefore G_V = \frac{R_G}{R_G + R_{sig}} \cdot \frac{R_L // r_o}{(R_L // r_o) + 1/g_m}$$

III

a) Open circuit voltage gain, $A_{V_0} = \frac{r_o}{r_o + 1/g_m}$

Given, $r_o = 20k\Omega$, $g_m = 5$

$$\therefore A_{V_0} = \frac{20 \times 10^3}{20 \times 10^3 + 1/5} \cong 1$$

b) Output resistance, $R_{out} = 1/g_m \,||\, r_o$

$$= 1/5 \,||\, 20 \times 10^3 = 0.1999$$

$$\cong \underline{0.2\Omega}$$

c) Voltage gain, $A_V = \frac{R_L || r_o}{(R_L || r_o) + 1/g_m}$ (Given $R_L = 1.5k\Omega$)

$$= \underline{0.8746}$$

BIRLA INSTITIUE OF TECHNOLOGY AND SCIENCE PILANI, DUBAI

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Evaluation component: QUIZ 1	Date & Time: 07-03-2013 , 11:15AM TO 11:35 AM
Weightage : 8%	Max marks :16
Duration: 20 Minutes	Note : *Answer all the question, assume any missing data suitably*

SET A

Q.1 Match the expressions given, below, with the terms by indicating matching terms: A to H against each expression. **0.25x8 =2M**

A (Terms)		B (Expressions)		
A.	Voltage Gain	i.	P_L/P_i	[C]
B.	Current Gain	ii.	$P_L \times 100/P_{dc}$	[F]
C.	Power Gain	iii.	$P_{dc}+P_I-P_L$	[H]
D.	Open Circuit Voltage Gain	iv.	v_o/v_i	[A]
E.	Open Circuit Transresistance	v.	i_o/i_i	[B]
F.	Efficiency	vi.	$\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$	[G]
G.	Amplifier Saturation	vii.	$A_{is}\left\{\frac{R_o}{R_i}\right\}$	[D]
H.	$P_{dissipated}$	viii.	$A_{vo}R_i$	[E]

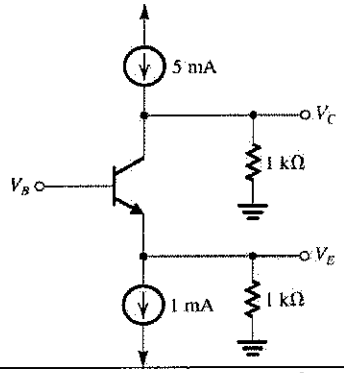
Q.2 Lower frequency part of an Amplifier's frequency response is typically that of **High pass** Single Time Constant Circuit while its high frequency part is typically that of **Low pass** Single Time Constant Circuit. **0.5x2= 1M**

Q.3 For a BJT to function like an Amplifier, its Emitter Base Junction should be **Forward** biased while its Collector Base Junction should be **Reverse** biased. **0.5x2= 1M**

Q.4 A Common-emitter amplifier operated with V_{CC}=+10V is biased at V_{CE}=+1.0V. **0.5+1+0.5 = 2M**

a. Its voltage gain is: **-360**;
b. Its max. allowed output negative swing without the transistor entering saturation is: **0.7V** ;
c. The corresponding maximum input signal permitted is: **1.94mV**

Q.5 For the transistor circuit shown in Fig. below, assume α≡1 and v_{BE}=0.5V. Find V_E and V_C for V_B=0V? **1+1 = 2M**



Ans:

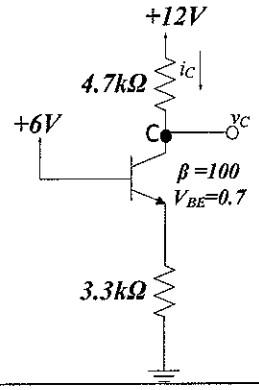
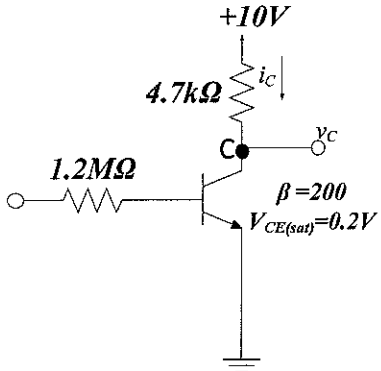
V_E= **-0.5V**

V_c= **4.3V**

Q.6 Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in: **1M**

A. Only the temperature
B. Only the β of the transistor
C. Both temperature and β
D. None of the above

Ans: **C**

Q.7	In a CE transistor amplifier, if collector–emitter voltage increases the instantaneous operating point: A. Moves up the load line B. Moves down the load line C. Moves at right angle to the load line D. Remains stationary Ans: **A**	1M
Q.8	For the following BJT circuit, what is the collector current and voltage at the collector point?  Ans: Collector Current= **1.6mA** Voltage at the collector= **4.48V**	1+1=2M
Q.9	Refer to the following figure. Determine the minimum value of I_B that will produce saturation.  Ans: **10.425µA**	2M
Q.10	For the common-emitter amplifier ac equivalent circuit, all capacitors are A. effectively shorts. B. effectively open circuits. C. not connected to ground. D. connected to ground. Ans: **A**	1M
Q.11	A BJT having β=200, is biased at a dc collector current of 1mA. Find the value of small signal input resistance between base and emitter (r_π) Ans: **5kΩ**	1M

SPACE FOR ROUGH WORK:

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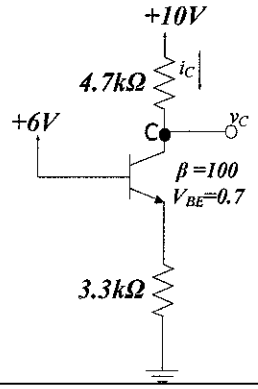
SET B

Q.1 Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in: **1M**

A. Both temperature and β
B. Only the β of the transistor
C. Only the temperature
D. None of the above

Ans: **A**

Q.2 For the following BJT circuit, what is the collector current and voltage at the collector point? **1+1=2M**



Ans:

Collector Current= **1.6mA**

Voltage at the collector=**2.48V**

Q.3 For the common-emitter amplifier ac equivalent circuit, all capacitors are **1M**

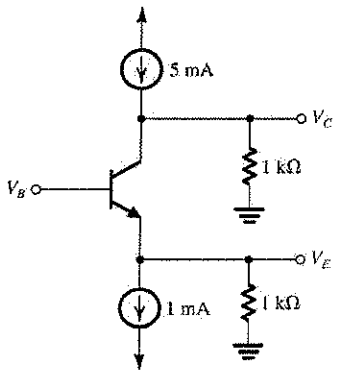
A. not connected to ground
B. effectively open circuits.
C. effectively shorts
D. connected to ground.

Ans: **C**

Q.4 A BJT having β=100, is biased at a dc collector current of 1mA. Find the value of small signal input resistance between base and emitter (r_π) **1M**

Ans: **2.5kΩ**

Q.5 For the transistor circuit shown in Fig. below, assume α≡1 and v_{BE}=0.7V. Find V_E and V_C for V_B=0V? **1+1 = 2M**



Ans:

V_E= **-0.7V**

V_C= **4.7 V**

Q.6	Match the expressions given, below, with the terms by indicating matching terms: A to H against each expression. **A (Terms)** / **B (Expressions)** A. Voltage Gain — i. P_L/P_I — [C] B. Current Gain — ii. $P_L \times 100/P_{dc}$ — [F] C. Power Gain — iii. $P_{dc}+P_I-P_L$ — [H] D. Open Circuit Voltage Gain — iv. v_o/v_i — [A] E. Open Circuit Transresistance — v. i_o/i_i — [B] F. Efficiency — vi. $\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$ — [G] G. Amplifier Saturation — vii. $A_{is}\left\{\frac{R_o}{R_i}\right\}$ — [D] H. $P_{dissipated}$ — viii. $A_{vo}R_i$ — [E]	0.25x8 =2M
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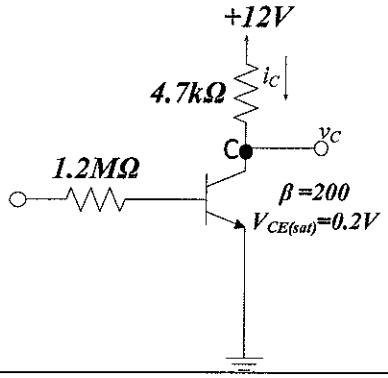
Q.8	Refer to the following figure. Determine the minimum value of I_B that will produce saturation.  Ans: **12.55µA**	2M
Q.9	For a BJT to function like an Amplifier, its Emitter Base Junction should not be **Reverse** biased while its Collector Base Junction should be **Reverse** biased.	0.5x2= 1M
Q.10	Lower frequency part of an Amplifier's frequency response is typically that of **High pass** Single Time Constant Circuit while its high frequency part is typically that of **Low pass** Single Time Constant Circuit.	0.5x2= 1M
Q.11	In a CE transistor amplifier, if collector–emitter voltage increases the instantaneous operating point: A. Remains stationary B. Moves at right angle to the load line C. Moves up the load line D. Moves down the load line Ans: **C**	1M

SPACE FOR ROUGH WORK

Student ID:	Student Name:

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B.	Current Gain	ii.	$P_L \times 100/P_{dc}$	[ ]
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E.	Open Circuit Transresistance	v.	i_o/i_i	[ ]
F.	Efficiency	vi.	$\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$	[ ]
G.	Amplifier Saturation	vii.	$A_{is}\left\{\frac{R_o}{R_i}\right\}$	[ ]
H.	$P_{dissipated}$	viii.	$A_{vo}R_i$	[ ]

Q.2 Lower frequency part of an Amplifier's frequency response is typically that of _____ Single Time Constant Circuit while its high frequency part is typically that of _____ Single Time Constant Circuit. **0.5x2= 1M**

Q.3 For a BJT to function like an Amplifier, its Emitter Base Junction should be _____ biased while its Collector Base Junction should be _____ biased. **0.5x2= 1M**

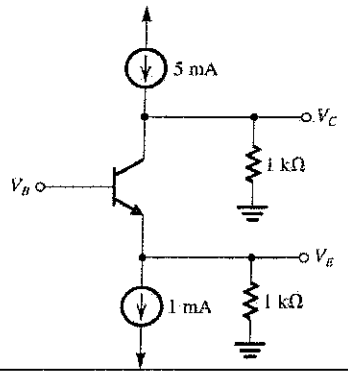
Q.4 A Common-emitter amplifier operated with V_{CC}=+10V is biased at V_{CE}=+1.0V. **0.5+1+0.5 = 2M**

a. Its voltage gain is:_____;

b. Its max. allowed output negative swing without the transistor entering saturation is:_____;

c. The corresponding maximum input signal permitted is:_____

Q.5 For the transistor circuit shown in Fig. below, assume $\alpha \equiv 1$ and v_{BE}=0.5V. Find V_E and V_C for V_B=0V? **1+1 = 2M**



Ans:

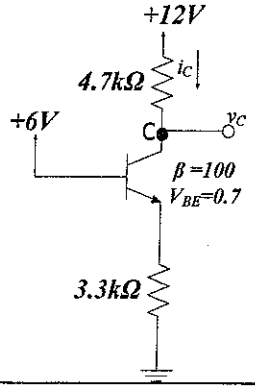
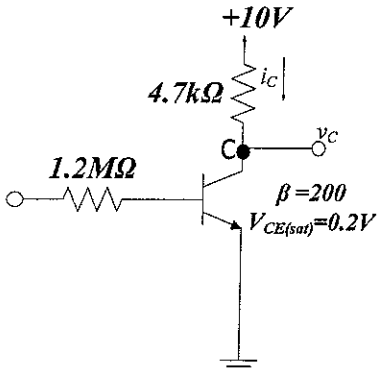
V_E=

V_C=

Q.6 Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in: **1M**

A. Only the temperature
B. Only the β of the transistor
C. Both temperature and β
D. None of the above

Ans:

Q.7	In a CE transistor amplifier, if collector–emitter voltage increases the instantaneous operating point: A. Moves up the load line B. Moves down the load line C. Moves at right angle to the load line D. Remains stationary Ans:	1M
Q.8	For the following BJT circuit, what is the collector current and voltage at the collector point?  Ans: Collector Current= Voltage at the collector=	1+1=2M
Q.9	Refer to the following figure. Determine the minimum value of I_B that will produce saturation.  Ans:	2M
Q.10	For the common-emitter amplifier ac equivalent circuit, all capacitors are A. effectively shorts. B. effectively open circuits. C. not connected to ground. D. connected to ground. Ans:	1M
Q.11	A BJT having β=200, is biased at a dc collector current of 1mA. Find the value of small signal input resistance between base and emitter (r_π) Ans:	1M

SPACE FOR ROUGH WORK:

Student ID:	Student Name:

BIRLA INSTITIUE OF TECHNOLOGY AND SCIENCE PILANI, DUBAI

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

SECOND SEMESTER 2012-2013

Course No: **EEE F244/ ECE F244/ INSTR F244**	Course Title: **MICROELECTRONICS CIRCUITS**
Evaluation component: QUIZ 1	Date & Time: 07-03-2013 , 11:15AM TO 11:35 AM
Weightage : 8%	Max marks :16
Duration: 20 Minutes *Write your answers only in space provided*	Note : *Answer all the question,* *assume any missing data suitably*

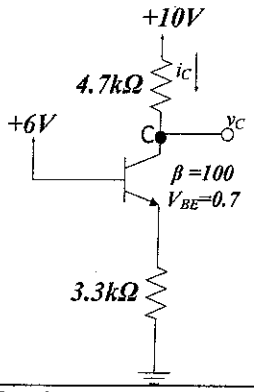
SET B

Q.1 Introducing a resistor in the emitter of a common emitter amplifier stabilizes the dc operating point against variations in: **1M**

A. Both temperature and β
B. Only the β of the transistor
C. Only the temperature
D. None of the above

Ans:

Q.2 For the following BJT circuit, what is the collector current and voltage at the collector point? **1+1=2M**



Ans:

Collector Current=

Voltage at the collector=

Q.3 For the common-emitter amplifier ac equivalent circuit, all capacitors are **1M**

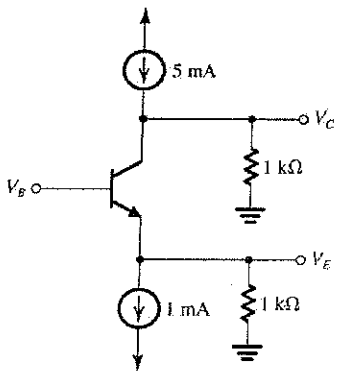
A. not connected to ground
B. effectively open circuits.
C. effectively shorts
D. connected to ground.

Ans:

Q.4 A BJT having β=100, is biased at a dc collector current of 1mA. Find the value of small signal input resistance between base and emitter (r_π) **1M**

Ans:

Q.5 For the transistor circuit shown in Fig. below, assume α≡1 and v_{BE}=0.7V. Find V_E and V_C for V_B=0V? **1+1 = 2M**



Ans:

V_E=

V_C=

Q.6 Match the expressions given, below, with the terms by indicating matching terms: A to H against each expression. **0.25x8 =2M**

A (Terms)	B (Expressions)		
A. Voltage Gain	i.	P_L/P_I	[ ]
B. Current Gain	ii.	$P_L \times 100/P_{dc}$	[ ]
C. Power Gain	iii.	$P_{dc}+P_I-P_L$	[ ]
D. Open Circuit Voltage Gain	iv.	v_o/v_i	[ ]
E. Open Circuit Transresistance	v.	i_o/i_i	[ ]
F. Efficiency	vi.	$\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$	[ ]
G. Amplifier Saturation	vii.	$A_{is}\left\{\frac{R_o}{R_i}\right\}$	[ ]
H. $P_{dissipated}$	viii.	$A_{vo}R_i$	[ ]

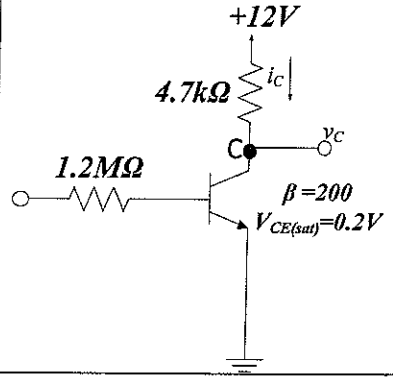
Q.7 A Common-emitter amplifier operated with V_{CC}=+10V is biased at V_{CE}=+1.0V. **0.5+1+0.5 = 2M**

a. Its voltage gain is:_____;

b. Its max. allowed output negative swing without the transistor entering saturation is:_____;

c. The corresponding maximum input signal permitted is:_____

Q.8 Refer to the following figure. Determine the minimum value of I_B that will produce saturation. **2M**



Ans:

Q.9 For a BJT to function like an Amplifier, its Emitter Base Junction should not be _____ biased while its Collector Base Junction should be _____ biased. **0.5x2= 1M**

Q.10 Lower frequency part of an Amplifier's frequency response is typically that of _____ Single Time Constant Circuit while its high frequency part is typically that of _____ Single Time Constant Circuit. **0.5x2= 1M**

Q.11 In a CE transistor amplifier, if collector–emitter voltage increases the instantaneous operating point: **1M**

A. Remains stationary
B. Moves at right angle to the load line
C. Moves up the load line
D. Moves down the load line

Ans:

SPACE FOR ROUGH WORK