# BITS, PILANI – DUBAI CAMPUS

## Knowledge Village, Dubai

Year II - Semester II 2003 - 2004

# COMPREHENSIVE EXAMINATION (Closed Book)

Course No.: ES UC263

Course Title: Microprocessor Programming and Interfacing

Date: June 10, 2004 Time: 3 Hours M.M. = 120 (40 %)NOTE: (i) Answer all the questions. All questions to be answered in the answer sheet only. (ii) Question paper contains **SEVEN** Pages. (iii) Answer all the parts of a question in continuation. (iv) Do not leave any blank page(s) in between the answers. (v) Do not write any thing on the question paper except your hall ticket number. (vi) Cross the blank page (s), if any. (vii) **QUESTION 1** Choose the most appropriate one. Execution of 'MOV 43H[SI], DH' instruction will (a) Increment the IP by 1. (i) (ii) Increment the IP by 2. (iii) Increment the IP by 3. Will not change the value of IP. (iv) In code format for a MOV instruction, what is the significance of the marked bits? These represent the "MOD" bits (i) (ii) These represent the "D and W" bits (iii) These represent the "REG" bits (iv) These represent the "R/M" bits

- What is the main difference between 'REPEAT UNTIL' and 'WHILE DO' structures?
  - In WHILE DO condition is checked before the action is done, whereas in REPEAT UNTIL action is done (once) before the condition is checked.
  - In WHILE DO action is done (once) before the condition is checked, whereas in REPEAT UNTIL condition is checked before the action is done.
  - (iii) WHILE DO and REPEAT UNTIL are same in every aspect.
  - (iv) None of the above is correct.

|   | 47   |
|---|------|
| d) Initialization instructions included in a program are used for  (i) Defining the symbolic address used by the programmer in the program  (ii) Put appropriate addresses in all the segment registers including pointers  (iii) Put appropriate addresses in all the segment registers except CS register  (iv) All of the above. |      |
| <ul> <li>Which of the following will provide the highest performance and capability?</li> <li>(i) Protected Mode</li> <li>(ii) Real-address Mode</li> <li>(iii) System Management Mode.</li> <li>(iv) Performance and capability of a microprocessor does not depend operating mode.</li> </ul>                                     | on   |
| f) A Label is  (i) Starting address of a program.  (ii) An address referred in a jump or call instruction.  (iii) Type of the data used.  (iv) Return address.  |      |
| g) The instruction MOV CS: [BX], DL is a  (i) Single byte instruction.  (ii) Double byte instruction.  (iii) Three byte instruction.  (iv) Four byte instruction.   |      |
| <ul> <li>(i) To transfer immediate data 0531H in register AL.</li> <li>(ii) To transfer lower byte i.e. 31H of immediate data 0531H in register AL.</li> <li>(iii) To transfer upper byte i.e. 05H of immediate data 0531H in register AL.</li> <li>(iv) To transfer a byte of data from port 0531H to the AL register.</li> </ul>  |      |
| <ul> <li>i) If the codes for ES = 00, CS = 01, SS = 10, and DS = 11 then segment of prefix for DS will be</li> <li>(i) 26H</li> <li>(ii) 2DH</li> <li>(iii) 36H</li> <li>(iv) 3DH</li> </ul>  | over |
| j) If the opcode for 8086 IN (fixed port) is given below, then the data type is  0 1 1 0 0 0 1 0 0 1 1 0 1  (i) Byte (ii) Word (iii) Double Word (iv) May be any one of the above.  |      |
|   |      |

th

|     | (k)   |                             | S = 0000H, CS = 0001H, SS = 0010H, and DS = 0011H then the execution V [0000], AL will result in Copying the byte in AL to a memory location at 00000H Copying the byte in AL to a memory location at 00010H Copying the byte in AL to a memory location at 00100H Copying the byte in AL to a memory location at 00110H | n of    |
|-----|---|-----------------------------|--|---------|
|     | (1)   | Wha (i) (ii) (iii) (iv)     | t is the purpose of putting INT 3 instruction in the end of the program?  To transfer the result into accumulator.  To execute the loop of the previous instructions, thrice.  Terminate the execution of the program.  Multiply the result available in accumulator by integer 3.                                       | Î       |
|     | (m)   | If the (i) (ii) (iii) (iv)  | top of the stack is specified as 45633 then the content of SS: SP may be 4000:5633 4500:0633 4200:3633 Any one of the above.   | 1       |
|     | (n)   | The i (i) (ii) (iii)        | instruction MOV DX, 4527H[BX] is a Single byte instruction. Double byte instruction. Triple byte instruction. Four byte instruction.   |         |
|     | (0)   | Instruction (ii) (iii) (iv) | uction JAE in a program can be replaced by instruction: JNBE JNB JNAE JBE  | 1       |
| OUI | ESTIO   | N 2                         |  |         |
| (a) | Des   | scribe                      | the function of the stack in the system and outline which registers the Create this structure.   | PU<br>3 |
| (b) | What is BIOS? What is the use of it?  |                             |  | (3)     |
| (c) | Describe one instruction each that uses and modifies the registers DX and SI, without specifically mentioning it in the format. |                             |  | _       |
| (d) | Wh<br>(i)<br>(ii)   | , O                         | emory model type is used for the following memory requirements:<br>one data segment of 64k bytes and three code segments.<br>ny number of code and data segments.  | 2       |
| (e) |   |                             | he purpose of including assembler directives or pseudo operations in the Al we use the 'EVEN' directive in 8086 ALP?   | LP?     |

(f) Given that the contents of CS = 200Ah, SS = 5539h, IP = 0100h, and SP = BE05h, calculate the 20-bit physical memory addresses for:

(i) Top of the stack

(ii) Next instruction to be fetched

#### **OUESTION 3**

Suppose DS = 5678h, ES = 2345h, CS = 6789h, SS = 0F0000h, BX = 3000h, BP = 1111h, DI = 2000h, SI = 3000h. What physical addresses in memory are accessed by the following instructions?

(i) MOV AX, [BP]

(ii) MOV [SI], 0CDEFh

(iii) MOV BX, [BX+DI+6789h]

(iv) MOV DX, CS: [SI]

(v) MOV BH, [BP+DI+3355h]

- (b) Explain the coding template used for 8086 instructions which MOV data between registers or between a register and a memory location.
- (c) Show the positions of various flag bits in 8086 flag register and briefly explain the function of each flag bit.

## **QUESTION 4**

- (a) Draw the timing diagram and list the sequence of operation that take place during the execution of a read machine cycle in 8086 microprocessor.
- (b) Suppose CS = 1122h, DS = 2233h, ES = 3344h, SS = 4455h; then show the data arrangement in memory with the corresponding addresses of MULTIPLICAND, MULTIPLIER and PRODUCT after the execution of the following ALP.

DATA HERE SEGMENT

MULTIPLICAND DW 204Ah MULTIPLIER DW 3B2Ah PRODUCT DW 2 DUP(0)

DATA\_HERE ENDS

CODE HERE SEGMENT

ASSUME CS:CODE\_HERE, DS:DATA\_HERE

START:

MOV AX, DATA\_HERE

MOV DS, AX

MOV AX, MULTIPLICAND

MUL MULTIPLIER
MOV PRODUCT, AX
MOV PRODUCT, AX
MOV PRODUCT+2, DX

CODE\_HERE ENDS

(c) Can we replace instruction PRODUCT DW 2 DUP(0) in the above program with instruction PRODUCT DD DUP(0)? What is the difference between the two instructions?

## **QUESTION 5**

- (a) What are the possible types of unconditional jump permitted in 8086 ALP? Give the coding templates for these types and explain them briefly.
- (b) Explain the assembly language program development algorithm with the help of a flow chart showing the sequence in which various program development tools are used and the extensions assigned to the files generated by these tools.
- (c) What will be the contents of the AX, BX, CX, and DX registers after the execution of the following code segment.

  Assume the SS and DS registers point to .data

.CODE

NUMB EQU 02 GRADE EQU 03

MOV BP. OFFSET MYTABLE

MOV BX, 0

MOV BL, [BP + 2]

MOV DI, GRADE

MOV SI, GRADE + 2

MOV CX, [BX + DI + NUMB]

MOV BL, [BP + 3]

MOV AX, [BX + SI + NUMB]

#### .DATA

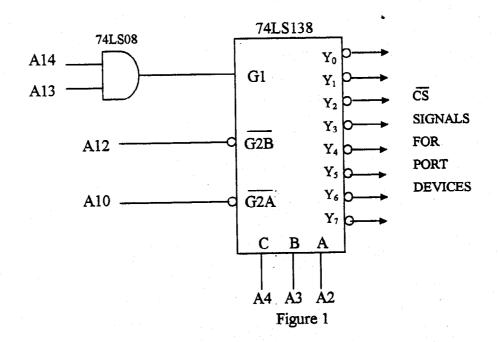
| MYTABLE | DB | 4, 11, 20, 28                               |     |
|---------|----|---|-----|
| JIM     | DB | 00h, 01h, 03h, 04h, 05h, 56h, 19h           |     |
| PAUL    | DB | 08h, 09h, 0Ah, 0Ch, 0Dh, 58h, 19h, 23h, 78h |     |
| STEVE   | DB | 10h, 11h, 12h, 14h, 15h, 16h, 17h, 18h      |     |
| DAVE    | DB | 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh 1Fh 20h         | 10h |

#### **QUESTION 6**

- (a) The interfacing for connecting eight EPROMS in parallel on a common address bus and common data bus in a certain system is done as follows:
  - (i) Address bits A13, A14 and A15 of 8086 are connected to A, B and C of 74LS138 (3  $\times$  8 decoder).
  - (ii) A12 address bit is connected to G2A of 74LS138. RD control signal is connected to G2B of 74LS138. +5V is connected to G1 of 74LS138.
  - (iii) Remaining address bits i.e. A0 A11 of 8086 are directly connected to each EPROM.

Draw the schematic of the interfacing and prepare the address decoder worksheet showing address decoding for eight EPROMS.

(b) Draw the address decoder worksheet to specify the Hex port device addresses of the schematic for 74LS138 shown in figure 1.



### **OUESTION 7**

- (i) Identify the port addresses of the control register and counter 2 in figure 2.
- (ii) Write a subroutine to initialize counter 2 in Mode 0 with a count of 50,000<sub>10</sub> for figure 2 interfacing scheme. The subroutine should also include reading counts on the fly; when the count reaches zero, it should return to the main program.

#### **QUESTION 8**

Write a BSR control word subroutine to set bits PC<sub>7</sub> and PC<sub>3</sub> of 8255 and reset them after 1 second. Use the schematic shown in figure 3 and assume that you can obtain a delay of 1 second by writing "CALL DELAY" in your program.

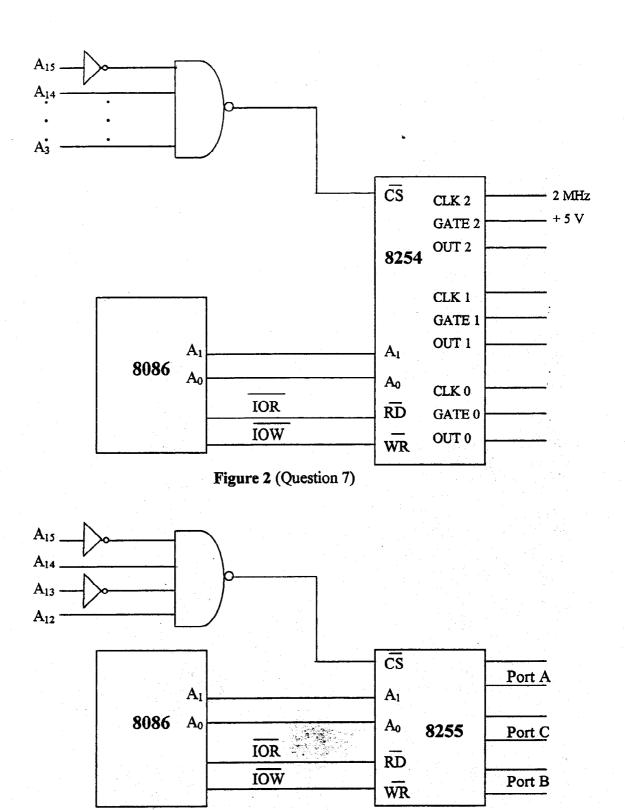


Figure 3 (Question 8)

# BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai
II Year (EEE/EIE/CSE) 2003 – 2004, Semester - II
TEST - II (Open Book)

Course Title: Microprocessor Programming and Interfacing (ES UC263)

Date: 25th April, 2004

Time: 50 Minutes

 $M.M. = 40 (\approx 13 \%)$ 

NOTE: (i) Only Text Book is allowed.

- (ii) Answer all the questions.
- (iii) Calculator is not allowed.
- (iv) Answer all the parts of a question in continuation.
- (v) Do not leave any blank page(s) in between the answers.
- Q. 1 (a) Given that the contents of DS = 6400h, BX = 0743h, BP = CA40h, SI = 2100h and DI = 04A4h, and that BETA is a data label with offset 0202h, for each of the following instructions identify the addressing mode and calculate the 20-bit physical memory address of the source or destination data:
  - (i) MOV [BX + DI + 4], AX
  - (ii) MOV BETA, BL

[ 08 ]

- (iii) MOV AH, [BP][DI + BETA]
- (iv) LODSB

- (b) Describe the function of the stack in the system and outline which registers the CPU uses to create this structure.
- Q. 2 (a) Which standard structure is being represent by the following program segment?

MOV CX, 10

XOR AX, AX

[2]

ADDSTART: CMP CX, 0

JE ADDEND

ADD AX, CX

DEC CX

JMP ADDSTART

ADDEND:

Suppose DS = 5678h, ES = 2345h, CS = 6789h, SS = 0F000h, BX (b) = 3000h, BP = 1111h, DI = 2000h, SI = 3000h. Generate the machine code values for the following 5 instructions. MOV [SI],0CDEFh [ 08 ] MOV BX, [BX+DI+6789h] MOV BH, [BP+DI+3355h] MOV DX, CS: [SI] Which of the following are invalid 8086 assembler language Q. 3 (a) instructions? State the error for each invalid instruction. Assume that the variables VAR1 and VAR2 are both defined as BYTEs: MOV VAR1, VAR2 [6] MOV SP, WORD PTR VAR1[DI] MOV CX, VAR1 MOV AH, VAR2[BX][DI] +144/2 MOV ES, CX Write down a suitable instruction for the following: **(b)** [ 04] Mask in LS 4 bits of AL (i) Divide AX by two (ii) Set MS bit of CX (iii) Clear AX (iv) What will be the content of the specified register after the **Q.4** execution of the following code segments: (i) MOV AX, 15 **AAA** [ 10 ] (ii) MOV AX, 0105h AAD (iii) MOV AL, 15 AAM (iv) MOV AL, '3' OR AL, 00100000b (v) MOV AL, 01h ROR AL, 1

Name:

ID. No.:

# BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai .

B.E. (Hons.) EEE/EIE/CS

Year II – Semester II 2003 – 2004

QUIZ I (Closed Book)

Course: ES UC263 [Microprocessor programming & Interfacing]

**Date: 23 March 2004** 

Time: 20 Minutes

M.M. = 20 (6.5 %)

**QUESTION NO.1:** Choose the most appropriate one.

 $[10\times1=10]$ 

- a. Execution of 'PUSH' instruction will
  - (i) Decrement the SP by 2.
  - (ii) Decrement the SP by 2 if PUSHing a 'word' or decrement the SP by 1 if PUSHing a 'byte'.
  - (iii) Does not affect the SP.
  - (iv) Increment the SP by 2.
- b. The code for a MOV instruction is given as 1000101111100011, what is the data type:
  - (i) Word

- (ii) Byte
- (iii) May be word or byte
- (iv) None of the above
- c. The instruction MOV DX, 4527H[BX] is a
  - (i) Single byte instruction.
  - (ii) Double byte instruction.
  - (iii) Triple byte instruction.
  - (iv) Four byte instruction.

- d. What is the purpose of putting INT 3 instruction in the end of the program?
  - (i) To transfer the result into accumulator.
  - (ii) To execute the loop of the previous instructions, thrice.
  - (iii) Terminate the execution of the program.
  - (iv) Multiply the result available in accumulator by integer 3.

#### e. A Label is

- (i) Starting address of a program.
- (ii) An address referred in a jump or call instruction.
- (iii) Type of the data used.
- (iv) Return address.
- f. Initialization instructions included in a program are used for
  - (i) Defining the symbolic address used by the programmer in the program
  - (ii) Put appropriate addresses in all the segment registers including pointers.
  - (iii) Put appropriate addresses in all the segment registers except CS registers
  - (iv) All of the above.
- g. Which one of the following instruction is correct:
  - (i) MOV CS, 1234H
  - (ii) PUSH AL
  - (iii) MOV [BX][BP], DX
  - (iv) All of these are incorrect.
- h. Which of the following will provide the highest performance and capability?
  - (i) Protected Mode
  - (ii) Real-address Mode
  - (iii) System Management Mode.
  - (iv) Performance and capability of a microprocessor does not depend on the operating mode.

| i.        | What i         | is the main difference between 'REPEAT UNTIL' and 'WHI                  | LE DO                                  |
|-----------|----------------|---|--|
|           | structur       | ires?   |  |
|           | (i)            | In WHILE DO condition is checked before the action is done, wh          | iereas in                              |
|           |                | REPEAT UNTIL action is done (once) before the condition is check        | ked.                                   |
|           | (ii)           | In WHILE DO action is done (once) before the condition is               | checked                                |
|           |                | whereas in REPEAT UNTIL condition is checked before the action          | is done.                               |
|           | (iii)          | WHILE DO and REPEAT UNTIL are same in every aspect.                     |  |
|           | (iv)           | None of the above is correct.   |  |
| j.        | If the to      | top of the stack is specified as 45633 then the content of may SS: SP m | ay be                                  |
|           | (i)            | 4000:5633   |  |
|           | (ii)           | 4500:0633   |  |
|           | (iii)          | ) 4200:3633   |  |
|           | (iv)           | Any one of the above.   |  |
| <u>Q1</u> | U <b>ESTIO</b> | ON NO.2: Fill in the blank appropriate word(s). [10 $\times$            | 1 = 10]                                |
| a.        | What is        | instruction is used to perform the following function in 8086 Micropr   | ocessor                                |
|           | (i)            | Multiply signed byte by byte or signed word by word                     | ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,, |
|           | (ii)           | Invert each bit of a byte or a word.                                    |  |
| b.        | Write o        | one line description for the following 8086 Mnemonics:                  |  |
|           | (i)            | ROR:  |  |
|           |                |   |  |
|           | (ii)           | SHR:  |  |
|           |                |   |  |
|           |                |   |  |
| c.        | How m          | nany GPRs are in the following Microprocessors:                         |  |

**Z-80** 

(i)

(ii)

|        | d. BP and SP work with  |
|--------|---|
|        | e. Can BH and BL form effective address?  |
|        | f. Is RAM an internal part of the 8086 Microprocessor Chip?                     |
|        | g. What information is inferred when the status of Interrupt Flag is one?       |
|        |   |
|        | h. What information is inferred when the status of the Direction Flag is Zero?  |
|        |   |
|        | i. Write the clock frequency for the following processors:                      |
|        | (i) 80286<br>(ii) P-IV  |
|        |   |
| 44<br> | j. What will be the Hex-code corresponding to MOV CL,[BX], if Opcode for MOV is |
|        | 100010.   |
|        |   |
|        |   |
|        |   |
|        |   |

## BITS, PILANI – DUBAI CAMPUS

Knowledge Village, Dubai II Year (EEE/EIE/CSE) 2003 – 2004, Semester - II TEST - I (Closed Book)

Course Title: Microprocessor Programming and Interfacing (ES UC263)

Date: March 7, 2004 Time: 50 Minutes M.M. = 40 (≈13 %)

| <ul> <li>(ii) All questions to be answered in the answer sheet onl</li> <li>(iii) Calculator is not allowed.</li> <li>(iv) Answer all the parts of a question in continuation.</li> <li>(v) Do not leave any blank page(s) in between the answer.</li> <li>1. Fill in the blank with appropriate word(s)</li> </ul> | _                  |
|---|--------------------|
| <ul><li>(iv) Answer all the parts of a question in continuation.</li><li>(v) Do not leave any blank page(s) in between the answer.</li></ul>  | l <b>y.</b>        |
| (v) Do not leave any blank page(s) in between the answ  |                    |
|   |                    |
| 1. Fill in the blank with appropriate word(s)   | ers.               |
|   | [1 each]           |
| (i) The main difference between 8086 and 8088 microproce  | essors is          |
| (ii) A microprocessor is said to be 8/16 bit microprocessor of  | on the basis of    |
| (iii) The reason for multiplexing the address and data buses  | of 8085 is         |
| (iv) Latching of any data on a bus will result in   | •••••              |
| (v) Control signal needed for demultiplexing the data and 8085 microprocessor is  | d address buses in |
| (vi) MIPS stands forand is a rough measu  | ıre of             |
| (vii) The advantage of 'Packed BCD' over BCD numbers is .   |                    |
| (viii) Name any two 32-bit microprocessors.   |                    |
| (ix) The main role of timing and control unit in a microproc  | essor is           |
| (x) In a microprocessor 'Flags' are used for  |                    |

| 2. | In reference to 8086 microprocessor, answer the following:                    | [3+3+4]             |  |  |  |
|----|---|---------------------|--|--|--|
|    | (i) What is the purpose of queue formation in BIU?                            |                     |  |  |  |
|    | (ii) What are the advantages of doing segmentation of memory?                 |                     |  |  |  |
|    | (iii) Write the assembly language statement, which will perform the following |                     |  |  |  |
|    | operations:   |                     |  |  |  |
|    | (a) Copy the BX register contents to SP register.                             |                     |  |  |  |
|    | (b) Load the number F3H into AL register.                                     |                     |  |  |  |
| 3. | Explain the functions of the following instructions:                          | [2 each]            |  |  |  |
|    | (i) MOV BL, [437AH]   |                     |  |  |  |
|    | (ii) MOV CX, 437BH  |                     |  |  |  |
|    | (iii) MOV CX, [32AAH]   |                     |  |  |  |
|    | (iv) MOV [32AAH], CX  |                     |  |  |  |
|    | (v) MOV AX, AX  |                     |  |  |  |
|    |   |                     |  |  |  |
| 4. | (a) What is wrong in the following instructions:                              | [1 each]            |  |  |  |
|    | (i) ADD [4321H], [3214H]  |                     |  |  |  |
|    | (ii) MOV AX, [432AH]  |                     |  |  |  |
|    | (iii) MOVAL, CX   |                     |  |  |  |
| •  | (iv) ADD BH: CL   |                     |  |  |  |
|    | (v) MOV AX, 2000:437AH  |                     |  |  |  |
|    |   |                     |  |  |  |
|    | (b) Indicate the status of Carry, Parity, Auxiliary Carry, Ze                 | ro, and Sign Flags, |  |  |  |
|    | when 8086 microprocessor executes the following instruction                   | ons: [5]            |  |  |  |
|    | MOV CX, B0A7H   |                     |  |  |  |
|    | MOV AX, 1122H   |                     |  |  |  |
|    | ADD AX, CX  |                     |  |  |  |
|    |   |                     |  |  |  |
|    |   |                     |  |  |  |