BITS PILANI DUBAI CAMPUS
DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI
I SEMESTER 2013-2014
COMPREHENSIVE EXAMINATION

COURSE NO	: **EEE/ECE/CS/INSTR F 215**	DURATION	: 3 HOURS
COURSE NAME	: **Digital Design**		**II Years**
WEIGHTAGE	: 40% (80 Marks)		
Date	: **08-01-2014 FN**		

Calculators are not allowed.
Answer Part A, Part B and Part C in separate answer sheets.

PART – A

1. Convert (show a complete working of all the steps used during conversions)
   a. (0.625) to binary. [2]
   b. $(231.3)_4$ to base 7. [2]
2. A switching network has: 2 control inputs- C_1 and C_2; 2 data inputs- X_1 and X_2; and 1 output- Z. The network performs one of the logic operations: AND, OR, EQU (Equivalence), or XOR (exclusive-OR) on the two data inputs depending on control inputs as given below:

C_1	C_2	Function performed by network
0	0	AND
0	1	OR
1	0	EQU (Equivalence)
1	1	XOR (exclusive-OR)

   a. Derive a truth table for Z. [3]
   b. Use K-map method and find a minimum AND-OR gate network to realize Z;
      i. Obtain the expression for Z in SOP form. [3]
      ii. Also draw the logic diagram to realize Z. [3]

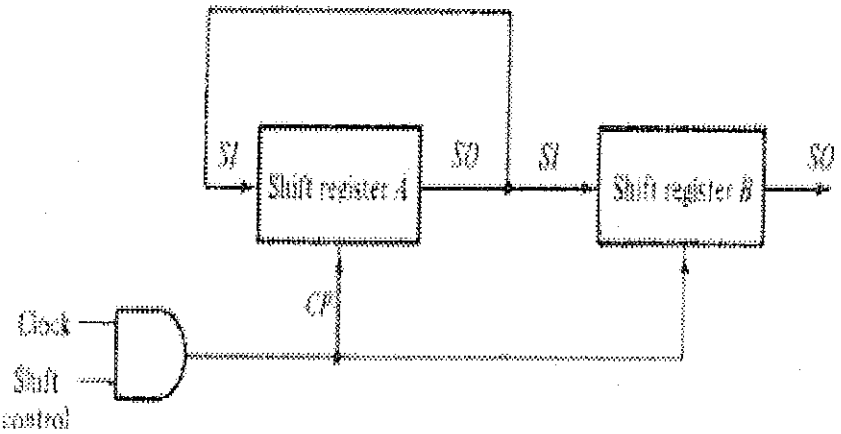
3. $F(a,b,c,d,e)=\sum m(0, 3, 4, 5, 6, 7, 8, 12, 13, 14, 16, 21, 23, 24, 29, 31)$
   a. Find the essential prime implicants using a K-map and indicate why each one of the chosen prime implicants is essential. [4]
   b. Find all the prime implicants by using the K-map. [5]
4. Realize: $F(w,x,y,z)= xy'z + x'yz + w$ using
   a. 3-input NAND gates only [5]
   b. 3-input NOR gates only [5]
5. Design a network of AND & OR gates to convert from excess-3 code (use literals: a b c to 8-4-2-1 BCD Code (use literals: W X Y Z). [4]

6. Show how 16-to-1 and 2-to-1 multiplexers could be connected to form a 32-to-1 MUX with 5 control inputs. [4]

PART B

1. Answer the following questions with respect to the clocked SR latch [2+2+2+2M]
   a) with the help of a diagram draw and explain the working of an SR latch constructed using Nand gates.
   b) Give the characteristic table.
   c) Give the characteristic equation.
   d) d. Give the graphic symbol

2. For the given figure give the states of register A , register B and serial output of register B for four clock cycles. The initial state of register A is 1011 and the initial state of Register B is 0010 [4M]



3. Give answers in one word or in one sentence. [1 X 5 = 5M]
   a) In a flip flop what does toggle mean ?
   b) A ring counter with five flip flops has a total of _____ states.
   c) A four bit synchronous counter use flip flops with a propagation delay of 15ns. The maximum possible time required for change of state is _____.
   d) How many flip flops are required to construct a mod 30 counter.
   e) Shifting a register content to the left by one position is equivalent to the _____ arithmetic operation.

4. [6+2M]
   a. With the help of clocked JK flip flops and timing diagrams, explain the working of a three bit ripple up counter.
   b. b. Give the truth table for clock transitions.

5. a. What is meant by a Synchronous counter? [1M]
   b. Design a Mod 5 synchronous counter using JK flip flops. [9M]

6. Explain how a shift register can be used as a ring counter giving the waveforms as the output of the flip flops. [5M]

PART – C

1. Explain the concept of paging with respect to virtual memory. [4 M]

2. Indentify the behavior of the IO devices, i.e. specify whether they are input or output device
   1. Keyboard 2. Mouse 3. Graphic display 4. Wireless LAN [4M]

3. Draw the logic diagram of the digital circuit specified by the following Verilog description. [6 M]

```
module Circuit(A,B,C,D,F);
input A,B,C,D;
output F;
wire w,x,y,z,a,d;
and (x,B,C,d);
and(y,a,C);
and(w,z,B);
or (z,y,A);
or(F,x,w);
not(a,A);
not(d,D);
endmodule
```

4. Multiply 14 by – 5 using Booth's multiplication algorithm. [10 M]

5. Tabulate the PLA programming table for the four Boolean functions listed below, minimize the number of product terms and draw the PLA structure. [10M]

   $A(x, y, z) = \sum (1, 2, 4, 6)$
   $B(x, y, z) = \sum (0, 1, 6, 7)$
   $C(x, y, z) = \sum (2, 4, 5, 6, 7)$
   $D(x, y, z) = \sum (1, 2, 3, 5, 7)$

6. Tabulate the truth table for an 8 X 4 ROM that implements the Boolean functions listed below. [6 M]

   $A(x, y, z) = \sum (1, 2, 4, 6)$
   $B(x, y, z) = \sum (0, 1, 6, 7)$
   $C(x, y, z) = \sum (2, 4, 5, 6, 7)$
   $D(x, y, z) = \sum (1, 2, 3, 5, 7)$

   Considering ROM as memory, specify the memory contents of 1 and 5.

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Dubai International Academic City, Dubai

Year II – Semester I 2013– 2014

TEST II (open book)

Course No.: **EEE/ECE/CS/INSTR F 215** Course Title: **Digital Design**

Date: 10.12.13 **Time: 50 Minutes** **Max. Marks = 45** **Weightage (10%)**

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1. Construct the state diagram for the shift register shown below with X as input and Z as output, [8M]

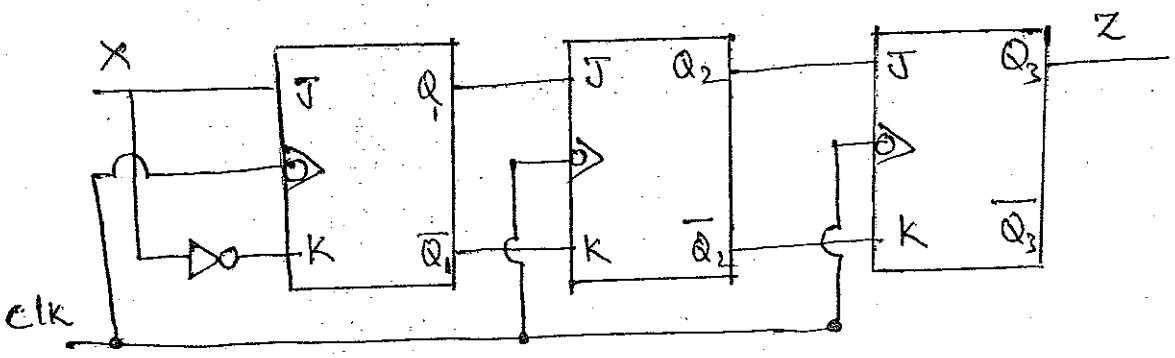

fig. 1

2. i) For the sequential circuit, shown below find the state equation for each flip flop. [6 M]
   ii) Also construct state table
   iii) What is the output sequence when input sequence is x = 01100

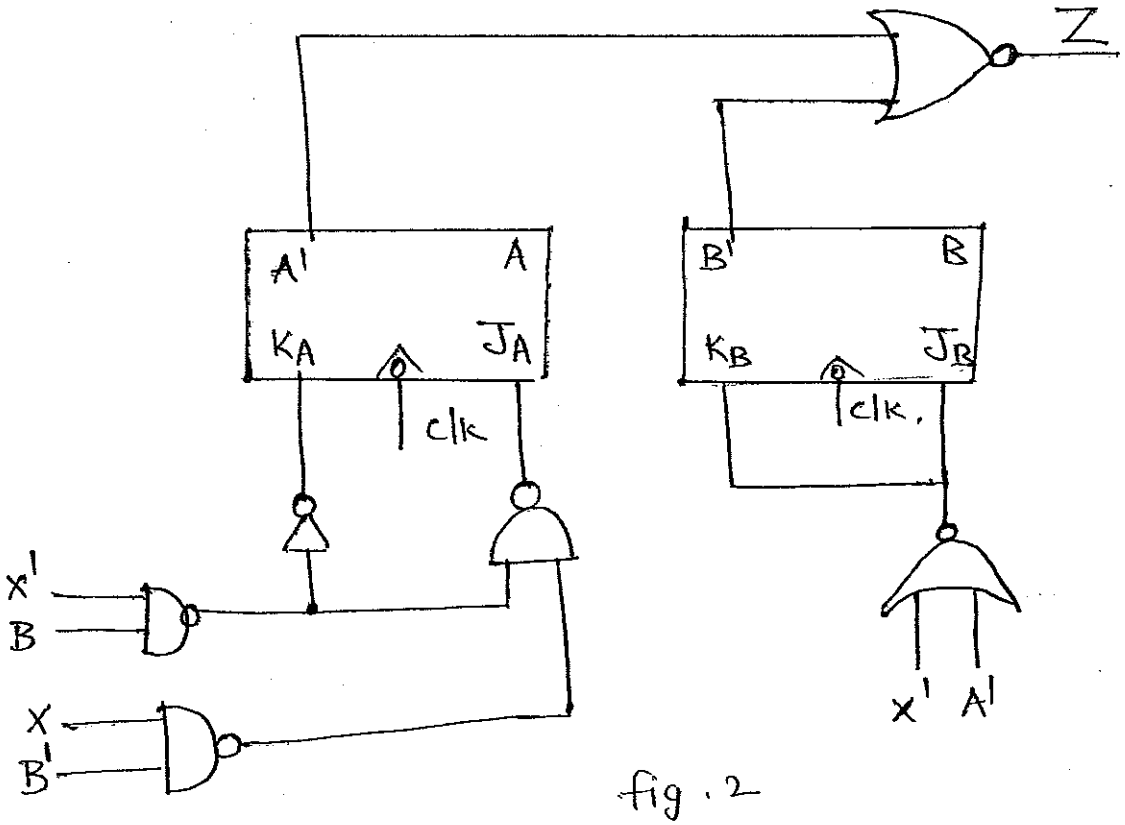

fig. 2

3. A Priority Encoder is designed for navigation purpose, here for example, the angular or rotary position of a compass is converted into a digital code by a 74LS148 8-to-3 line priority encoder and inputted to the systems computer to provide navigational data and an example of a simple 8 position to 3-bit output compass encoder is shown in fig 3.

a) Draw the truth table

b) Give the Boolean expression for the three outputs Q0, Q1, Q2

c) Finally draw how this digital encoder can be constructed using logic gates. Assume D7 has the highest priority and D0 has the lowest priority. [4 +2+2M]

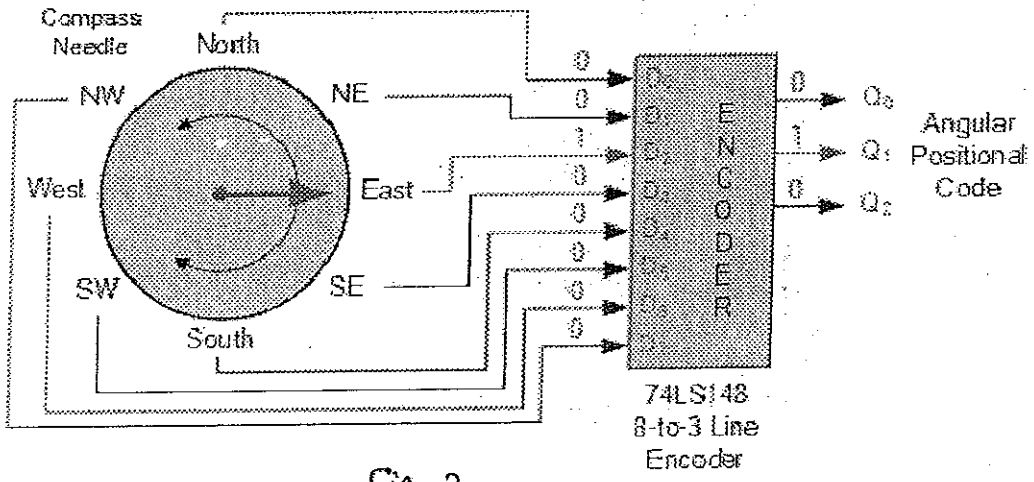

fig · 3

4. The given block diagram is of a decimal to BCD encoder. Give the status of the input and the output lines required to generate the number 7. [2M]

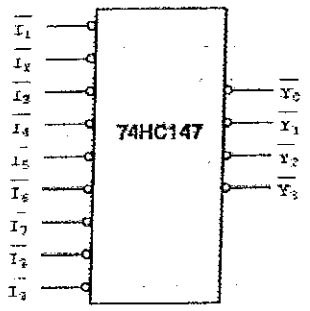

fig · 4

Design only the **sum** function of the full adder using only 2 **X 1 MUX.** [5 M]

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Year II – Semester I 2013– 2014

TEST I

Course No.: **EEE/ECE/CS/INSTR F 215** Course Title: **Digital Design**

Date: 08.10.13 **Time: 50 Minutes** **Max. Marks = 45** **Weightage (15%)**

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1. Find all prime implicants for the Boolean function given below and determine which are essential. **(5 Marks)**

$$F(A,B,C,D) = \sum (0,2,3,5,7,8,10,11,14,15)$$

2. Simplify the following Boolean function F together with don't care conditions and then express it in the simplified sum of minterms form **(5 Marks)**

$$F(A,B,C,D) = \sum (4,5,6,7,12,13,14)$$
$$d(A,B,C,D) = \sum (1,9,11,15)$$

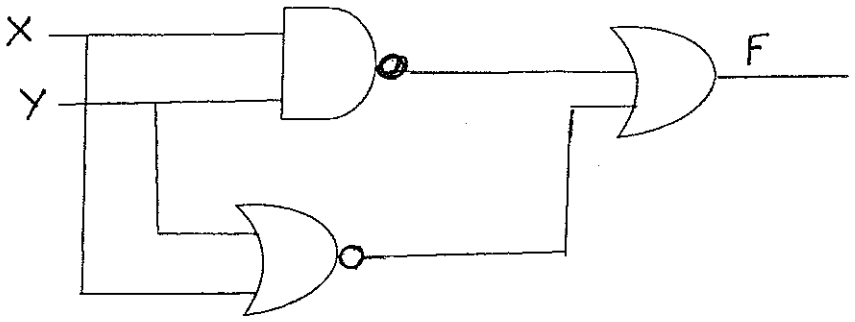
3. Draw the logic diagram that implements the **compliment** of the following function. **(5 Marks)**

$$F(A,B,C,D) = \sum (0,1,2,3,4,8,9,10,11,12)$$

4. Find the minimum number of gates required to implement the function given below **(2 Marks)**

$$A + AB^1 + AB^1C$$

5. Draw the truth table for the following logic diagram. **(3 Marks)**



ID NO: ---------- Instructor Name:----------

NAME: ----------

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QUIZ II

SET B

Course No.: **EEE/ECE/CS/INSTR F 215** Course Title: **Digital Design**

Date: 13.11.13 **Time: 20 Minutes** **Max. Marks = 15** **Weightage (5%)**

1. A 4-bit magnitude comparator has _____ no. of inputs and _____ no. of outputs. [1 M]

2. Complete the missing entries in the Full Subtractor truth table given below. [2 M]

X	Y	Z	D	B
0	0	0	0	0
0	0	1		
0	1	0		
0	1	1		
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1		

3. In a typical binary multiplier implementation using AND gates, state how new partial product gets formed? [2 M]

4. In a 4-bit magnitude comparator, "equality" Function can be implemented by just employing _____ logic [1 M]

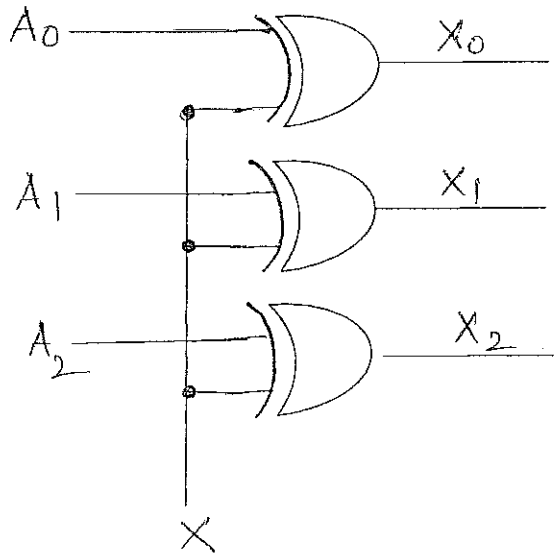
5. Draw the logic circuit for the function A (B^{I} + C) using NOR gates only. Inputs are available in both true and false (high and low) states. [2.5 M]

6. Draw the diagram of a digital circuit for the function F(X,Y,Z) = $Y^{I}Z + X Z^{I}$ using only NAND gates, assume that the inputs are available only in the true (high) state. [2.5 M]

7. _____ No. of AND gates and _____ no. of 4-bit adders would be required to produce a product of seven bits. Assume 2 binary nos.: $B_3B_2B_1B_0$ and $A_2A_1A_0$ are to be multiplied. [1 M]

8. What should be the value of X, so that we get X_0, X_1, X_2 to be one's complement of A_0, A_1, A_2

[1 M]



X =

9. Write the output of the following circuit. [2 M]