BITS PILANI DUBAI CAMPUS

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI

I SEMESTER 2012-2013

COMPREHENSIVE EXAMINATION

COURSE	: EEE/INSTR/ECE/CS F215	Digital Design II YEAR
DURATION	: 3 HOURS	
WEIGHTAGE	: 40% (80 Marks)	
Date	: 03-01-2013 AN	

Calculators are not permitted

Answer Part A, Part B and Part C in separate answer sheets

PART A

1a) Add the octal numbers **27** and **42** and express the results in binary. **[3+3+3] M**

1b) Determine the base x of the number for the following operation to be correct.

$(54)_x / 4_x = (13)_x$.

1c) Simplify the following Boolean expression and implement using NOR gates only

$F(A,B,C,D) = (A' + C)(A' + C')(A + B + C'D)$

2a) Design a half adder using 8 X 1 Multiplexer and additional control input X. Additional control input X is MSB of select input of MUX. The function of X input is as follows: When X is '0', "sum" output of half adder is delivered and when X is '1' "carry" output is delivered. **[4 M]**

2.b) Design a three input combinational logic circuit which will give three bit binary output as input added with two (X + 2) for the input decimal equivalent X is less than four and subtracted three (X - 3) for input is more than or equal to four. Implement the circuit using minimum no. of logic gates. **[5 M]**

3.a) Derive the Boolean expressions for the four bit look ahead carry generator and design a four bit parallel adder circuit using the same. **[5 M]**

3.b) Write the truth table for a BCD to seven segment decoder circuit. Using a 4x16 active low decoder and minimum no. of two input external logic gates implement the logic circuit for the segments **'e'** and **'f'** **[6 M]**

1 – 9

2 – 9

3 – 11 / 29

PART B

4a) A sequential circuit with two JK flipflop and one input x is described by the following input and output equations. $J_A = J_B = x$; $K_A = B'$; $K_B = A$ and $y = A \oplus B$

A and B are outputs of flip flops and y is output of the circuit

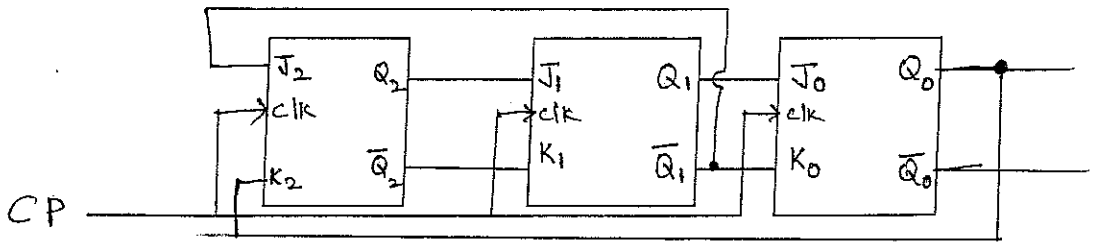
(i) Draw the sequential circuit.

(ii) Obtain the state table

(iii) Draw the state diagram

(iv) If an input sequence 0111001010 is applied to the initial state '00', find out the corresponding next state and the output sequences **[2 x 4 M]**

4 b) For the modified ring counter shown, taking Q_0=0, Q_1=0 and Q_2=1. Make a table of readings Q_0, Q_1, Q_2, J_2 and K_2 after each clock pulse. How many pulses are required before the system begins to operate as a divide-by N counter **[5 M]**



5a) Assuming unused states are driven to don't care states, Design a synchronous counter with the following repeated binary count sequence: 0, 2, 5, 7 using T flip-flop. Check what will happen when unused state occurs for the designed circuit. **[6 M]**

5b) Draw the logic diagram of a four-bit register with four D flip-flops and four 4 X 1 multiplexers with mode selection inputs s1 and s0. The register operates according to the following function table. **[4 M]**

S1	S0	Register Operation
0	0	Clear to 0
0	1	Shift right
1	0	Load new parallel data
1	1	Complement the four outputs

PART C

6) Tabulate the PLA programming table for the following Boolean functions listed below. Minimize the numbers of product terms. Consider both true and complemented outputs for minimization and also draw the PLD logic map. **[9 M]**

$A(x, y, z) = \sum (1, 2, 4, 6)$
$B(x, y, z) = \sum (0, 1, 6, 7)$
$C(x, y, z) = \sum (2, 4, 5, 6, 7)$

7a) Perform the signed number multiplication for the data 13 x -12, using Booth's algorithm. Explain each step. **[5 M]**

7b) Design a logic circuit to perform 4 x 4 bit multiplication. [5 M]

8. Answer any **three** questions from the following [3 x 3M]

1. Write the HDL description for the 2x4 active low decoder with enable pin
2. Define the term Noise Margin and Propagation delay of a digital IC
3. Draw the circuit diagram of a three input TTL NAND gate with totem pole output. Explain the operation of the circuit.
4. Using 1 K memory ICs, design a 4 K memory bank. You may use a 2 X 4 active low decoder also in the design. Also show all the signals in the design.
5. Write short note on switch tail ring counter.

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BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai
Year II – Semester I 2012– 2013
Test II (Open Book)

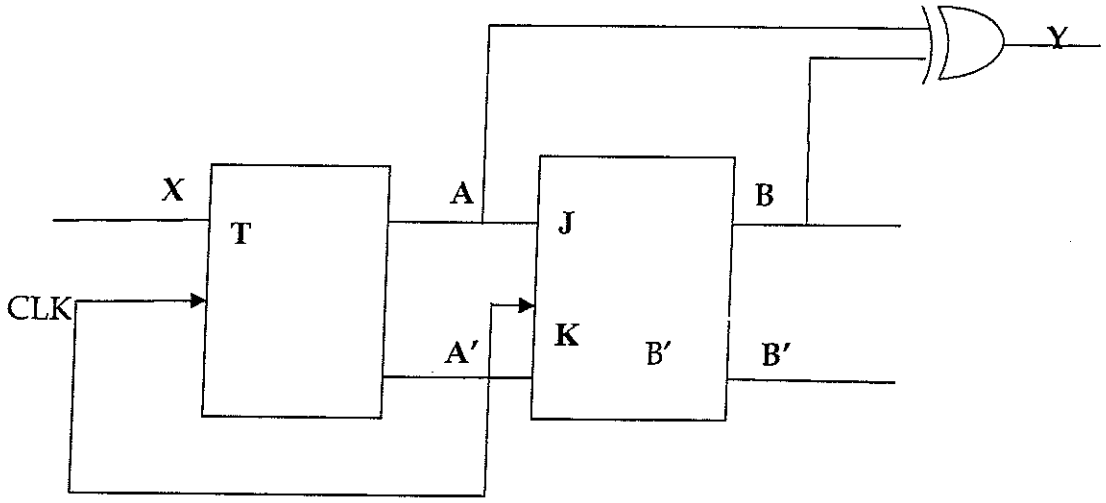
Course No.: EEE/ECE/CS/INSTR F 215 Course Title: DIGITAL DESIGN

Date: November 25, 2012 Time: 50 Minutes Max. Marks = 25

(Answer all questions. Assume positive logic)

1. A PN flip-flop has four operations, no change, clear to 0, and set 1 and complement, when inputs P and N are 01, 00, 11 and 10 respectively.
   a) Tabulate the characteristic table b) Derive the characteristic equation
   c) Show how the PN flip-flop can be converted to a D flip-flop **[9 M]**

2. For the sequential circuit given below, draw the state diagram.
   If the input sequence X = 1010101111 is applied at input T determine the next state sequence and output sequence. Assume A and B are at 0, 0 initially **[8 M]**



3. Implement the function that converts 4 bit binary code to its equivalent gray code using 4 X 16 active low decoder and external AND gates. **[8 M]**

BITS PILANI DUBAI CAMPUS

Dubai International Academic City, Dubai
Year II – Semester I 2012– 2013
Test I (closed Book)

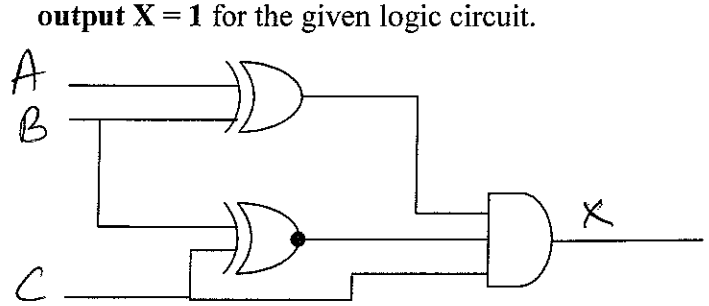
Course No.: **EEE/ECE/CS/INSTR F 215** Course Title: **DIGITAL DESIGN**

Date: October 11, 2012 Time: 50 Minutes Max. Marks = 25

(Answer all questions. Calculators are not allowed. Assume positive logic)

1. Perform the following conversions (upto 5 binary places for the fraction)
   (73.85)$_{10}$ = (_____)$_2$ = (_____)$_8$ = (_____)$_{16}$ (2M+1M+1M)

2. Consider the following logic circuit. What are the required **input values for A, B and C** to make the **output X = 1** for the given logic circuit. (4M)



3. Find a **reduced SOP function** that can detect a 8421 BCD code corresponding to a **single digit prime number from the inputs $D_8D_4D_2D_1$**. Assume the invalid codes give don't care outputs. Find the Prime Implicants and the Essential Prime Implicants of the function. (5M)

4. Draw the truth table of a **full subtractor**. Implement the circuit using **minimum number of two input EX-OR and NAND gates alone.** **(4M)**

5. Design a parallel adder for adding two 2- bit words [(A1 A0) + (B1 B0)] using half adders and minimum basic gates. (4M)

6. Plot the given function X(A, B, C, D) in a four variable K Map. **X = A+ B'C + CD'** **(4M)**

NAME:----------ID NO:----------

BITS PILANI DUBAI CAMPUS SET A

Dubai International Academic city, Dubai
Year II – Semester I 2012 – 2013
Quiz II (Closed Book)

Course No: **EEE/ECE/CS/INSTR F215** Course Title: **Digital Design**

Date: November 8th, 2012 Time: 20 Minutes Max. Marks = 20

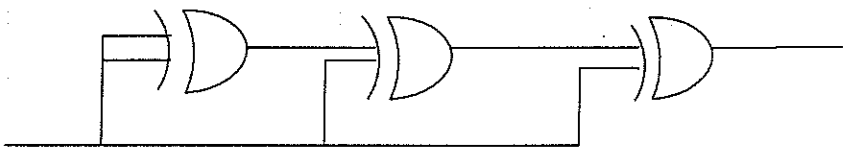
1. Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed? [2 M]

   $n-1$
   2×1 MUX

2. Implement the SUM function of a Full adder circuit with a 2 x 1 MUX and external logic gates. [4M]

3. Write the Boolean expression for a two bit word comparator circuit to check whether A > B [2 M]

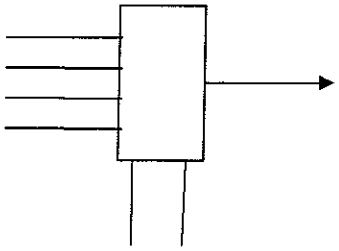
4. Write the output of the circuit shown in figure below. [3 M]



5. Design a 3 x 8 decoder using 2x4 decoders and universal logic gates. [3M]

6. Construct the logic circuit for multiplying two binary numbers (A_1 A_0) by B0 [3M]

7. Find the function F(x,y,z) implemented using the following circuit. [3M]



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