BITS, PILANI – DUBAI, ACADEMIC CITY, DUBAI
FIRST SEMESTER 2006 – 2007
ES UC241 ELECTRICAL SCIENCES – I
COMPREHENSIVE EXAMINATION (CLOSED BOOK)
MAXIMUM MARKS: 80 **WEIGHTAGE: 40%**
DATE: 08/01/08 **DURATION: 3 HOURS**

Write PART A & B & C & D in separate answer sheets.

PART A

1. Use mesh analysis to evaluate the three unknown currents i_1 i_2 &i_3 in the circuit shown in Figure1 **[5 marks]**

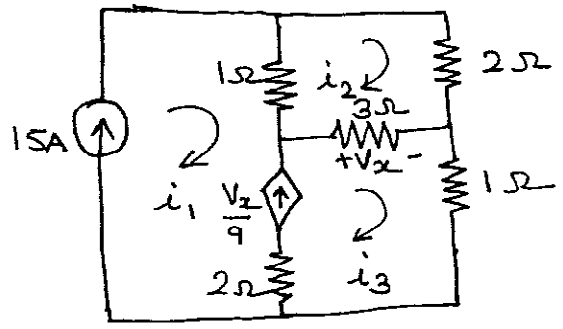

Figure 1

2. For the circuit shown in Figure 2 using thevenin's theorem calculate the current in the 2 Ω resistor **[5marks]**

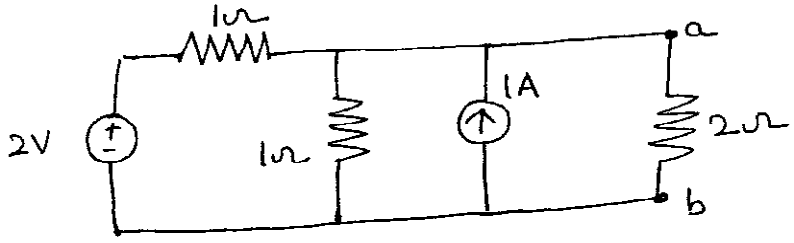

Figure 2

3. Use the principle of superposition to determine the value of i_x for the circuit shown in Figure 3. **[6marks]**

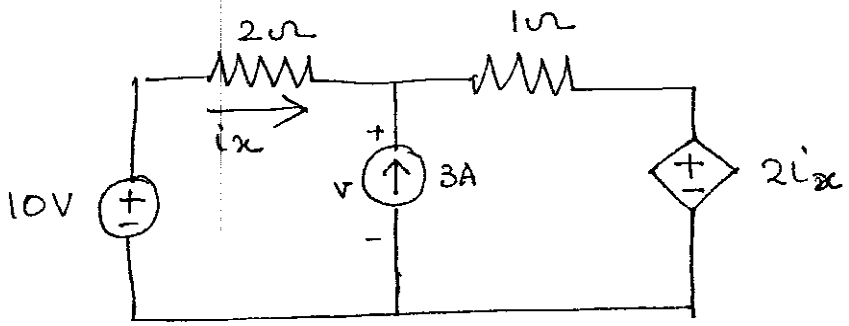

Figure3

4. Find the value of the adjustable resistance R which results in maximum power transfer across the terminals a & b of the circuit shown in Figure 4. **[5marks]**

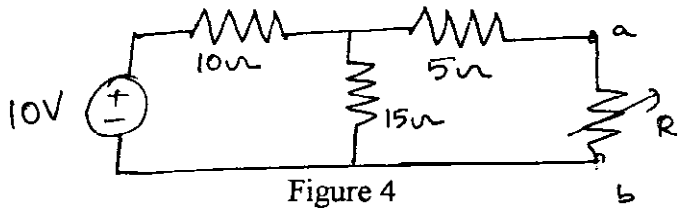

Figure 4

PART B

5. Derive the output expression V_0 for the OP –Amp circuit given in Figure 5. **[4 marks]**

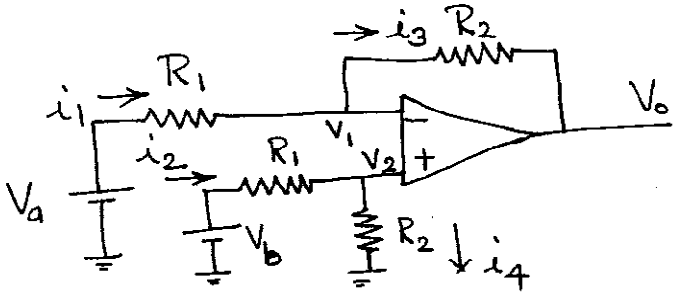

Figure 5

6. For the given circuit shown in Figure 6 find V_o & I , V_c at t <0, t >0, t= 1.3 m.sec **[10 marks]**

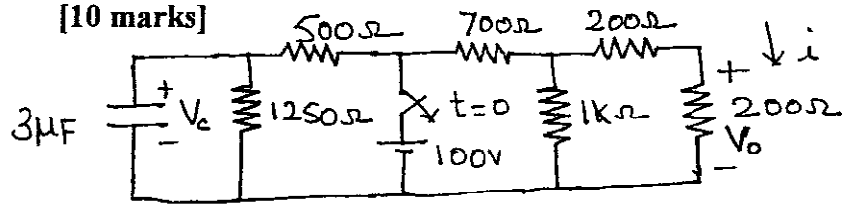

Figure 6

7. For the given circuit shown in Figure 7 the switch s has been in position 'a' for a long period of time and it is thrown to position 'b' at t =0. Determine i(t) for all t. **[12 marks]**

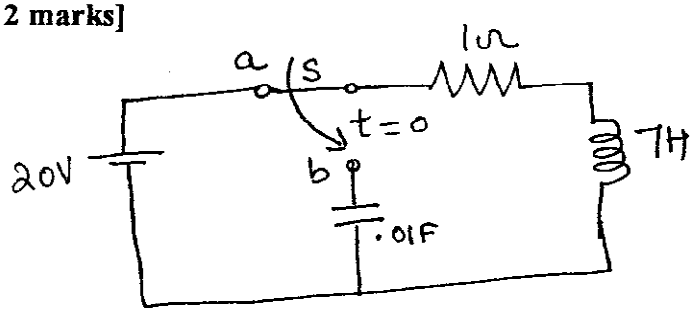

Figure 7

PART C

8. Draw the collector static characteristic of a typical P-N-P BJT(made of silicon) in common- base (CB) configuration, clearly indicate boundaries for each region of operation. **[6 Marks]**

9. For the circuit shown in Figure 8, $V_{cc} = V_{EE} = 5V$; $R_E = R_C = 2K\Omega$. Assuming that the transistor is in the active region and that $\alpha = 1$, Find i_E, V_{CB} and V_{EC}. **[7 marks]**

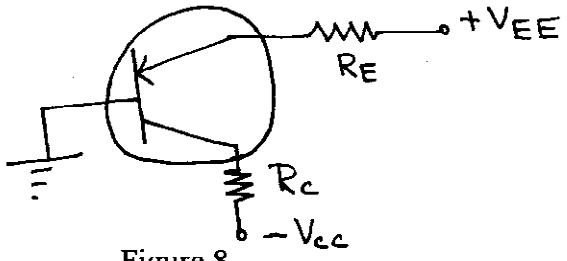

Figure 8

10. For the ideal diode circuit given in Figure 9, the input voltage is $V_s = 12\text{Sin}\omega t$ V. Determine the output voltage V_0. **[7 marks]**

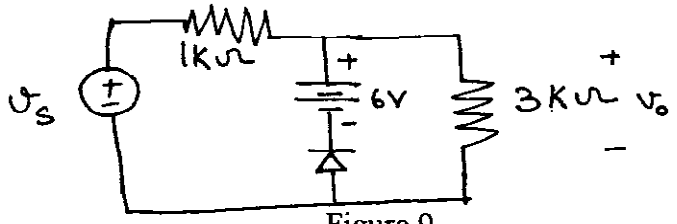

Figure 9

PART D

11. For the given circuit in Figure 10, the enhancement MOSFET has $K = 0.25\text{mA/V}^2$ and $V_t = 2V$. Given that $R_s = 0\ \Omega$ and $V_{DD} = 16V$, determine the value of R_D for which the enhancement MOSFET will operate on the border between the active and the ohmic regions when V_{GG} is 4V. **[8 marks]**

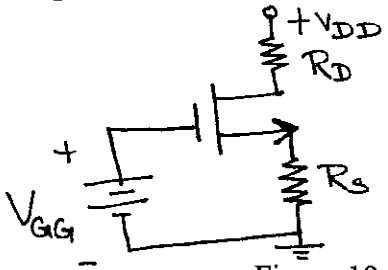

Figure 10

12. Determine the function F that characteristics the output of the logic circuit shown in Figure 11. Identify the operations performed by writing the truth table. **[5 marks]**

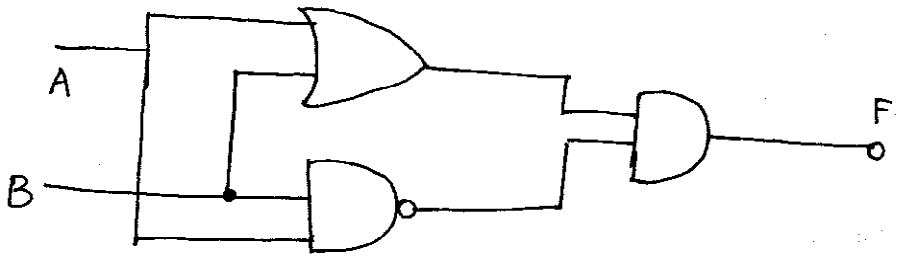

Figure 11

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FIRST SEMESTER 2006 – 2007
ES UC241 ELECTRICAL SCIENCES – I
TEST 2 (OPEN BOOK)

MAXIMUM MARKS: 20 WEIGHTAGE: 20%
DATE: 13/12/07 DURATION: 50 MINUTES

1. For the circuit shown in Figure 1, the switch is open and steady state is reached. If the switch is closed at t=0; find i(t). **[5marks]**

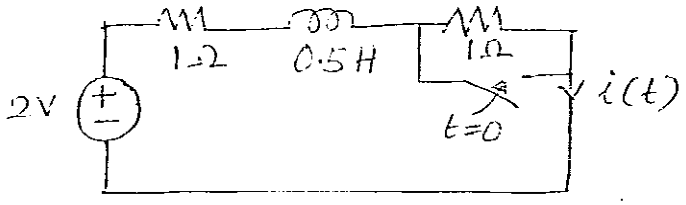

Figure 1

2. For the circuit shown in Figure 2, the switch has been in position 'a' for a long time. At t=0 the switch is thrown to position 'b'. Determine i(t) for all t. **[5 marks]**

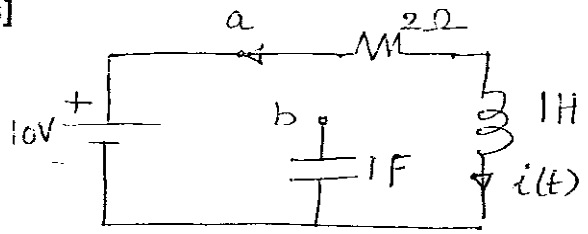

Figure 2

3. For the diode circuit shown in figure 3, V_s= 2V and the silicon diode has a saturation current of 1 nA at 300K. Given that v = 0.7 V. Find R_2 when R_1 = 1 kΩ. **[5 marks]**

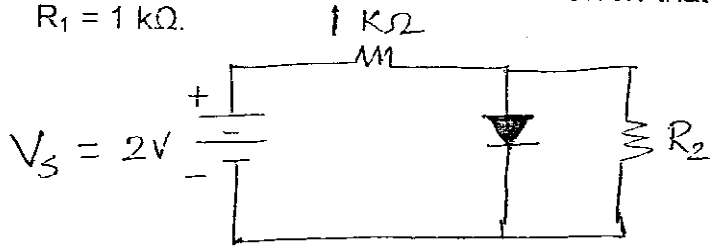

Figure 3

4. Determine the minimum and maximum load currents for which the zener diode in Figure 4 will maintain regulation. What is the minimum value of R_L that can be used?
V_z = 12 V, $I_{z\,(min)}$ = 1 mA, $I_{z\,(max)}$ = 50 mA. Assume V_z remains constant at 12 V over the range of current values. **[5 marks]**

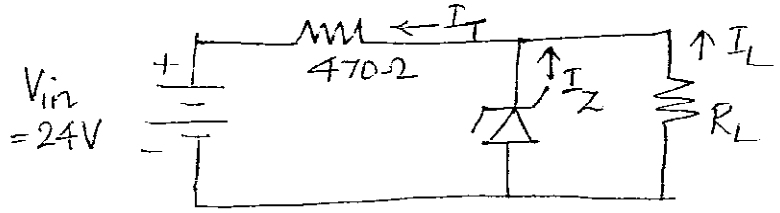

Figure 4

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FIRST SEMESTER 2007 – 2008
ES UC241 ELECTRICAL SCIENCES – I
TEST 1(CLOSED BOOK)

MAXIMUM MARKS: 25 **WEIGHTAGE: 25%**
DATE: 28/10/07 **DURATION: 50 MINUTES**

1. For the circuit shown in Figure 1, find maximum power absorbed across load resistance 5 Ω. [7marks]

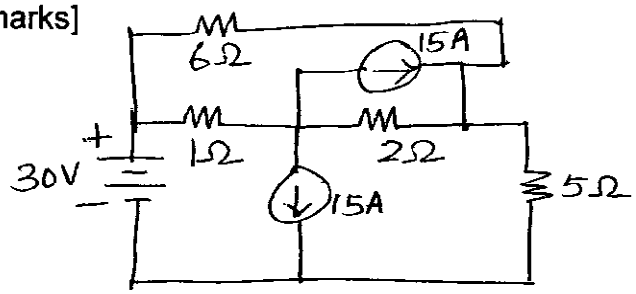

Figure 1

2. For the circuit shown in Figure 2, find current I to make V1 to zero. [6 marks] Apply nodal analysis.

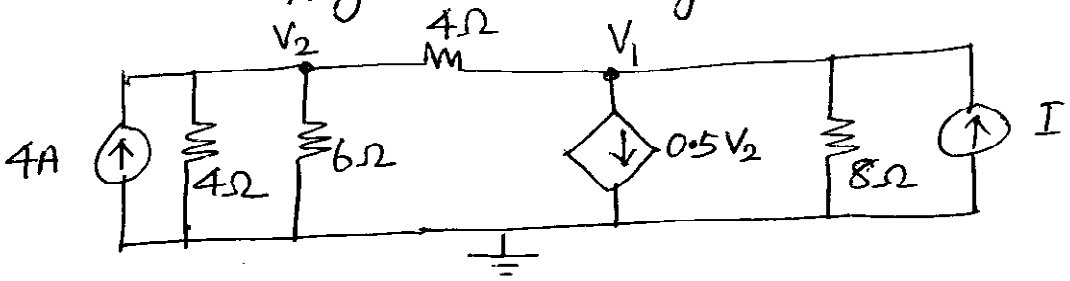

Figure 2

3. Consider the circuit shown in Figure 3, Find the portion of I and V that are due to the 12 –V voltage source. (b) Find the portion of I and V that are due to the 6-V voltage source. (c) Find the portion of I and V that are due to the 6-A current source. [7 marks]

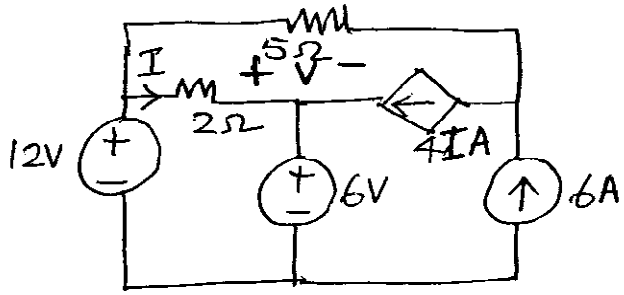

Figure 3

4. Design a non-inverting op-amp circuit for which the gain is 6 and total resistance used is 120 K Ω. [5 marks]